National Semiconductor

MICROCIRCUIT DATA SHEET

MNDM54LS161A-X REV 1B0

Original Creation Date: 04/16/98
Last Update Date: 07/10/02
Last Major Revision Date: 04/17/98

SYNCHRONOUS PRESETTABLE BINARY COUNTER

General Description

The 'LS161A is a high-speed synchronous modulo-16 binary counter. It is synchronously presettable for application in programmable dividers and has two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'LS161A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW.

Industry Part Number

54LS161A

NS Part Numbers

DM54LS161AJ-MLS
DM54LS161AW-MLS
DM54LS161AW/883

Prime Die

L161A

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Synchronous Counting and Loading
- High-speed Synchronous Expansion

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Input Voltage	-0.5V to +10.0V
VCC Pin Potential to Ground Pin	-0.5V to +7.0V
Junction Temperature under Bias	-55C to +175C
Current Applied to Output in LOW state (Max)	twice the rated Iol (ma)

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55 C to +125 C
Supply Voltage	
Military	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH (1)	Input High Current	VCC=5.5V, VM=2.7V, VINL=0.0V, VINH=4.5V	1, 3	INPUTS		20.0	uA	1, 2, 3
IIH (2)	Input High Current	VCC=5.5V, VM=2.7V, VINL=0.0V, VINH=4.5V	1, 3	$\overline{PE}$, CET		40.0	uA	1, 2, 3
IBVI (1)	Input High Current	VCC=5.5V, VM=10.0V, VINH=4.5V, VINL=0.0V	1, 3	INPUTS		0.1	mA	1, 2, 3
IBVI (2)	Input High Current	VCC=5.5V, VM=10.0V, VINH=4.5V, VINL=0.0V	1, 3	$\overline{PE}$, CET		0.2	mA	1, 2, 3
IIL (1)	Input LOW Current	VCC=5.5V, VM=0.4V, VINH=4.5V	1, 3	INPUTS	-0.03	-0.4	mA	1, 2, 3
IIL (2)	Input LOW Current	VCC=5.5V, VM=0.4V, VINH=4.5V	1, 3	$\overline{PE}$, CET	-0.06	-0.8	mA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VINL=0.0V, IOL=4.0mA, VINH=4.5V, VIL=0.7V	1, 3	OUTPUTS		0.4	V	1, 2, 3
VOH	High Level Output Voltage	VCC=4.5V, VIH=2.0V, IOH=-0.4mA, VINH=4.5V, VIL=0.7V, VINL=0.0V	1, 3	OUTPUTS	2.5		V	1, 2, 3
IOS	Short Circuit Output Current	VCC=5.5V, VINH=4.5V, VOUT=0.0V, VINL=0.0V	1, 3	OUTPUT	-20.0	-100	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA, VINH=4.5V	1, 3	INPUTS		-1.5	V	1, 2, 3
ICCL	Supply Current	VCC=5.5V, VINL=0.0V, VINH=4.5V	1, 3	VCC		31.0	mA	1, 2, 3
ICCH	Supply Current	VCC=5.5V, VINL=0.0V, VINH=4.5V	1, 3	VCC		31.0	mA	1, 2, 3

Electrical Characteristics

AC PARAMETER - 15pF

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=15pF Temp range: +25C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH (1)	Propagation Delay	VCC=5.0V, $\overline{PE}$ =4.5V	5	CP to Qn		20.0	ns	9
tpHL (1)	Propagation Delay	VCC=5.0V, $\overline{PE}$ =4.5V	5	CP to Qn		27.0	ns	9
tpLH (2)	Propagation Delay	VCC=5.0V, $\overline{PE}$ =GND	5	CP to Qn		24.0	ns	9
tpHL (2)	Propagation Delay	VCC=5.0V, $\overline{PE}$ =GND	5	CP to Qn		27.0	ns	9
tpHL (3)	Propagation Delay	VCC=5.0V	5	$\overline{MR}$ to Qn		28.0	ns	9
tpLH (4)	Propagation Delay	VCC=5.0V	5	CP to TC		25.0	ns	9
tpHL (4)	Propagation Delay	VCC=5.0V	5	CP to TC		21.0	ns	9
tpLH (5)	Propagation Delay	VCC=5.0V	5	CET to TC		14.0	ns	9
tpHL (5)	Propagation Delay	VCC=5.0V	5	CET to TC		14.0	ns	9
ts (H/L)	Setup Time	VCC=5.0V	5	Pn to CP	20.0		ns	9
th (H/L)	Hold Time	VCC=5.0V	5	Pn to CP	0.0		ns	9
ts (H/L) 2	Setup Time	VCC=5.0V	5	CET,CEP,$\overline{PE}$ to CP	20.0		ns	9
th (H/L) 2	Hold Time	VCC=5.0V	5	CET,CEP,$\overline{PE}$ to CP	0.0		ns	9
tREC	Rise Time	VCC=5.0V	5	$\overline{MR}$ to CP	20.0		ns	9
tW (H) 1	Pulse Width	VCC=5.0V	5	CPn	15.0		ns	9
tW (L) 1	Pulse Width	VCC=5.0V	5	CPn	25.0		ns	9
tW (L) 2	Pulse Width	VCC=5.0V	5	$\overline{MR}$	15.0		ns	9
fMAX	Maximum Clock Frequency	VCC=5.0V	5	CP	25.0		MHZ	9

Electrical Characteristics

AC PARAMETER - 50pF

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pF, RL=2K ohms Temp range: -55C to +125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH (1)	Propagation Delay	VCC=5.0V PE =4.5V	2, 4	CP to Qn	2.0	25.0	ns	9
			2, 4	CP to Qn	2.0	33.0	ns	10, 11
tpHL (1)	Propagation Delay	VCC=5.0V PE =4.5V	2, 4	CP to Qn	2.0	32.0	ns	9
			2, 4	CP to Qn	2.0	42.0	ns	10, 11
tpLH (2)	Propagation Delay	VCC=5.0V PE =GND	2, 4	CP to Qn	2.0	29.0	ns	9
			2, 4	CP to Qn	2.0	38.0	ns	10, 11
tpHL (2)	Propagation Delay	VCC=5.0V PE =GND	2, 4	CP to Qn	2.0	32.0	ns	9
			2, 4	CP to Qn	2.0	42.0	ns	10, 11
tpHL (3)	Propagation Delay	VCC=5.0V	2, 4	MR to Qn	2.0	33.0	ns	9
			2, 4	MR to Qn	2.0	43.0	ns	10, 11
tpLH (4)	Propagation Delay	VCC=5.0V	2, 4	CP to TC	2.0	30.0	ns	9
			2, 4	CP to TC	2.0	39.0	ns	10, 11
tpHL (4)	Propagation Delay	VCC=5.0V	2, 4	CP to TC	2.0	26.0	ns	9
			2, 4	CP to TC	2.0	34.0	ns	10, 11
tpLH (5)	Propagation Delay	VCC=5.0V	2, 4	CET to TC	2.0	19.0	ns	9
			2, 4	CET to TC	2.0	25.0	ns	10, 11
tpHL (5)	Propagation Delay	VCC=5.0V	2, 4	CET to TC	2.0	19.0	ns	9
			2, 4	CET to TC	2.0	25.0	ns	10, 11
ts (H/L) 1	Setup Time	VCC=5.0V	2, 4	Pn to CP	20.0		ns	9
			2, 4	Pn to CP	25.0		ns	10, 11

Electrical Characteristics

AC PARAMETER - 50pF(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pF, RL=2K ohms Temp range: -55C to +125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
th (H/L) 1	Hold Time	VCC=5.0V	2, 4	Pn to CP	0.0		ns	9
			2, 4	Pn to CP	5.0		ns	10, 11
ts (H/L) 2	Setup Time	VCC=5.0V	2, 4	CET,CEP,PE to CP	20.0		ns	9
			2, 4	CET,CEP,PE to CP	25.0		ns	10, 11
th (H/L) 2	Hold Time	VCC=5.0V	2, 4	CET,CEP,PE to CP	0.0		ns	9
			2, 4	CET,CEP,PE to CP	5.0		ns	10, 11
tREC	Rise Time	VCC=5.0V	2, 4	$\overline{MR}$ to CP	20.0		ns	9
			2, 4	$\overline{MR}$ to CP	25.0		ns	10, 11
tw (H) 1	Pulse Width	VCC=5.0V	2, 4	CPn	15.0		ns	9
			2, 4	CPn	20.0		ns	10, 11
tw (L) 1	Pulse Width	VCC=5.0V	2, 4	CP	25.0		ns	9
			2, 4	CP	30.0		ns	10, 11
tw (L) 2	Pulse Width	VCC=5.0V	2, 4	$\overline{MR}$	15.0		ns	9
			2, 4	$\overline{MR}$	20.0		ns	10, 11
fMAX	Clock Frequency	VCC=5.5V	2, 4	CP	25.0		MHZ	9
			2, 4	CP	20.0		MHZ	10, 11

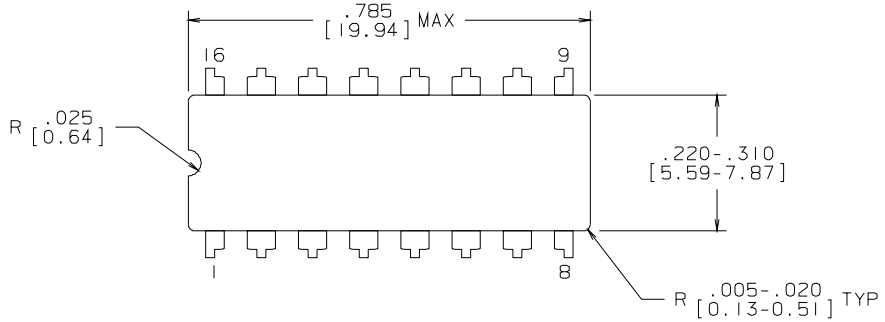
Note 1: Screen tested 100% on each device at -55C, +25C & +125C temperature, subgroups A1, 2, 3, 7 & 8.
Note 2: Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, subgroup A9. Subgroups 10 & 11 are guaranteed, not tested.
Note 5: Guaranteed, not tested.

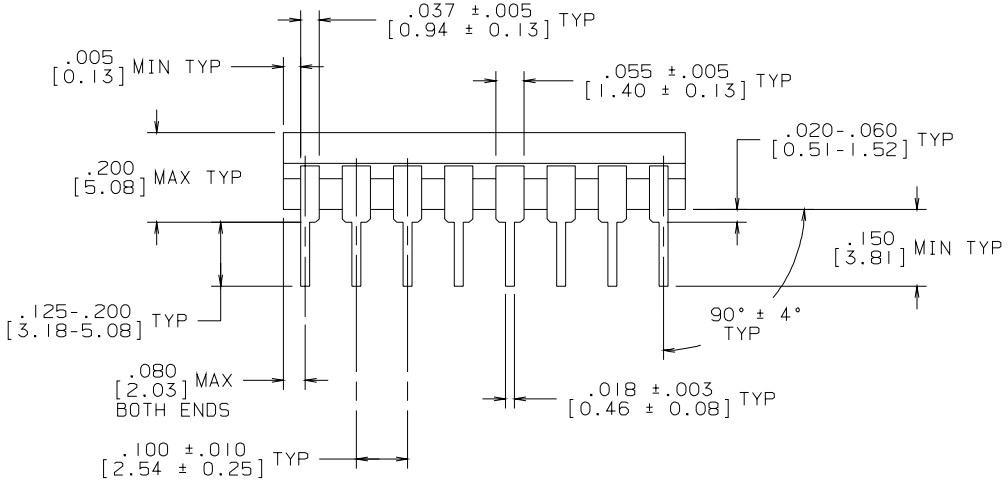
Graphics and Diagrams

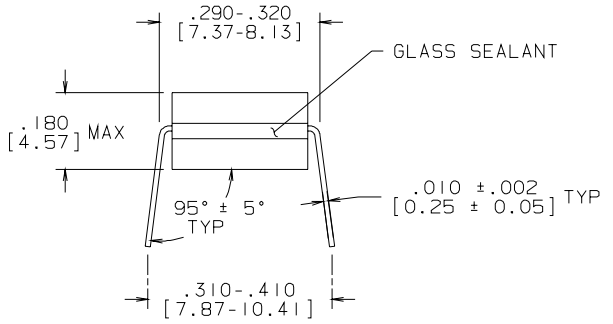
GRAPHICS#	DESCRIPTION
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
W16ARL	CERPACK (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

PROJECTION

INCH [MM]

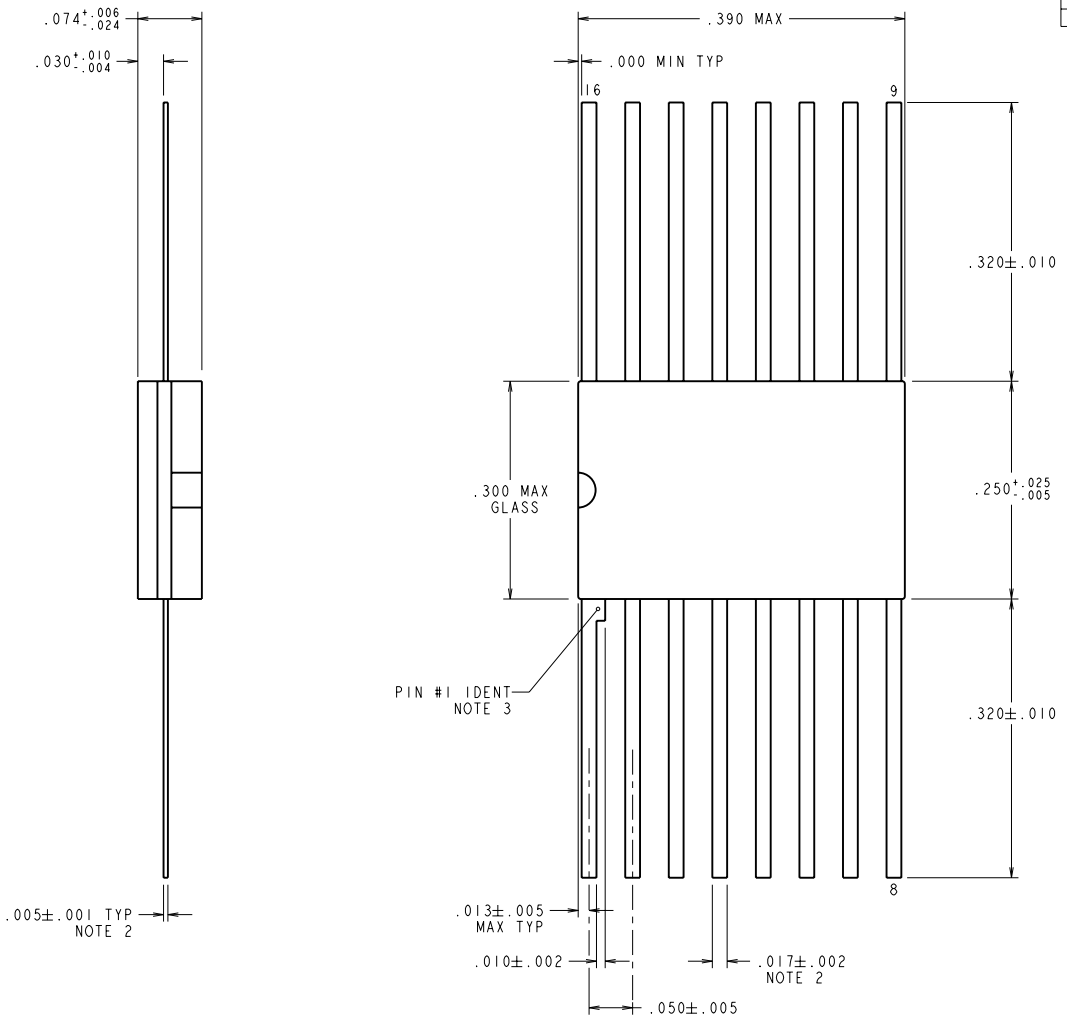
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-092, VARIATION AC, DATED 04/89.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD

PROJECTION

INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0002958	07/10/02	Donald B. Miller	Archive Table 1 54LS161A, Rev C0.2. Release MDS MNDM54LS161A-X, Rev 1A0. Changed note 5 (guaranteed not tested) in the AC (50pF) notes reference column to note 2 (screen tested 100% at +25C, subgroup 9) & to note 4 (Subgroups 10 & 11 are guaranteed, not tested). Changed note 2 in the AC (15pF) notes reference column to note 5. Re-worded the phrase in note 4 from "and periodically at +125C & -55C, subgroups 10 & 11" to "subgroups 10 & 11 are guaranteed, not tested".
1B0	M0004023	07/10/02	Rose Malone	Update MDS: MNDM54LS161A-X, Rev. 1A0 to MNDM54LS161A-X, Rev. 1B0. Updated NS Part Numbers on Main Table, Added Mkt Dwg.'s to Graphics Section.