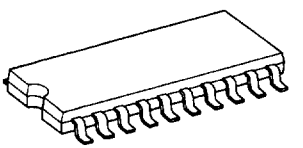
TC74LVQ245F/FW/FS

OCTAL BUS TRANSCEIVER

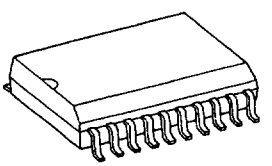
The TC74LVQ245 is a high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation.
It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.
The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74LVQ245F



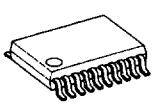
SOP20-P-300

TC74LVQ245FW



SOL20-P-300

TC74LVQ245FS



SSOP20-P-225A

Weight SOP20-P-300 : 0.22g (Typ.)
SOL20-P-300 : 0.46g (Typ.)
SSOP20-P-225A : 0.09g (Typ.)

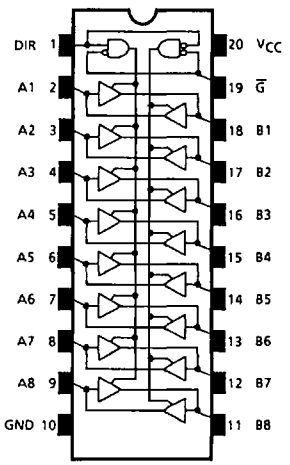
FEATURES

- High speed : t_{pd} = 5.8ns (Typ.) (V_{CC} = 3.3V)
- Low power dissipation : I_{CC} = 4μA (Max.) (Ta = 25°C)
- Input voltage level : V_{IL} = 0.8V (Max.) (V_{CC} = 3V)
  V_{IH} = 2.0V (Min.) (V_{CC} = 3V)
- Symmetrical output impedance
  : $|I_{OH}| = I_{OL}$ = 12mA (Min.)
- Balanced propagation delays
  : $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74HC245

APPLICATION NOTES

Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

PIN ASSIGNMENT



(TOP VIEW)

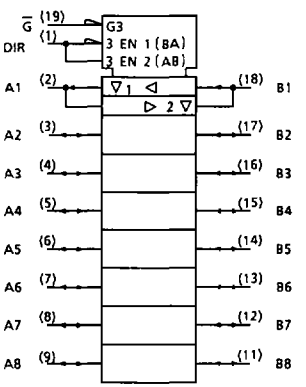
TRUTH TABLE

INPUTS		OUTPUTS	FUNCTION	
$\overline{G}$	DIR		A-BUS	B-BUS
L	L	A = B	OUTPUT	INPUT
L	H	B = A	INPUT	OUTPUT
H	X	Z	High Impedance	

X : Don't Care

Z : High Impedance

IEC LOGIC SYMBOL



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage (DIR, $\overline{G}$)	V_{IN}	−0.5~V_{CC}+0.5	V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10s	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage (DIR, $\overline{G}$)	V_{IN}	0~V_{CC}	V
Bus I/O Voltage	$V_{I/O}$	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	"H" Level	V_{IH}			3.0	2.0	—	—	2.0	—	V
	"L" Level	V_{IL}			3.0	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
				I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.5	—	±5.0	μA
Input Leakage Current		I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC characteristics (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		2.7	—	8.0	14.1	1.0	17.0	ns
	t_{pHL}		3.3 ± 0.3	—	6.7	10.0	1.0	11.5	
Output Enable Time	t_{pZL}		2.7	—	10.7	18.3	1.0	20.0	ns
	t_{pZH}		3.3 ± 0.3	—	8.9	13.0	1.0	14.0	
Output Disable Time	t_{pLZ}		2.7	—	7.9	20.4	1.0	22.0	ns
	t_{pHZ}		3.3 ± 0.3	—	6.6	14.5	1.0	15.0	
Output To Output Skew	t_{osLH}	(Note 1)	2.7	—	—	1.5	—	1.5	ns
	t_{osHL}		3.3 ± 0.3	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	DIR, $\overline{G}$ (Note 2)		—	5	10	—	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn		—	13	—	—	—	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	38	—	—	—	pF

(Note 1) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :

$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per bit)

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.6	1.0	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.6	−1.0	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V