3.3V CMOS Static RAM
4 Meg (512K x 8-Bit)

IDT71V424YS
IDT71V424YL

Features

- 512K x 8 advanced high-speed CMOS Static RAM
- JEDEC Center Power / GND pinout for reduced noise
- Equal access and cycle times
  - — *Commercial and Industrial: 10/12/15ns*
- Single 3.3V power supply
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 36-pin, 400 mil plastic SOJ package and 44-pin, 400 mil TSOP.

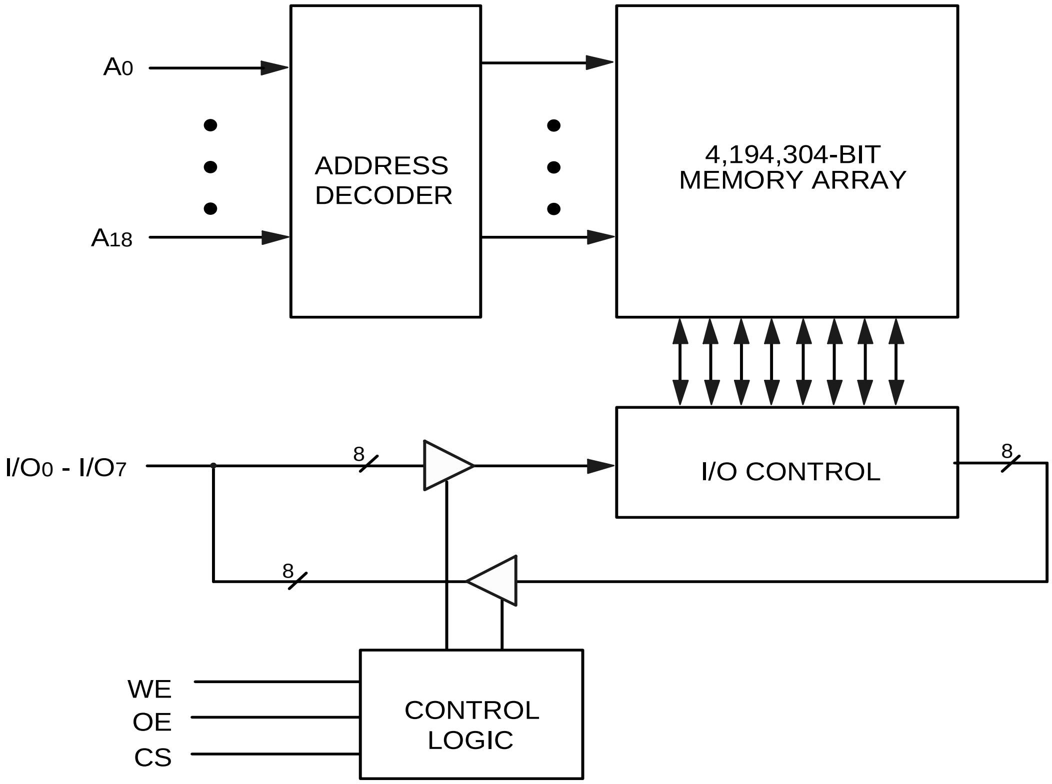
Description

The IDT71V424 is a 4,194,304-bit high-speed Static RAM organized as 512K x 8. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71V424 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71V424 are TTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71V424 is packaged in a 36-pin, 400 mil Plastic SOJ and 44-pin, 400 mil TSOP.

Functional Block Diagram



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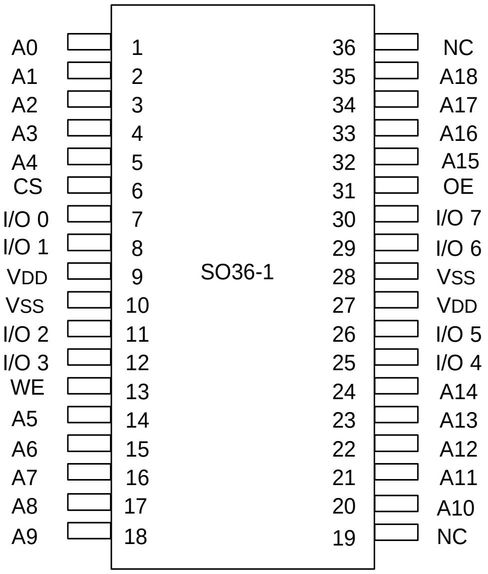
JULY 2004

Pin Configuration



SOJ
Top View

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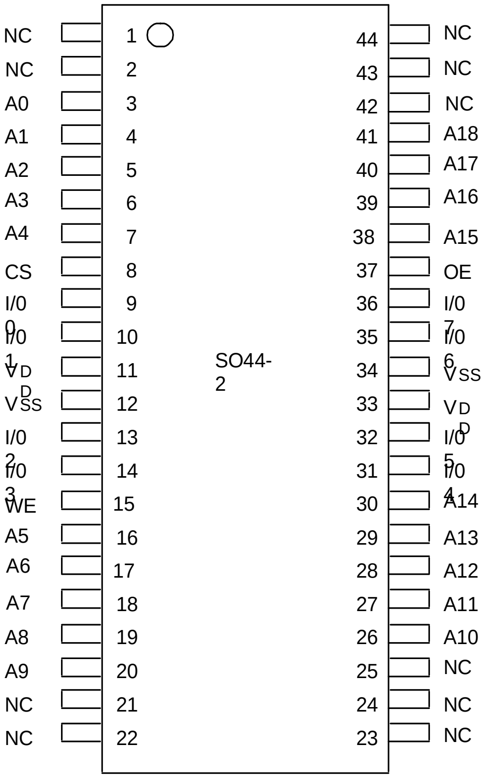
Pin Configuration



TSOP
Top View

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Pin Description

A$_0$ – A$_{18}$	Address Inputs	Input
$\overline{CS}$	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
I/O$_0$ - I/O$_7$	Data Input/Output	I/O
V$_{DD}$	3.3V Power	Power
V$_{SS}$	Ground	Gnd

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Capacitance

(T$_A$ = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$ = 3dV	7	pF
C$_{I/O}$	I/O Capacitance	V$_{OUT}$ = 3dV	8	pF

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NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

Truth Table[1,2]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	DATA$_{OUT}$	Read Data
L	X	L	DATA$_{IN}$	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I$_{SB}$)
V$_{HC}$[3]	X	X	High-Z	Deselected - Standby (I$_{SB1}$)

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NOTES:

1. H = V$_{IH}$, L = V$_{IL}$, x = Don't care.
2. V$_{LC}$ = 0.2V, V$_{HC}$ = V$_{DD}$ -0.2V.
3. Other inputs ≥V$_{HC}$ or ≤V$_{LC}$.

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{DD}	Supply Voltage Relative to V_{SS}	-0.5 to +4.6	V
V_{IN}, V_{OUT}	Terminal Voltage Relative to V_{SS}	-0.5 to V_{DD}+0.5	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1	W
I_{OUT}	DC Output Current	50	mA

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NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	Vss	VDD
Commercial	0°C to +70°C	0V	See Below
Industrial	–40°C to +85°C	0V	See Below

6468 tbl 05

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3(1)	V
V_{IL}	Input Low Voltage	-0.3(2)	—	0.8	V

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NOTES:

1. V_{IH} (max.) = V_{DD}+2V a.c. (Pulse Width $\leq$ 5ns) for I $\leq$ 20mA.
2. V_{IL} (min.) = –2V a.c. (Pulse Width $\leq$ 5ns) for I $\leq$ 20mA.

DC Electrical Characteristics

(V_{DD} = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Condition	IDT71V424		
			Min.	Max. Unit	
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = V_{SS} to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{DD} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{DD}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{DD} = Min.	2.4	—	V

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DC Electrical Characteristics(1, 2, 3)

(V_{DD} = Min. to Max., V_{LC} = 0.2V, V_{HC} = V_{DD} – 0.2V)

Symbol	Parameter		71V424YS/YL 10		71V424YS/YL 12		71V424YS/YL 15		Unit
			Com'l.	Ind.(5)	Com'l.	Ind.(5)	Com'l.	Ind.(5)	
I_{CC}	Dynamic Operating Current $\overline{CS}$ $\leq$ V_{LC}, Outputs Open, V_{DD} = Max., f = f_{MAX}(4)	S	180	180	170	170	160	160	mA
		L	165	—	155	155	145	145	mA
I_{SB}	Dynamic Standby Power Supply Current $\overline{CS}$ $\geq$ V_{HC}, Outputs Open, V_{DD} = Max., f = f_{MAX}(4)	S	60	60	55	55	50	50	mA
		L	55	—	50	50	45	45	mA
I_{SB1}	Full Standby Power Supply Current (static) $\overline{CS}$ $\geq$ V_{HC}, Outputs Open, V_{DD} = Max., f = 0(4)	S	20	20	20	20	20	20	mA
		L	10	—	10	10	10	10	mA

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NOTES:

1. All values are maximum guaranteed values.
2. All inputs switch between 0.2V (Low) and V_{DD} - 0.2V (High).
3. Power specifications are preliminary.
4. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
5. Standard power 10ns (S10) speed grade only.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1, 2 and 3

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AC Test Loads

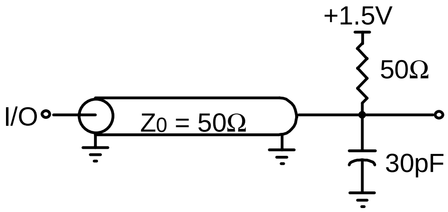

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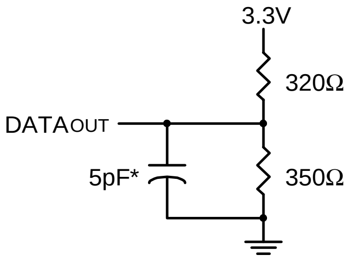
Figure 1. AC Test Load



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*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

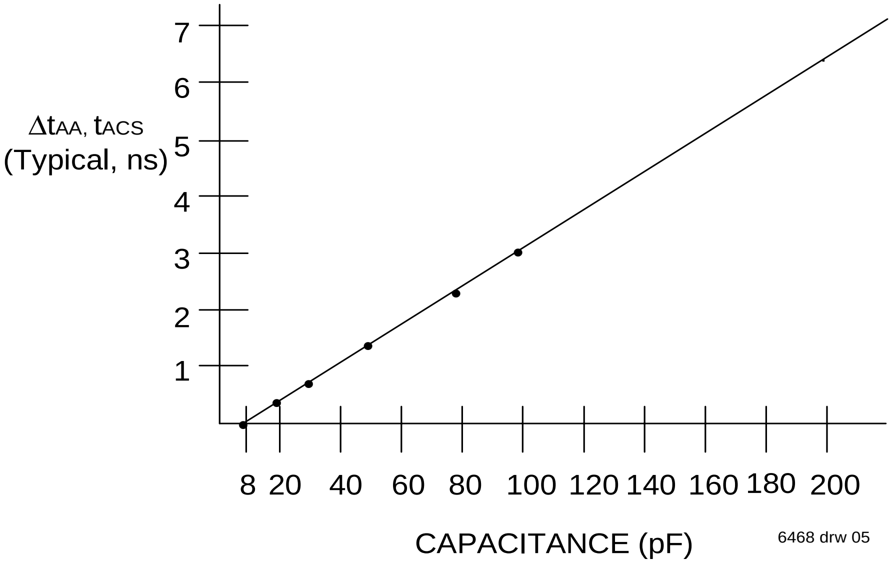

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Figure 3. Output Capacitive Derating

AC Electrical Characteristics

(Vcc = 3.3V ± 10%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	71V424S/L10(2)		71V424S/L12		71V424S/L15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	4	—	4	—	4	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	5	—	6	—	7	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	5	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	10	—	12	—	15	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	8	—	8	—	10	—	ns
t_{CW}	Chip Select to End of Write	8	—	8	—	10	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	8	—	10	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	6	—	6	—	7	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	3	—	3	—	3	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	6	—	7	—	7	ns

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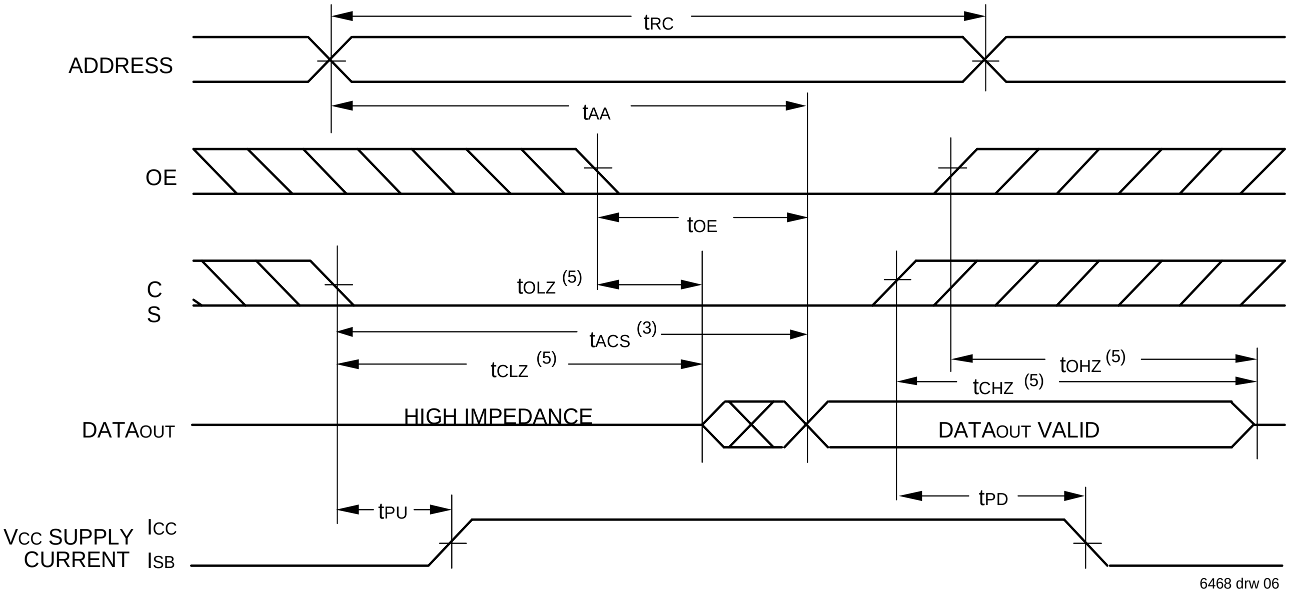
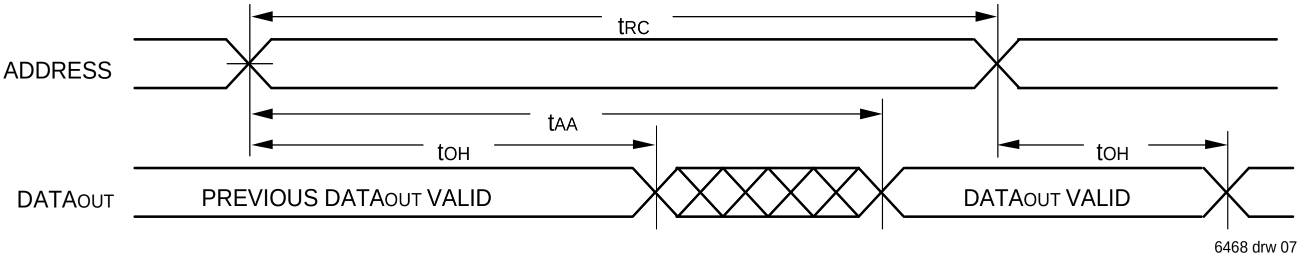
NOTES:

1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
2. 0ºC to +70ºC temperature range only for low power 10ns (L10) speed grade.

Timing Waveform of Read Cycle No. 1(1)

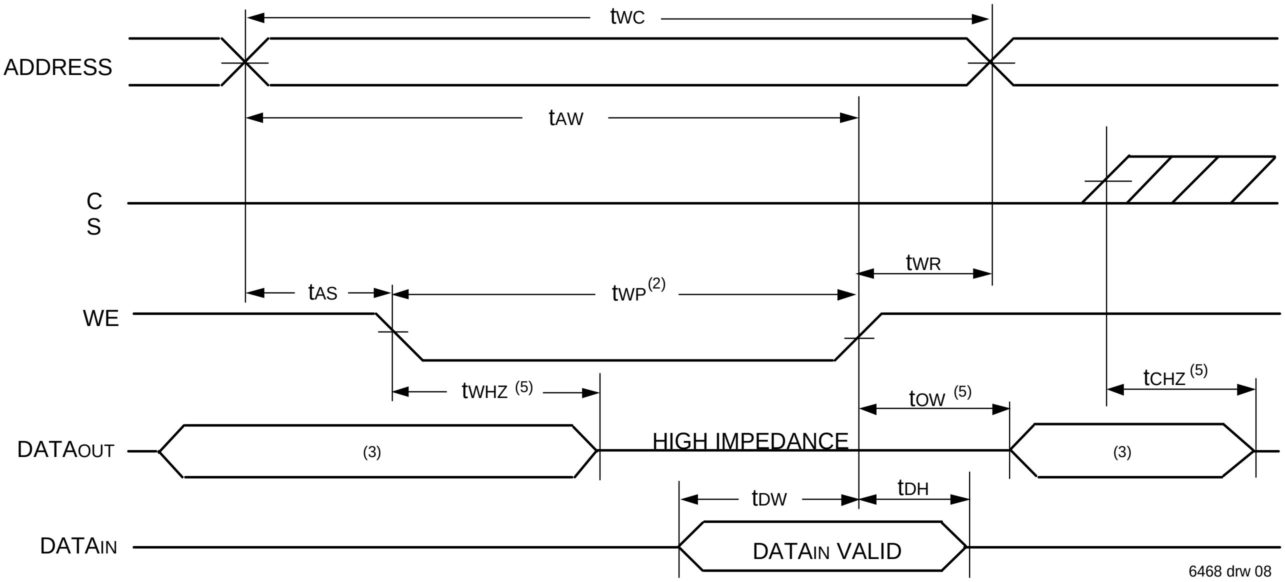


Timing Waveform of Read Cycle No. 2(1, 2, 4)

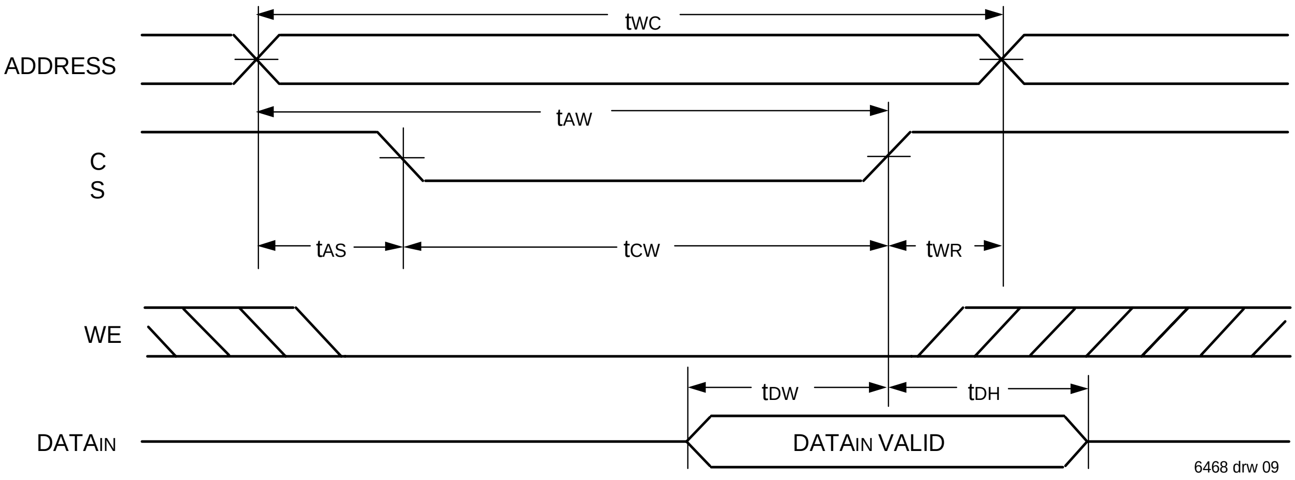


NOTES:
1. $\overline{\text{WE}}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{\text{CS}}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{\text{CS}}$ transition LOW; otherwise tAA is the limiting parameter.
4. $\overline{\text{OE}}$ is LOW.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1, 2, 4)



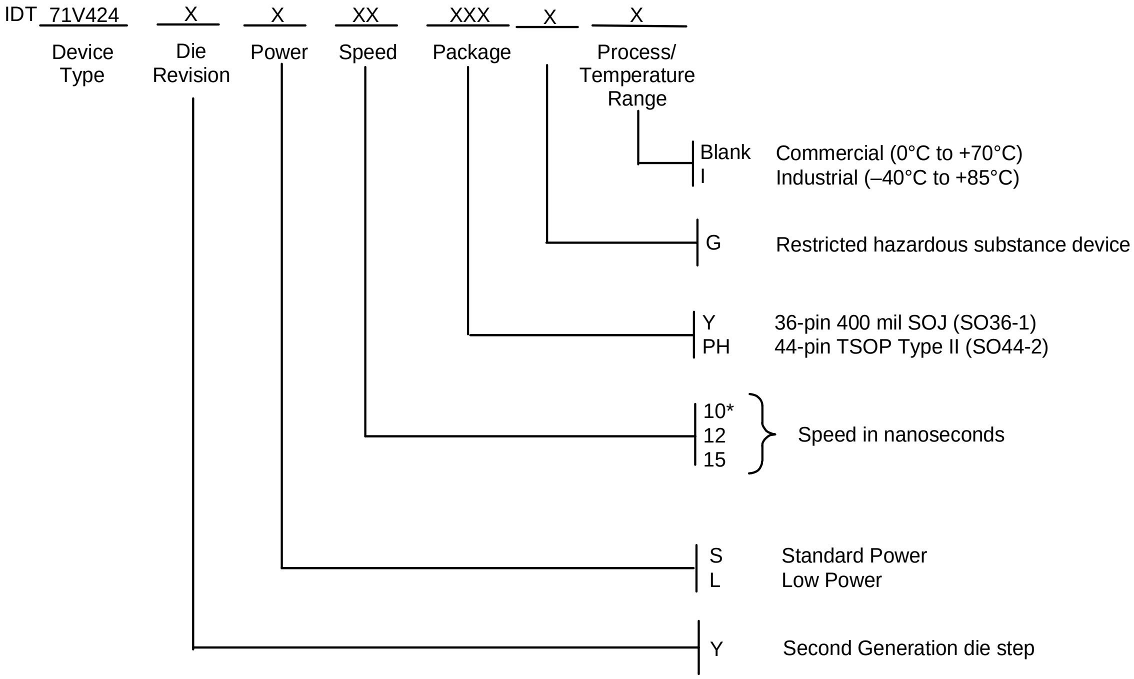
Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1, 4)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS}$ must be active during the t_{CW} write period.
5. Transition is measured ±200mV from steady state.

Ordering Information



* Commercial only for low power 10ns (L10) speed grade.

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Datasheet Document History

07/16/04	Released new datasheet

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