FAIRCHILD
A Schlumberger Company

F100164
16-Input Multiplexer

F100K ECL Product

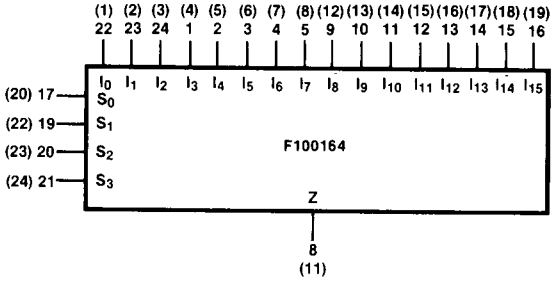
Description

The F100164 is a 16-input multiplexer. Data paths are controlled by four Select lines (S_0-S_3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data.

Pin Names

I_0-I_{15}	Data Inputs
S_0-S_3	Select Inputs
Z	Data Output

Logic Symbol



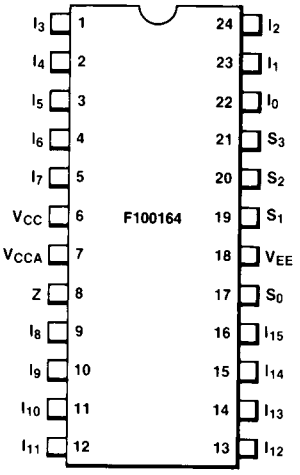
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information

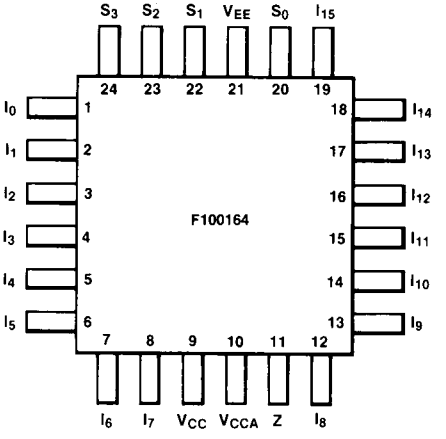
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

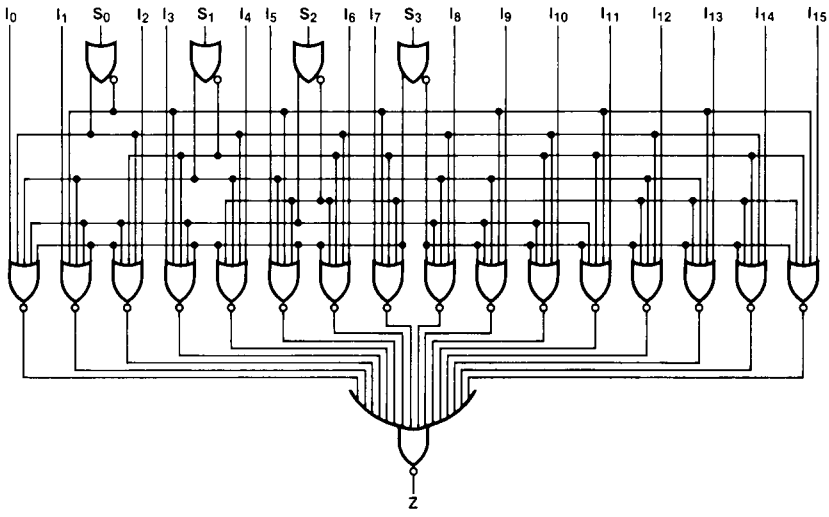
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table

Select Inputs				Output
S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current I_n S_0, S_1 S_2, S_3			 280 240 200	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−105	−70	−49	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

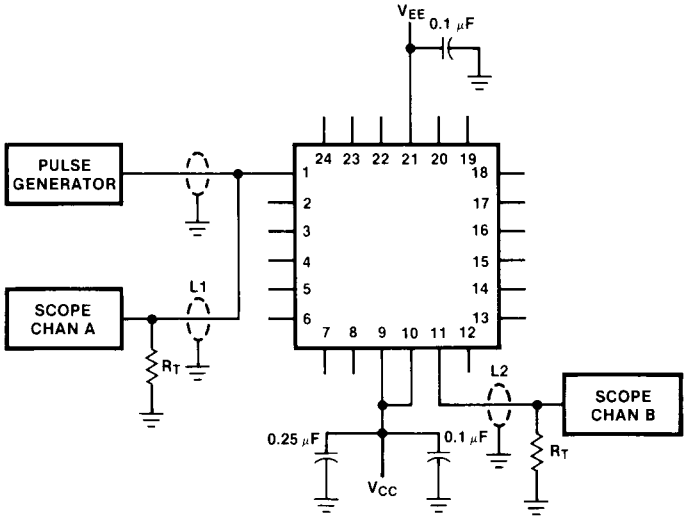
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.80	2.20	0.90	2.35	0.90	2.55	ns	
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	1.45	3.10	1.45	3.20	1.55	3.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	1.10	2.45	1.10	2.50	1.20	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.80	2.00	0.90	2.15	0.90	2.35	ns	
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	1.45	2.90	1.45	3.00	1.55	3.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	1.10	2.25	1.10	2.30	1.20	2.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	

*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak, for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times