DAC-8565 Complete High Speed 12-Bit Monolithic D/A Converter

Features

- Nonlinearity 1/2 LSB — 0.012%
- Differential nonlinearity — 0.012% (13 bits)
- Settles to 1/2 LSB in 300nS
- On-chip buried zener voltage reference
- Linearity guaranteed over temperature
- Low power — 225mW including reference
- Direct interface to all major logic families
- Includes trimmed application resistors

Highlights

- The DAC-8565 is a monolithic 12-Bit DAC that has on-board a self-contained voltage reference plus application resistors.
- The device incorporates interdigitizing of the elements forming the currents of the 3 MSBs of the DAC. Interdigitizing minimizes the effects of thin film sputtering, thermal, and diffusion gradients in the most critical portions of the design. Excellent linearity distributions are achieved prior to trimming, thus ensuring optimal stability of nonlinearity over temperature, as well as ensuring stability versus time.
- The thin film resistors have a trim tab which is distant from the main body of the resistor. This resistor geometry ensures near perfect nonlinearity after trim, and this geometry also reduces damage due to laser trimming.
- The internal reference is laser trimmed to 10 Volts with a ±1.0% maximum error. The reference voltage is available externally and can supply 2mA beyond that required for the reference and bipolar offset resistors.
- The DAC-8565 contains SiCr thin film application resistors which can be used with either an external op amp, creating a precision voltage output DAC, or as input resistors for a successive approximation A/D converter. The resistors are inherently matched and are laser trimmed to guarantee minimum full scale and bipolar offset errors.
- The DAC-8565S grade guarantees linearity and monotonicity over the -55°C to +125°C range and is available fully processed to MIL-STD-883, Level B.

Description

The DAC-8565 is a fast 12-bit digital-to-analog converter. Inside the 24 pin DIP package are all of the circuit functions required for a complete DAC: a stable zener voltage reference, a reference amplifier and resistors, twelve laser trimmed binary weighted current sources, twelve high speed precision current steering switches, and laser trimmed span and bipolar offset application resistors.

The high performance and flexibility of the DAC-8565 are achieved through circuit design and layout, SiCr thin film resistor processing, and interactive computer-controlled laser trimming. The DAC-8565 settles to 1/2 LSB in 300nS typically, with a maximum settling time of 400nS. Accuracy is specified at a **maximum** of 1/2 LSB for all grades.

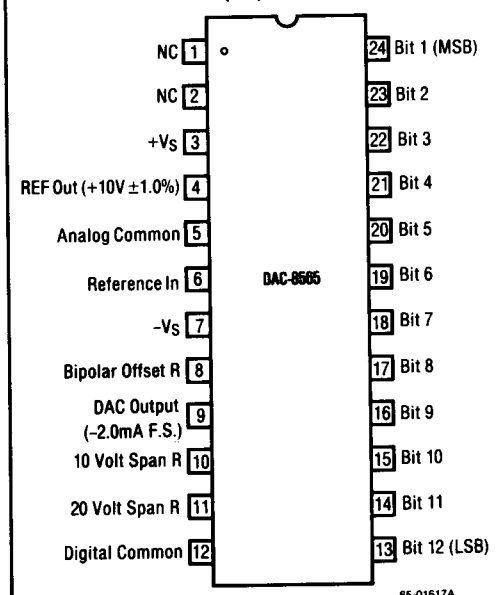
High speed and accuracy coupled with inherent high output impedance make the DAC-8565 the ideal DAC for high speed display drivers, high speed control systems, and in conjunction with the RC4805 high speed latching comparator in anlaog-to-digital converters.

The zener voltage reference is laser trimmed to optimize both temperature drift and absolute output voltage. Typical reference drift is better than 15 ppm/°C (S and J grade).

The DAC-8565 is available in three performance grades. The DAC-8565JS and DS grades are specified over 0°C to +70°C, while the SS grade is specified over the -55°C to +125°C temperature range.

Connection Information

24-Lead Sidebrazed DIP
(Top View)



Ordering Information

Part Number	Package	Operating Temperature Range
DAC-8565DS	S	0°C to +70°C
DAC-8565JS	S	0°C to +70°C
DAC-8565SS	S	-55°C to +125°C
DAC-8565SS/883B	S	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
S = 24-lead small outline DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

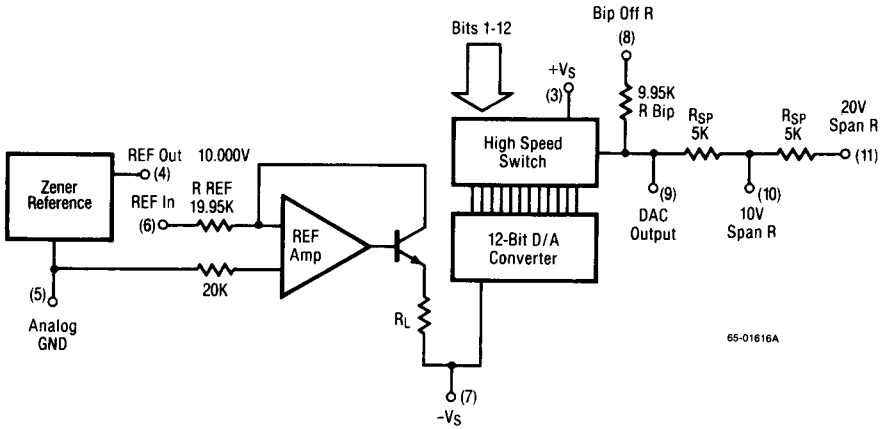
Absolute Maximum Ratings

Supply Voltages ..... ±18V
Logic Inputs ..... -1V to +18V
Analog Common to Digital Common ..... ±1V
Voltage on DAC Output (Pin 9) ..... -3V to +18V
Reference Input to Analog Common ..... ±12V
Bipolar Offset to Analog Common ..... ±12V
10V Span R to Analog Common ..... ±12V
20V Span R to Analog Common ..... ±24V
Ref Out ..... Indefinite Short to Either Common, Momentary Short to $+V_S$
Lead Soldering Temperature (60 Sec) ..... +300°C

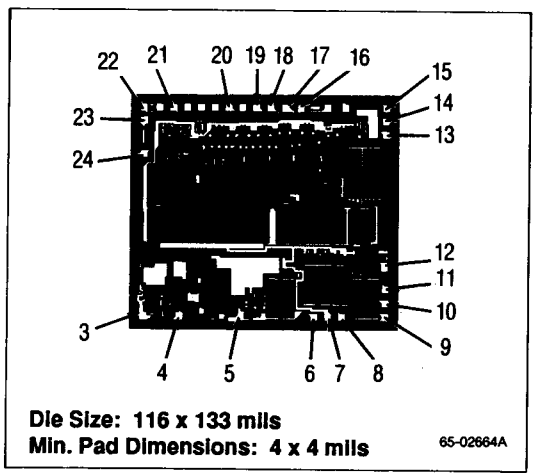
Thermal Characteristics

	24-Lead Sidebrazed DIP
Max. Junction Temp.	175°C
Max. P_D T_A <50°C	1042 mW
Therm. Res θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For T_A >50°C Derate at	8.38 mW/°C

Functional Block Diagram



Mask Pattern



Electrical Characteristics (T_A = +25°C, $+V_S$ = +15V, $-V_S$ = -15V, unless otherwise noted)

Parameters	Test Conditions	DAC-8565S/J			DAC-8565D			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		12	12	12	12	12	12	Bits
Monotonicity		12	12	12	12	12	12	Bits
Nonlinearity			±.006	±.012		±.006	±.012	%FS
Differential Nonlinearity	Deviation From Ideal Step Size		±.007	±.018		±.007	±.018	%FS
Full Scale Current	Unipolar (all bits on) Internal Reference (full temperature)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
	Bipolar (Figure 2 R_2 = 50Ω fixed) All Bits On or Off (full temperature)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	
Output Resistance		1.0	10		1.0	10		MΩ
Output Voltage Compliance	R_O > 1.0MΩ (full temperature)	-1.5		+10	-1.5		+10	V
Output Capacitance			25			25		pF
Offset Unipolar Zero Scale			0.001	0.005		0.002	0.01	%FS
Bipolar	(Figure 2 R_2 = 50Ω Fixed)		0.05	0.15		0.10	0.30	
Settling Time to 1/2 LSB (guaranteed by design)	All Bits On to Off or Off to On		300	400		300	400	nS
Full Scale Transition Rise Time	10% to 90% Plus Propagation Delay		30			30		nS
Fall Time	90% to 10% Plus Propagation Delay		30			30		
Logic Input Levels Logic "0"	(Full temperature)			0.8			0.8	V
Logic "1"	(Full temperature)	2.0			2.0			
Logic Input Current	V_{IN} = 0V to 18V (Full temperature)			80			80	μA
Reference Input Current	V_{REF} = 10.000V	0.4	0.5	0.6	0.4	0.5	0.6	mA
Input Resistance		15	20	25	15	20	25	kΩ
Supply Range	(Full temperature)	±13.5	±15	±16.5	±13.5	±15	±16.5	V
Supply Current	$+V_S$ = +13.5 to +16.5		3.0	5.0		3.0	5.0	mA
	$-V_S$ = -13.5 to -16.5		-10	-18		-10	-18	
Power Consumption			195	345		195	345	mW

Electrical Characteristics (Continued)

Parameters	Test Conditions	DAC-8565S/J			DAC-8565D			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Sensitivity	$+V_S$ = +15V, ±10%		.0003	.001		.0007	.002	%FS
	$-V_S$ = -15V, ±10%		.0015	.0025		.002	.0035	
Reference Output Voltage	External Current = 1mA	9.9	10	10.1	9.7	10	10.3	V
Reference Output Current	(Available for External Loads)	1.0	2.0		1.0	2.0		mA
External Adjustment Gain Error With Fixed 50Ω Resistor for R2	Figure 1		±0.1	±0.25		±0.1	±0.50	%FS
Bipolar Zero Error With Fixed 50Ω Resistor for R1	Figure 2		±0.05	±0.15		±0.05	±0.3	%FS
Gain Adjustment Range	Figure 1	±0.25			±0.50			%FS
Bipolar Zero Adjustment Range	Figure 2	±0.15			±0.3			%FS
Programmable Output Range	(See Figs. 1, 2, 3 & 4)	0		5.0	0		5.0	V
		-2.5		+2.5	-2.5		+2.5	
		0		10	0		10	
		-5.0		+5.0	-5.0		+5.0	
		-10		+10	-10		+10	
Wideband Reference Noise	0.1 to 1MHz		1.0			1.0		mV
DAC-8565S = -55°C to +125°C, DAC-8465J/D = 0°C to +70°C (unless otherwise noted)								
Resolution		12	12	12	12	12	12	Bits
Monotonicity		12	12	12	12	12	12	Bits
Nonlinearity			±.012	±.018		±.012	±.018	%FS
Differential Nonlinearity	Deviation From Ideal Step Size	Monotonicity Guaranteed						
Temperature Coefficients Unipolar Zero			1.0	2.0		1.0		
Bipolar Zero			5.0	10		10		
Differential Nonlinearity			2.0			2.0		ppm/°C
Gain With Internal Reference	Full Scale		15	30		30		
Gain With External Reference			5.0			5.0		
Supply Current	$+V_S$ = +13.5 to +16.5V		4.0	7.0		4.0	7.0	mA
	$-V_S$ = -13.5 to -16.5V		-12	-18		-12	-18	

Connecting the DAC-8565 for Buffered Voltage Output

The standard current to voltage conversion connections using an operational amplifier are shown in Figure 1. If a low offset voltage operational amplifier (OP-07, OP-27, OP-37) is used, excellent performance can be obtained in most applications without trimming. If a fixed 50Ω resistor is substituted for the 100Ω trimmer of Figure 1, unipolar zero will be typically much less than ±1/2 LSB and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer (R1) of Figure 2 will give a bipolar zero error typically within ±2.0 LSB.

The configuration of Figure 1 will provide a unipolar 0V to +10V output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

Unipolar Configurations

Step 1 — Gain Adjust
Turn all bits on and adjust 100Ω gain trimmer R1 until the output is +9.9976 (full scale should be adjusted to 1 LSB less than +10.000V). If a +10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

In most cases a zero trim is not needed, due to the extremely low zero scale output current. Pin 8 should be connected to pin 9 for unipolar operation.

Bipolar Configurations

These configurations will yield ±5.0V, ±10V, or ±2.5V, with positive full scale occurring with all bits on (all 1's).

Step 1 — Offset Adjust
Turn off all bits. Adjust 100Ω trimmer R1 to give -5.000, -10.000, or -2.500V, depending upon the full scale range selected.

Step 2 — Gain Adjust
Turn on all bits and adjust trimmer R2 to give a reading of +4.9976, +9.9951, or +2.4988V depending upon the range.

If a precision op amp such as the OP-07, OP-27, or OP-37 is used no separate trimming of the operational amplifier is required or recommended.

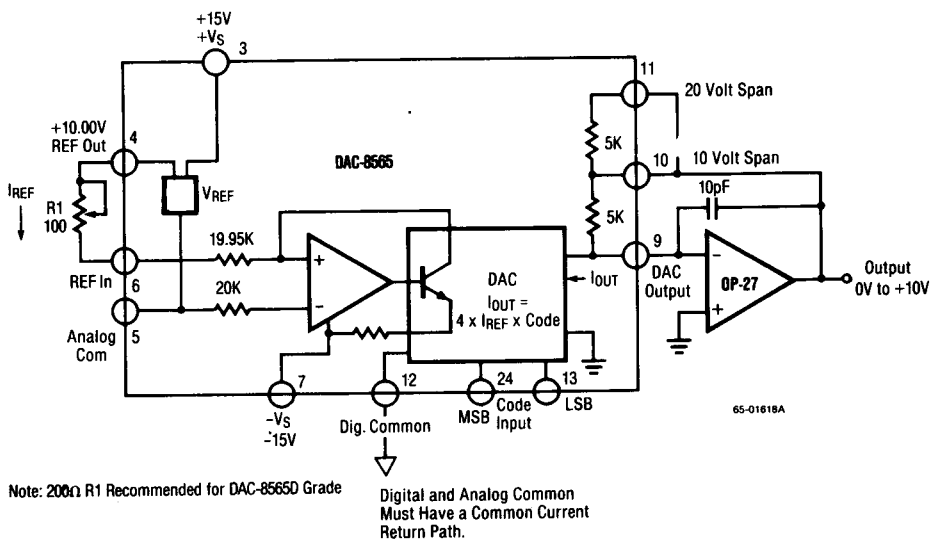
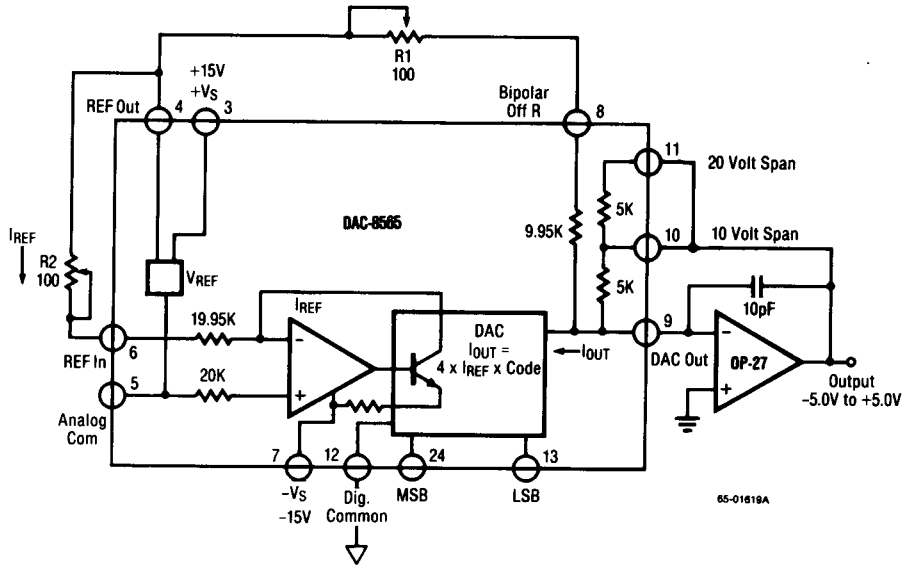


Figure 1. 0V to +10V Unipolar Voltage Output



Note: 200Ω R1 and R2 Pots are Recommended for DAC-8565D Grade

Figure 2. ±5.0V Bipolar Voltage Output

0V to +5.0V Range

A 0V to +5V output can be achieved by modifying the configuration of Figure 1. Tie pin 11 to pin 9 rather than to pin 10 and adjust full scale to +4.9988V.

Internal/External Reference Use

The DAC-8565 has an internal bandgap voltage reference which is trimmed for both temperature coefficient and absolute accuracy. The reference is buffered with an internal operational amplifier and is capable of driving a minimum of 5.0mA in addition to the 0.5mA into REF_{IN} and 1.0mA into Bipolar Offset for the DAC. The reference is typically trimmed to ±0.2% but specified to 1.0% (J, S grades) max error. Testing and specifying of absolute unipolar and bipolar full scale is done using the internal reference. For noise performance of the reference see Figure 6.

Digital Input Considerations

The DAC-8565 uses a positive true straight binary code for unipolar outputs (all 1's give full scale output) and an offset binary code for bipolar output ranges. In the bipolar mode, all 0's give -F.S., with only the MSB on give 0.00V, and with all 1's, +F.S. is achieved.

The threshold of the digital input circuitry is set at +1.4V independent of supply voltage. The bit lines are compatible with TTL, DTL, CMOS, and unbuffered CMOS.

Application of Analog and Digital Commons

The DAC-8565 separates analog and digital grounds to optimize accuracy and noise. 200mV difference between the two grounds can be tolerated without degradation in performance.

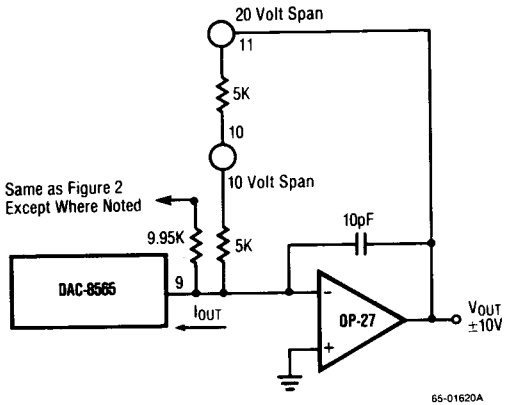


Figure 3. ±10V Bipolar Voltage Output

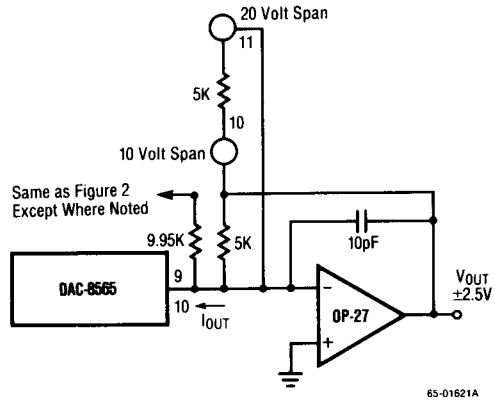


Figure 4. ±2.5V Bipolar Voltage Output

Output Voltage Compliance

The DAC-8565 has a minimum output voltage compliance range of -1.5V to +10V and is independent of both the positive and negative supply voltages. The output can be modeled as a 25pF capacitance shunted by a 10MΩ resistance across the output current source to ground. This is a dramatic improvement over competitive DAC-8565 designs which have an 8kΩ output impedance. The DAC-8565's output current varies insignificantly as a function of output voltage, allowing direct conversion to voltage by an external resistor in many applications.

More significantly, the errors introduced by the input errors of the external output operational amplifier are not magnified by a low output impedance. The output system error from the op amp is equal to:

$$(V_{ERR} \text{ in op amp}) \left(\frac{R_{SPAN} + R_{IN}}{R_{IN}} \right)$$

and defaults to only the inherent input errors of the op amp.

Settling Time

The internally compensated reference amplifier and differential bit switch are optimized for fast settling operation. Worst case settling time occurs when all bits are switched and is specified as 400nS maximum. Note: The settling time specification is for the output current, not for a voltage. When using an external op amp as a current to voltage converter, the settling time will usually be dominated by the speed performance of the operational amplifier. When using the DAC in a successive approximation A/D application, care in the selection of the comparator is critical in determining accuracy and speed. Raytheon recommends the use of the RM4805 comparator to optimize A/D performance. Please refer to the 4805 application notes for further details on speed and accuracy characteristics of successive approximation A/D converters.

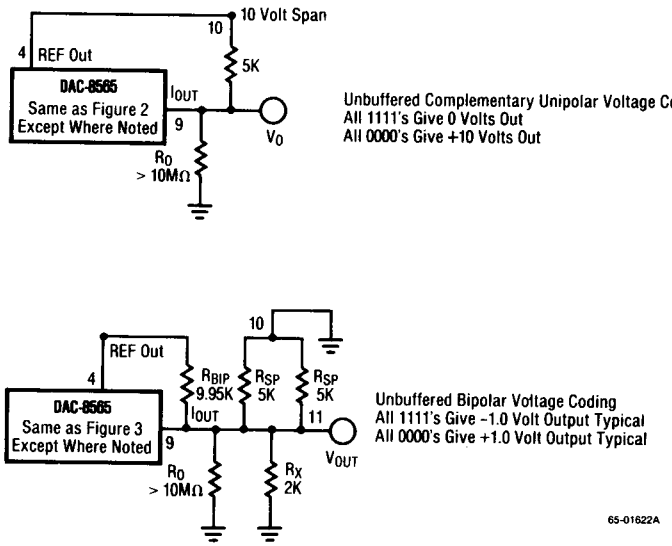
Direct Unbuffered Voltage Output for Cable Driving

The high output impedance and compliance range allow for direct current to voltage conversion using the bipolar and span resistors. The

circuit configurations of Figure 5 yield complementary unipolar coding (+10V to 0V) as well as ±1.0V bipolar coding. The 10MΩ output impedance of the DAC-8565 allows for direct current to voltage conversion without any degradation of linearity performance.

12-Bit Analog-to-Digital Converter

Figure 7 shows an application of the DAC-8565 coupled with the 4805 comparator to make a successive approximation 12-bit analog-to-digital converter. The SAR selected is the AM2504. Latched output capability is provided by the 25LS374. Conversion time with the 1K summing mode resistance should be set by the clock at 13μS.



Note: R_{SPANS} can vary by ±20% max

Figure 5. Unbuffered Voltage Output Configurations

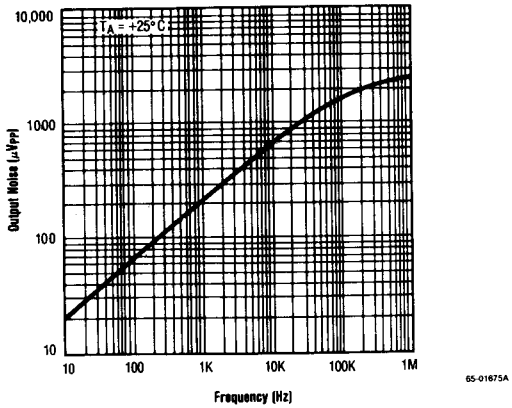


Figure 6. Output Wideband Noise vs Bandwidth (0.1Hz to Frequency Indicated)

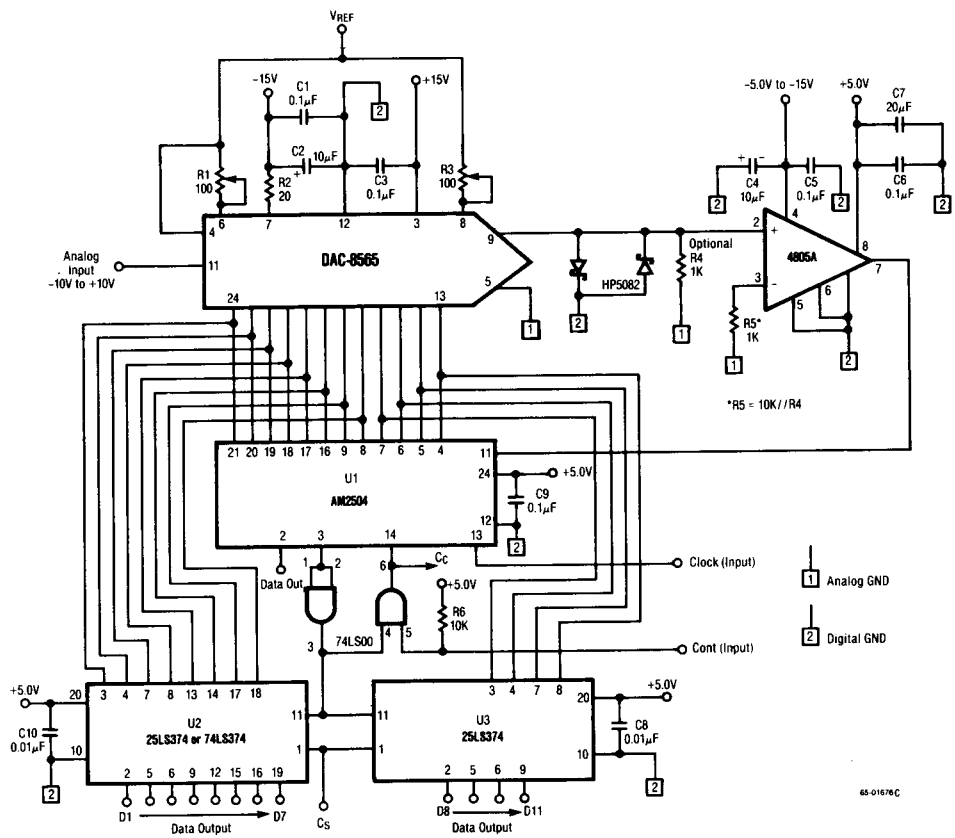


Figure 7. 12-Bit Analog-to-Digital Converter