Integrated Device Technology, Inc.

BiCMOS STATIC RAM 72K (8K x 9-BIT) CACHE-TAG RAM

ADVANCE INFORMATION
IDT71B79

FEATURES:

- High-speed address to MATCH comparison time
  - — Military: 12/15/20ns (max.)
  - — Commercial: 10/12/15ns (max.)
- High-speed address access time
  - — Military: 12/15/20ns (max.)
  - — Commercial: 10/12/15ns (max)
- High-speed asynchronous RAM Clear
- Produced with advanced BiCEMOS™ high-performance technology
- Single 5V (+10%) power supply
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard 28-pin plastic and hermetic DIP (300 mil), 28-pin SOJ

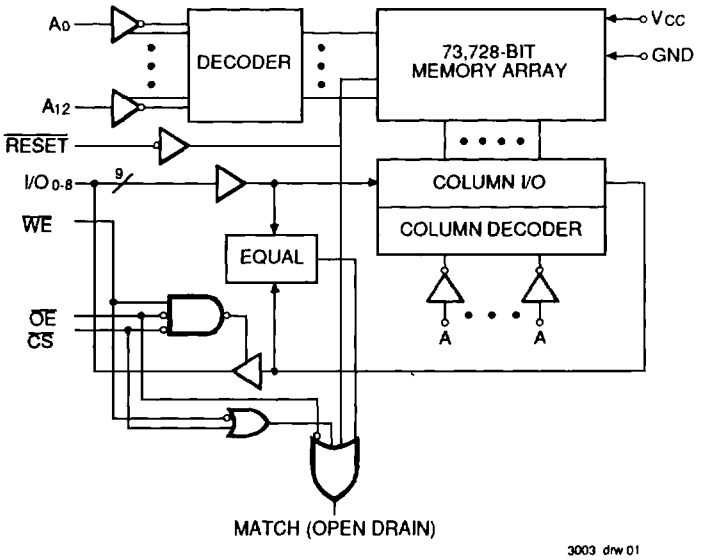
DESCRIPTION:

The IDT71B79 is a high-speed cache address comparator subsystem consisting of a 72K-bit static RAM organized as 8K x 9 and an 9-bit comparator. The IDT71B79 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT71B79 can also be used as an 8K x 9 high-speed static RAM.

The IDT71B79 is fabricated using IDT's high-performance, high-reliability technology — BiCEMOS. Address access times as fast as 10ns and address-to-comparison times of 10ns are available with maximum power consumption of 825mW.

The MATCH pin of several IDT71B79s can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput.

FUNCTIONAL BLOCK DIAGRAM



3003 drw 01

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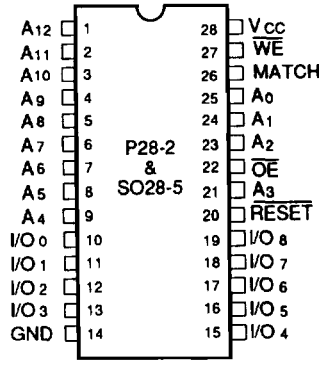
PIN CONFIGURATION



DIP/SOJ
TOP VIEW

3003 drw 02

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