Integrated Circuit Systems, Inc.

ICS95V157
Advance Information

2.5V Wide Range Frequency Clock Driver (33MHz - 233MHz)

Recommended Application:

Single-ended clock input with zero delay board fan out

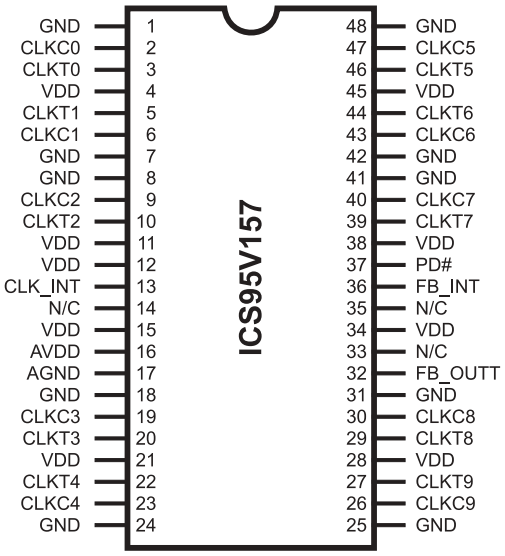
Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution (SSTL2)
- Feedback pin for input to output synchronization
- PD for power management
- Spread Spectrum tolerant inputs

Switching Characteristics:

- CYCLE - CYCLE jitter (>100MHz):<60ps
- OUTPUT - OUTPUT skew: <40ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

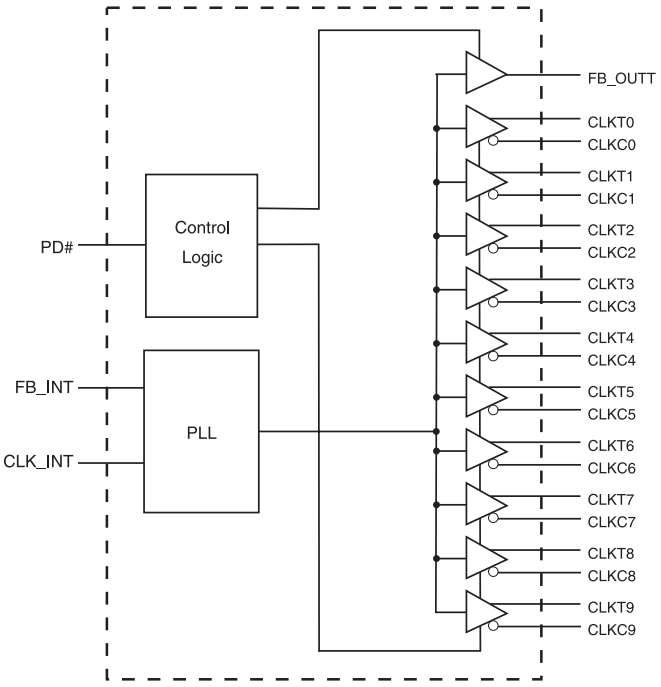
Pin Configuration



48-Pin TSSOP

6.10 mm. Body, 0.50 mm. pitch = TSSOP

Block Diagram



Functionality

INPUTS			OUTPUTS			PLL State
AVDD	PD#	CLK_INT	CLKT	CLKC	FB_OUTT	
GND	H	L	L	H	L	Bypassed/off
GND	H	H	H	L	H	Bypassed/off
2.5V (nom)	L	L	Z	Z	Z	off
2.5V (nom)	L	H	Z	Z	Z	off
2.5V (nom)	H	L	L	H	L	on
2.5V (nom)	H	H	H	L	H	on

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
4, 11, 12, 15, 21, 28, 34, 38, 45,	VDD	PWR	Power supply 2.5V
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	OUT	"True" Clock of differential pair outputs.
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	OUT	"Complementary" clocks of differential pair outputs.
13	CLK_INT	IN	"True" reference clock input
32	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
36	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
14, 33, 35	N/C	-	Not connected
37	PD#	IN	Power Down. LVCMOS input

This PLL Clock Buffer is designed for a V_{DD} of 2.5V, an AV_{DD} of 2.5V and differential data input and output levels.

ICS95V157 is a zero delay buffer that distributes a single-ended clock input (CLK_INT) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one single-ended feedback clock output (FB_OUTT). The clock outputs are controlled by the input clocks (CLK_INT), the feedback clock (FB_INT), the 2.5-V LVCMOS input (PD#) and the analog power input (AV_{DD}). When input (PD#) is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are tri-stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

The PLL in the **ICS95V157** clock driver uses the input clocks (CLK_INT) and the feedback clock (FB_INT) to provide high-performance, low-skew, low-jitter, output differential clocks (CLKT [0:9], CLKC [0:9]). **ICS95V157** is also able to track Spread Spectrum Clock (SSC) for reduced EMI.

ICS95V157 is characterized for operation from 0°C to 85°C.

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 4.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} + 0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	VI = VDD or GND	5			µA
Input Low Current	I_{IL}	VI = VDD or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	CL = 0pf @ 200MHz		260		mA
	I_{DDPD}	CL = 0pf			100	mA
Output High Current	I_{OH}	VDD = 2.3V, V_{OUT} = 1V	TBD	TBD		mA
Output Low Current	I_{OL}	VDD = 2.3V, V_{OUT} = 1.2V	TBD	TBD		mA
High Impedance Output Current	I_{OZ}	VDD = 2.7V, Vout=VDD or GND			±10	mA
Input Clamp Voltage	V_{IK}	VDDQ = 2.3V Iin = -18mA			TBD	V
High-level output voltage	V_{OH}	VDD = min to max, IOH = -1 mA	TBD			V
		VDDQ = 2.3V, IOH = -12 mA	TBD			V
Low-level output voltage	V_{OL}	VDD = min to max I_{OL}=1 mA			TBD	V
		VDDQ = 2.3V IOH=12 mA			TBD	V
Input Capacitance[1]	C_{IN}	VI = GND or VDD		TBD		pF
Output Capacitance[1]	C_{OUT}	VOUT = GND or VDD		TBD		pF

[1]Guaranteed by design at 233MHz, not 100% tested in production.

Recommended Operating Condition (see note1)

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		2.3		2.7	V
Low level input voltage	V_{IL}	CLK_INT			V_{DDQ}/2 - 0.35	V
		PD#	-0.3		0.7	V
High level input voltage	V_{IH}	CLK_INT	V_{DDQ}/2 + 0.35			V
		PD#	1.7		V_{DDQ} + 0.6	V
DC input signal voltage (note 2)			-0.3		V_{DDQ}	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DDQ}/2 - 0.15		V_{DDQ}/2 + 0.15	V
High level output current	I_{OH}				TBD	mA
Low level output current	I_{OL}				TBD	mA
Input slew rate	S_R		1		4	V/ns
Operating free-air temperature	T_A		0		85	°C

Notes:
1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of the input.

Timing Requirements

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$freq_{op}$	2.5V±0.2V @ 25°C	33	233	MHz
Application Frequency Range	$freq_{App}$	2.5V±0.2V @ 25°C	95	170	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}	from VDD = 3.3V to 1% target freq.		100	µs

Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		TBD		ns
High-to low level propagation delay time	t_{PLL}[1]	CLK_IN to any output		TBD		ns
Output enable time	t_{EN}	PD# to any output		TBD		ns
Output disable time	tdis	PD# to any output		TBD		ns
Period jitter	$T_{jit\ (per)}$	100/125/133/167/200MHz	-50		50	ps
Half-period jitter	t(jit_hper)	100/133/167/200MHz	-80		50	
Input clock slew rate	t(sir_I)		1		4	V/ns
Output clock slew rate	t(sl_o)		1		4	V/ns
Cycle to Cycle Jitter[1]	T_{cyc}-T_{cyc}	100/125/133/167/200MHz			60	ps
Phase error	$t_{(phase\ error)}$[4]		TBD		TBD	ps
Output to Output Skew	T_{skew}				40	ps
Pulse skew	T_{skewp}				TBD	ps
Duty cycle	D_C[2]	100MHz to 200MHz	49.5		50.5	%
Rise Time, Fall Time	tr, tf	Load = 120W/16pF	650	800	950	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, were the cycle (t_c) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.

Parameter Measurement Information

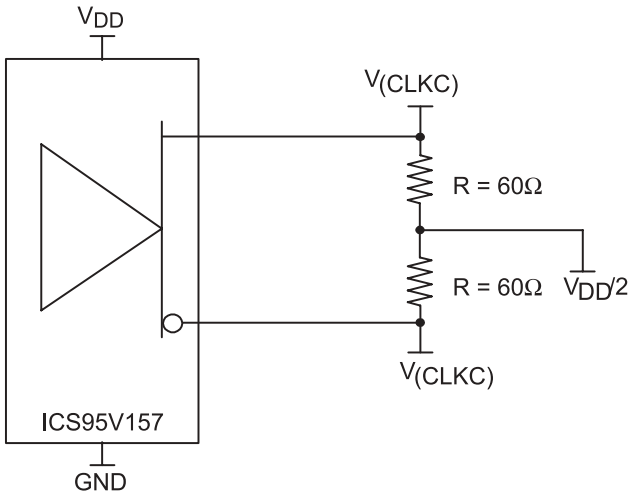
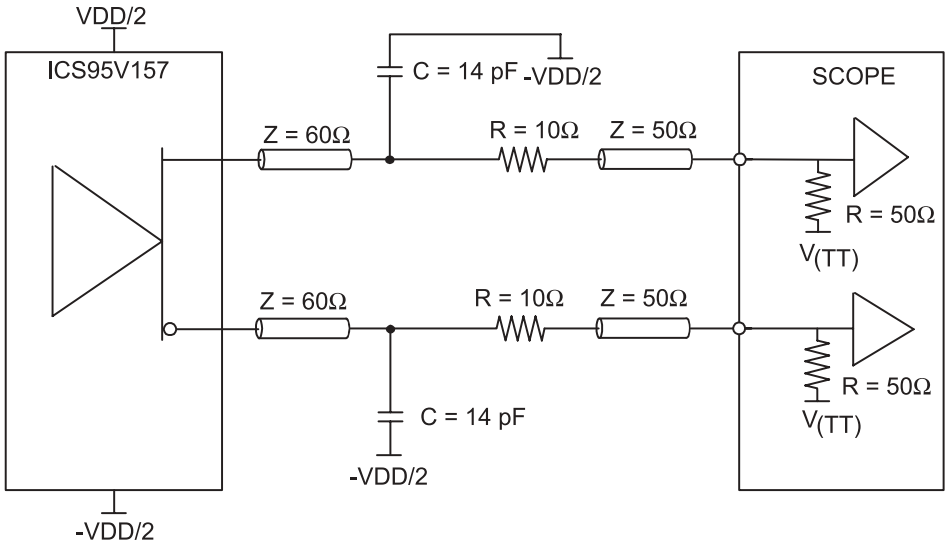
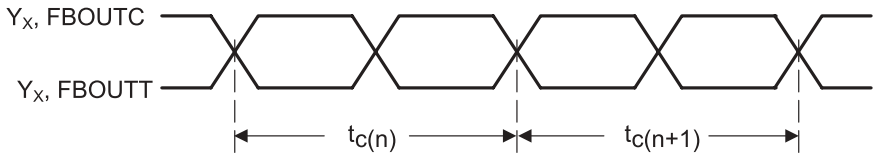


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)}$ = GND

Figure 2. Output Load Test Circuit



$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$

Figure 3. Cycle-to-Cycle Jitter

Parameter Measurement Information

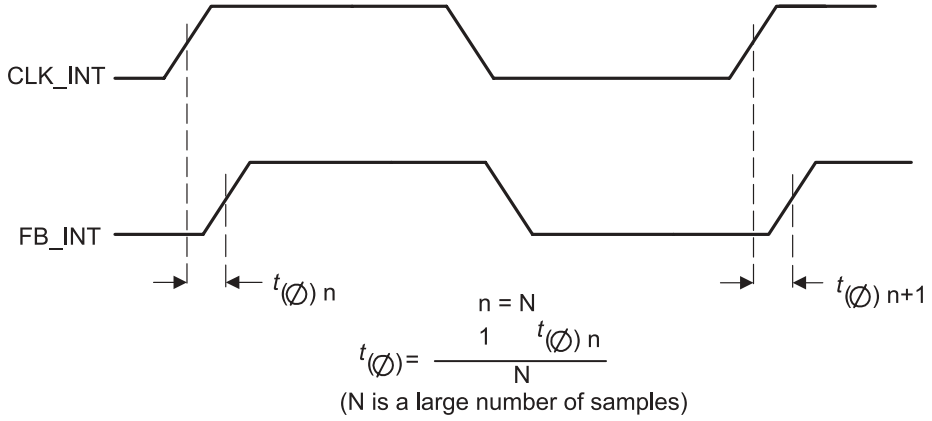


Figure 4. Static Phase Offset

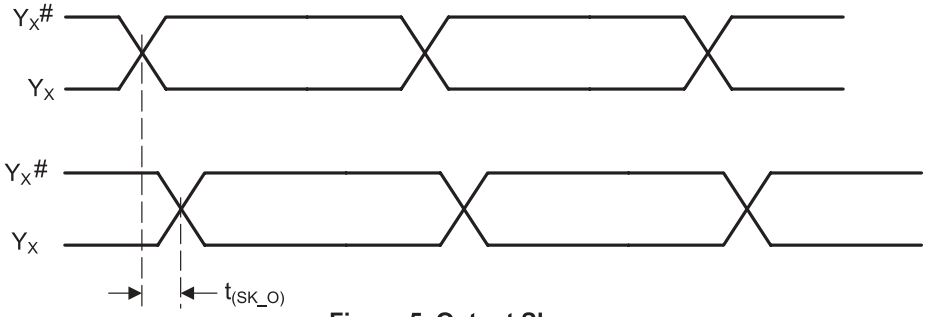


Figure 5. Output Skew

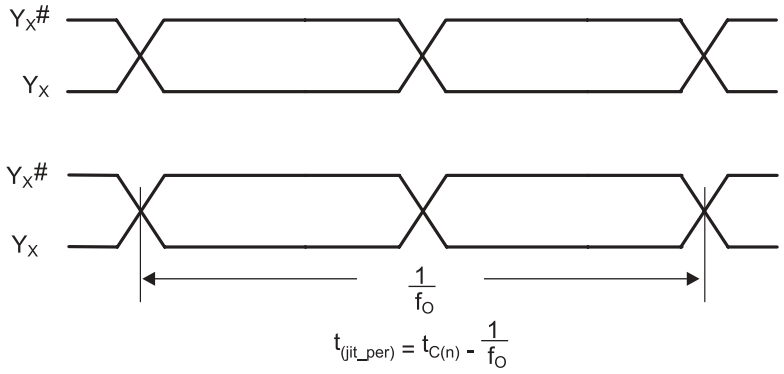


Figure 6. Period Jitter

Parameter Measurement Information

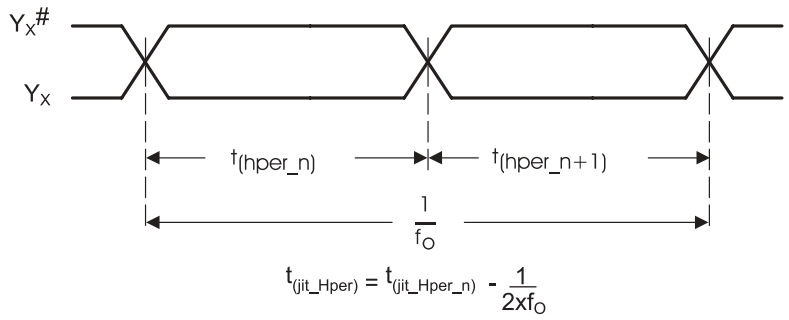
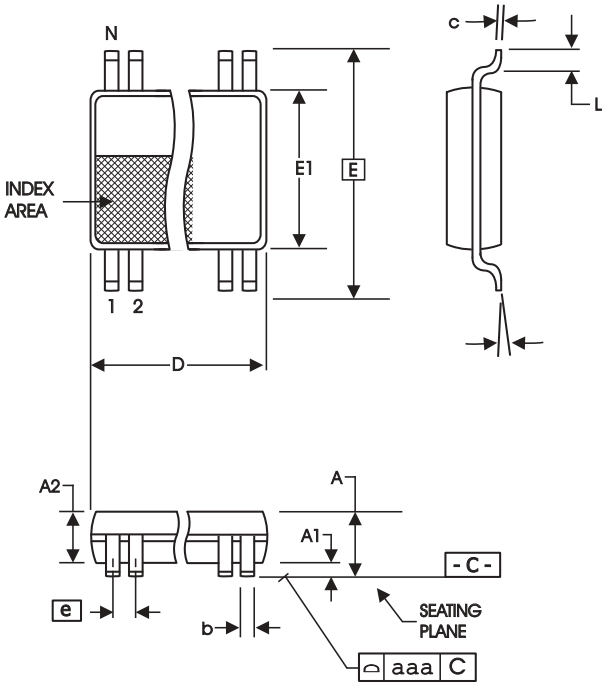


Figure 7. Half-Period Jitter

Figure 8. Input and Output Slew Rates



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (20 mil)

Ordering Information

ICS95V157yG

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0501—08/22/02

95V157A (DDR PLL)

Description
2.5 Single-Ended-to-SSTL_2 Clock Driver (33MHz - 233MHz)
Market Group
DIMM
Additional Info
• Low skew, low jitter PLL clock driver • 1 to 10 differential clock distribution (SSTL_2) • Feedback pin for input to output synchronization • PD# for power management • Spread Spectrum tolerant inputs

Related Orderable Parts

Attributes	95V157AG	95V157AGI	95V157AGIT	95V157AGLF	95V157AGLFT	95V157AGT
Package	TSSOP 48 (PA48)	TSSOP 48 (PA48)	TSSOP 48 (PA48)	TSSOP 48 (PAG48)	TSSOP 48 (PAG48)	TSSOP 48 (PA48)
Speed	NA	NA	NA	NA	NA	NA
Temperature	C	I	I	C	C	C
Voltage	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V
Status	Active	Active	Active	Active	Active	Active
Sample	No	No	No	No	No	No
Minimum Order Quantity	380	190	1000	380	2000	1000
Factory Order Increment	38	38	1000	38	2000	1000

Related Documents

Type	Title	Size	Revision Date
Datasheet	95V157A Datasheet	208 KB	03/27/2006
Product Change Notice	PCN#: TB-0510-05 New Shipping Tube for TSSOP/TVSOP/TSSOP Exposed	202 KB	12/13/2005

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