

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VCXH16373FT

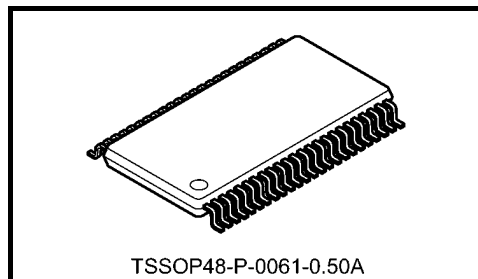
## Low-Voltage 16-Bit D-Type Latch with Bushold

The TC74VCXH16373FT is a high-performance CMOS 16-bit D-type latch. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This 16-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ( $\overline{OE}$ ) which are common to each byte. It can be used as two 8-bit latches or one 16-bit latch. When the  $\overline{OE}$  input is high, the outputs are in a high-impedance state.

The D data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

All inputs are equipped with protection circuits against static discharge.



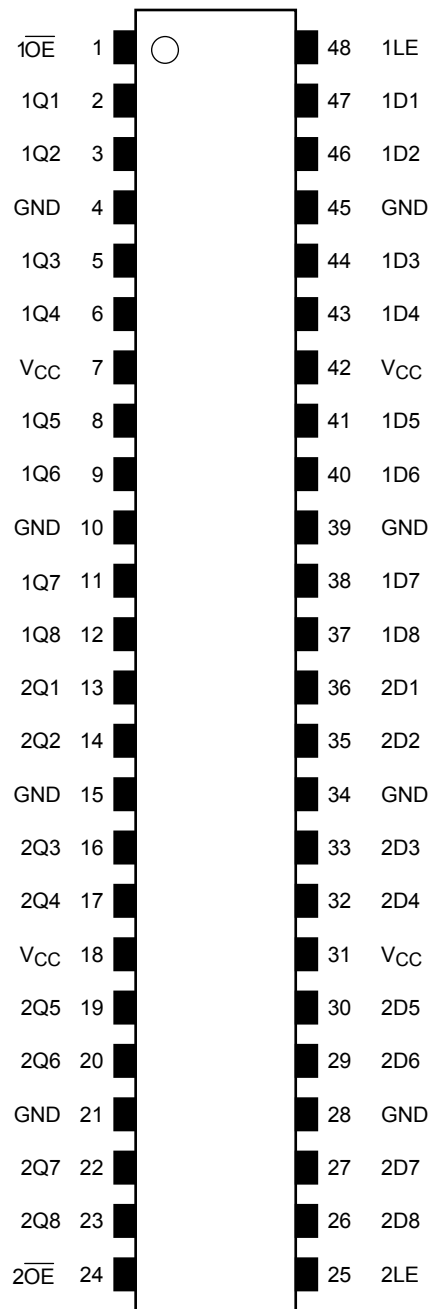
Weight: 0.25g (typ.)

## Features

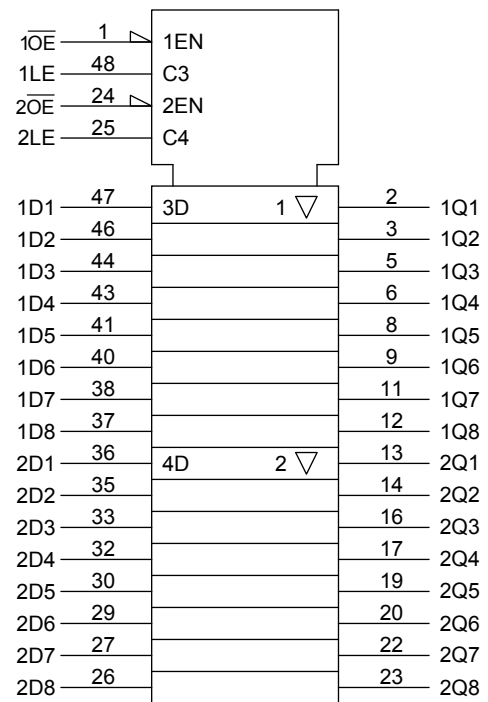
- Low-voltage operation:  $V_{CC} = 1.8$  to  $3.6$  V
- Bushold on data inputs eliminating the need for external pull-up/pull-down resistors
- High-speed operation:  $t_{pd} = 3.0$  ns (max) ( $V_{CC} = 3.0$  to  $3.6$  V)  
:  $t_{pd} = 3.4$  ns (max) ( $V_{CC} = 2.3$  to  $2.7$  V)  
:  $t_{pd} = 5.7$  ns (max) ( $V_{CC} = 1.8$  V)
- Output current:  $I_{OH}/I_{OL} = \pm 24$  mA (min) ( $V_{CC} = 3.0$  V)  
:  $I_{OH}/I_{OL} = \pm 18$  mA (min) ( $V_{CC} = 2.3$  V)  
:  $I_{OH}/I_{OL} = \pm 6$  mA (min) ( $V_{CC} = 1.8$  V)
- Latch-up performance:  $-300$  mA
- ESD performance: Machine model  $\geq \pm 200$  V  
Human body model  $\geq \pm 2000$  V
- Package: TSSOP
- 3.6-V tolerant function and power-down protection control inputs and outputs

Start of commercial production  
2001-07

## Pin Assignment (top view)



## IEC Logic Symbol



## Truth Table

Inputs			Outputs
$\overline{1OE}$	1LE	1D1-1D8	1Q1-1Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

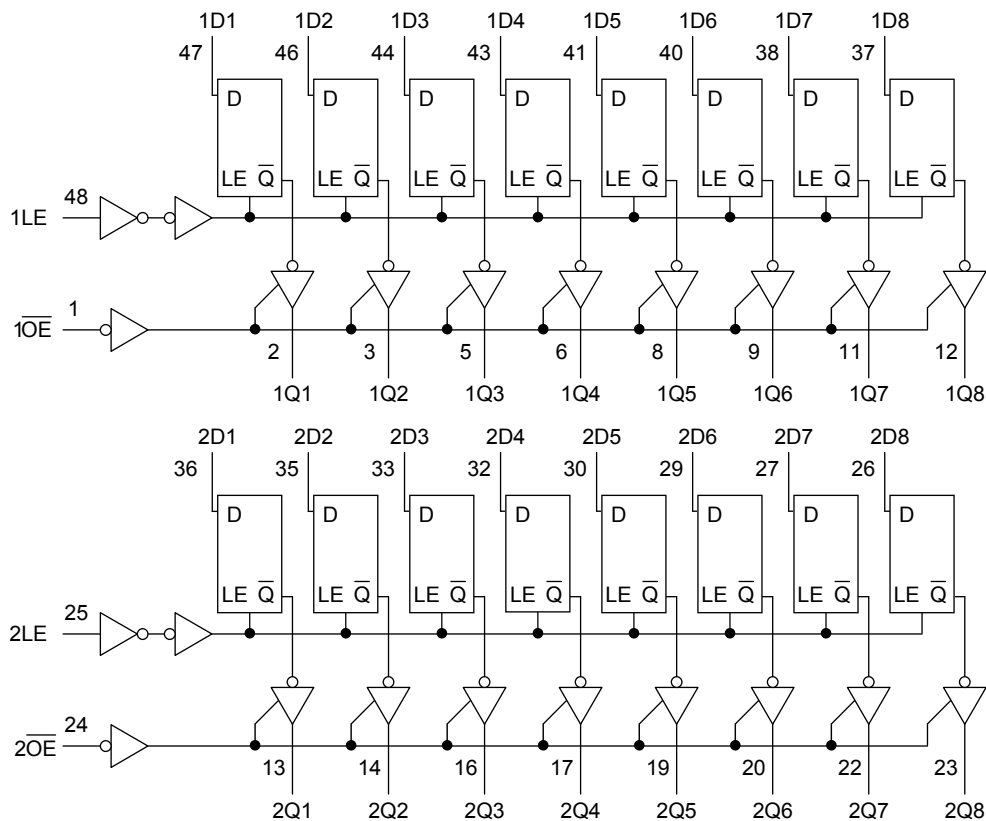
Inputs			Outputs
$\overline{2OE}$	2LE	2D1-2D8	2Q1-2Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	-0.5 to 4.6	V
DC input voltage	( $\overline{OE}$ , LE)	-0.5 to 4.6	V
	(An)	-0.5 to $V_{CC} + 0.5$	
DC output voltage	$V_{OUT}$	-0.5 to 4.6 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	$I_{IK}$	-50	mA
Output diode current	$I_{OK}$	$\pm 50$ (Note 4)	mA
Output current	$I_{OUT}$	$\pm 50$	mA
Power dissipation	$P_D$	400	mW
DC $V_{CC}$ /ground current per supply pin	$I_{CC}/I_{GND}$	$\pm 100$	mA
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: OFF state

Note 3: High or low state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

## Operating Ranges (Note 1) (Note 2)

Characteristics		Symbol	Rating	Unit
Power supply voltage		$V_{CC}$	1.8 to 3.6	V
			1.2 to 3.6 (Note 3)	
Input voltage	( $\overline{OE}$ , LE)	$V_{IN}$	-0.3 to 3.6	V
	(An)		0 to $V_{CC}$	
Output voltage		$V_{OUT}$	0 to 3.6 (Note 4)	V
			0 to $V_{CC}$ (Note 5)	
Output current		$I_{OH}/I_{OL}$	$\pm 24$ (Note 6)	mA
			$\pm 18$ (Note 7)	
			$\pm 6$ (Note 8)	
Operating temperature		$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time		$dt/dv$	0 to 10 (Note 9)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 2: Floating or unused control inputs must be held high or low.

Note 3: Data retention

Note 4: OFF state

Note 5: High or low state

Note 6:  $V_{CC} = 3.0$  to  $3.6$  V

Note 7:  $V_{CC} = 2.3$  to  $2.7$  V

Note 8:  $V_{CC} = 1.8$  V

Note 9:  $V_{IN} = 0.8$  to  $2.0$  V,  $V_{CC} = 3.0$  V

## Electrical Characteristics

### DC Characteristics (Ta = -40 to 85°C, 2.7 V < VCC ≤ 3.6 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>	—		2.7 to 3.6	2.0	—	V
	L-level	V <sub>IL</sub>	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -12 mA	2.7	2.2	—	
				I <sub>OH</sub> = -18 mA	3.0	2.4	—	
				I <sub>OH</sub> = -24 mA	3.0	2.2	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.7 to 3.6	—	0.2	
				I <sub>OL</sub> = 12 mA	2.7	—	0.4	
				I <sub>OL</sub> = 18 mA	3.0	—	0.4	
				I <sub>OL</sub> = 24 mA	3.0	—	0.55	
Input leakage current	( $\overline{OE}$ , LE)	I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
	(An)		V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7 to 3.6	—	±5.0	
Bushold input minimum drive hold current	I <sub>I</sub> (HOLD)	V <sub>IN</sub> = 0.8 V		3.0	75	—	μA	
		V <sub>IN</sub> = 2.0 V		3.0	-75	—		
Bushold input over-drive current to change state	I <sub>I</sub> (OD)	(Note 1)		3.6	—	450	μA	
		(Note 2)		3.6	—	-450		
3-state output OFF state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 3.6 V		2.7 to 3.6	—	±10.0	μA	
Power-off leakage current	I <sub>OFF</sub>	V <sub>OUT</sub> = 0 to 3.6 V		0	—	10.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7 to 3.6	—	20.0	μA	
		V <sub>CC</sub> ≤ V <sub>OUT</sub> ≤ 3.6 V (Note 3)		2.7 to 3.6	—	±20.0		
Increase in I <sub>CC</sub> per input	ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		2.7 to 3.6	—	750	μA	

Note 1: An external driver must source at least the specified current to switch LOW-to-HIGH.

Note 2: An external driver must sink at least the specified current to switch HIGH-to-LOW.

Note 3: Outputs high impedance only.

## DC Characteristics (Ta = -40 to 85°C, 2.3 V ≤ VCC ≤ 2.7 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>	—		2.3 to 2.7	1.6	—	V
	L-level	V <sub>IL</sub>	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.3 to 2.7	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -6 mA	2.3	2.0	—	
				I <sub>OH</sub> = -12 mA	2.3	1.8	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.3 to 2.7	—	0.2	
				I <sub>OL</sub> = 12 mA	2.3	—	0.4	
				I <sub>OL</sub> = 18 mA	2.3	—	0.6	
Input leakage current	( $\overline{OE}$ , LE)	I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V	2.3 to 2.7	—	±5.0	μA	
	(An)		V <sub>IN</sub> = V <sub>CC</sub> or GND	2.3 to 2.7	—	±5.0		
Bushold input minimum drive hold current	I <sub>I</sub> (HOLD)	V <sub>IN</sub> = 0.7 V	2.3	45	—	μA		
		V <sub>IN</sub> = 1.6 V	2.3	-45	—			
Bushold input over-drive current to change state	I <sub>I</sub> (OD)	(Note 1)	2.7	—	300	μA		
		(Note 2)	2.7	—	-300			
3-state output OFF state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 3.6 V	2.3 to 2.7	—	±10.0	μA		
Power-off leakage current	I <sub>OFF</sub>	V <sub>OUT</sub> = 0 to 3.6 V	0	—	10.0	μA		
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	2.3 to 2.7	—	20.0	μA		
		V <sub>CC</sub> ≤ V <sub>OUT</sub> ≤ 3.6 V (Note 3)	2.3 to 2.7	—	±20.0			

Note 1: An external driver must source at least the specified current to switch LOW-to-HIGH.

Note 2: An external driver must sink at least the specified current to switch HIGH-to-LOW.

Note 3: Outputs high impedance only.

## DC Characteristics (Ta = -40 to 85°C, 1.8 V ≤ VCC < 2.3 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>	—		1.8 to 2.3	0.7 × V <sub>CC</sub>	—	V
	L-level	V <sub>IL</sub>	—		1.8 to 2.3	—	0.2 × V <sub>CC</sub>	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	1.8	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -6 mA	1.8	1.4	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	1.8	—	0.2	
				I <sub>OL</sub> = 6 mA	1.8	—	0.3	
Input leakage current	( $\overline{OE}$ , LE)	I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V		1.8	—	±5.0	μA
	(An)		V <sub>IN</sub> = V <sub>CC</sub> or GND		1.8	—	±5.0	
Bushold input minimum drive hold current	I <sub>I</sub> (HOLD)	V <sub>IN</sub> = 0.36 V		1.8	25	—	μA	
		V <sub>IN</sub> = 1.26 V		1.8	-25	—		
Bushold input over-drive current to change state	I <sub>I</sub> (OD)	(Note 1)		1.8	—	200	μA	
		(Note 2)		1.8	—	-200		
3-state output OFF state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 3.6 V		1.8	—	±10.0	μA	
Power-off leakage current	I <sub>OFF</sub>	V <sub>OUT</sub> = 0 to 3.6 V		0	—	10.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		1.8	—	20.0	μA	
		V <sub>CC</sub> ≤ V <sub>OUT</sub> ≤ 3.6 V (Note 3)		1.8	—	±20.0		

Note 1: An external driver must source at least the specified current to switch LOW-to-HIGH.

Note 2: An external driver must sink at least the specified current to switch HIGH-to-LOW.

Note 3: Outputs high impedance only.



## AC Characteristics (Ta = -40 to 85°C, input: tr = tf = 2.0 ns, CL = 30 pF, RL = 500 Ω) (Note 1)

Characteristics	Symbol	Test Condition	VCC (V)	Min	Max	Unit
Propagation delay time (D-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1, Figure 2	1.8	1.5	5.7	ns
			2.5 ± 0.2	1.0	3.4	
			3.3 ± 0.3	0.8	3.0	
Propagation delay time (LE-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1, Figure 2	1.8	1.5	6.0	ns
			2.5 ± 0.2	1.0	3.9	
			3.3 ± 0.3	0.8	3.0	
3-state output enable time	t <sub>pZL</sub> t <sub>pZH</sub>	Figure 1, Figure 3	1.8	1.5	7.0	ns
			2.5 ± 0.2	1.0	4.6	
			3.3 ± 0.3	0.8	3.5	
3-state output disable time	t <sub>pLZ</sub> t <sub>pHZ</sub>	Figure 1, Figure 3	1.8	1.5	5.0	ns
			2.5 ± 0.2	1.0	3.8	
			3.3 ± 0.3	0.8	3.5	
Minimum pulse width (LE)	t <sub>w (H)</sub>	Figure 1, Figure 2	1.8	3.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum set-up time	t <sub>s</sub>	Figure 1, Figure 2	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time	t <sub>h</sub>	Figure 1, Figure 2	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to output skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 2)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: For C<sub>L</sub> = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design.

(t<sub>osLH</sub> = |t<sub>pLHm</sub> - t<sub>pLHn</sub>|, t<sub>osHL</sub> = |t<sub>pHLm</sub> - t<sub>pHLn</sub>|)

## Dynamic Switching Characteristics (Ta = 25°C, input: tr = tf = 2.0 ns, CL = 30 pF)

Characteristics	Symbol	Test Condition	VCC (V)	Typ.	Unit
Quiet output maximum dynamic VOL	VOLP	VIH = 1.8 V, VIL = 0 V (Note)	1.8	0.25	V
		VIH = 2.5 V, VIL = 0 V (Note)	2.5	0.6	
		VIH = 3.3 V, VIL = 0 V (Note)	3.3	0.8	
Quiet output minimum dynamic VOL	VOLV	VIH = 1.8 V, VIL = 0 V (Note)	1.8	-0.25	V
		VIH = 2.5 V, VIL = 0 V (Note)	2.5	-0.6	
		VIH = 3.3 V, VIL = 0 V (Note)	3.3	-0.8	
Quiet output minimum dynamic VOH	VOHV	VIH = 1.8 V, VIL = 0 V (Note)	1.8	1.5	V
		VIH = 2.5 V, VIL = 0 V (Note)	2.5	1.9	
		VIH = 3.3 V, VIL = 0 V (Note)	3.3	2.2	

Note: Parameter guaranteed by design.

## Capacitive Characteristics (Ta = 25°C)

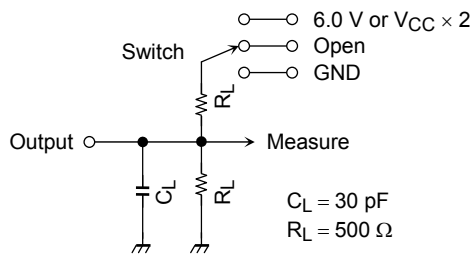
Characteristics	Symbol	Test Condition	VCC (V)	Typ.	Unit
Input capacitance	CIN	—	1.8, 2.5, 3.3	6	pF
Output capacitance	CO	—	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	CPD	fIN = 10 MHz (Note)	1.8, 2.5, 3.3	20	pF

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$$

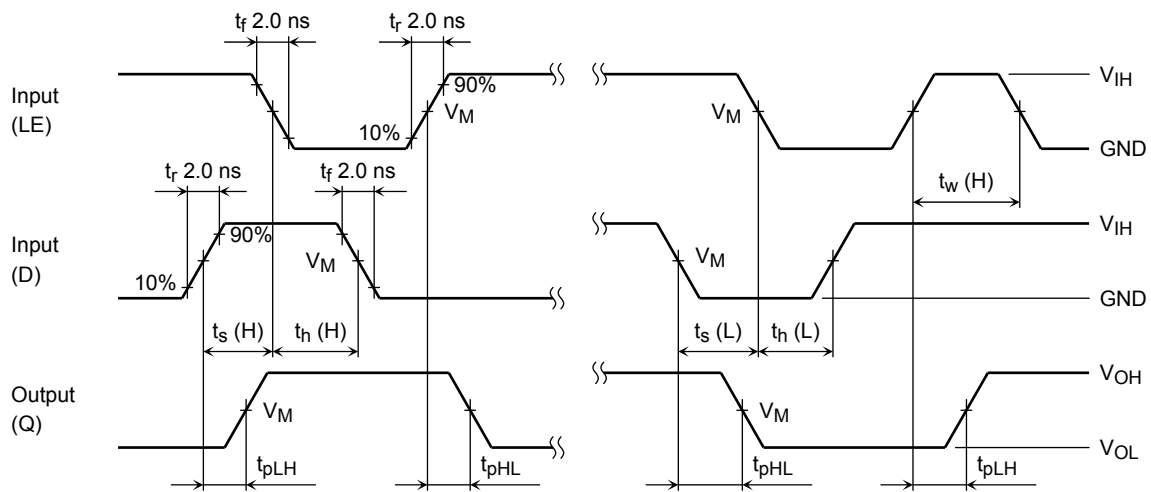
**AC Test Circuit**



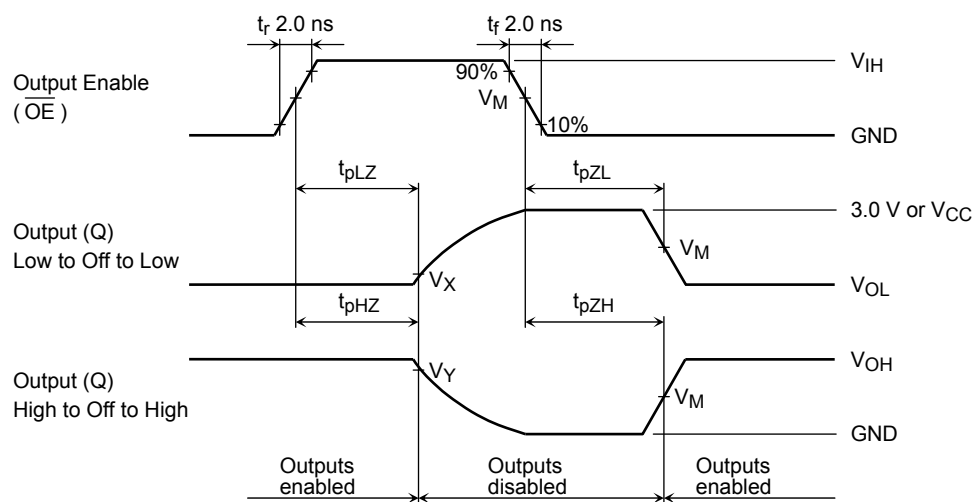
Parameter	Switch
$t_{pLH}$ , $t_{pHL}$	Open
$t_{pLZ}$ , $t_{pZL}$	6.0 V $V_{CC} \times 2$
	@ $V_{CC} = 3.3 \pm 0.3 \text{ V}$ @ $V_{CC} = 2.5 \pm 0.2 \text{ V}$ @ $V_{CC} = 1.8 \text{ V}$
$t_{pHZ}$ , $t_{pZH}$	GND

**Figure 1**

**AC Waveform**



**Figure 2**  $t_{pLH}$ ,  $t_{pHL}$ ,  $t_w$ ,  $t_s$ ,  $t_h$



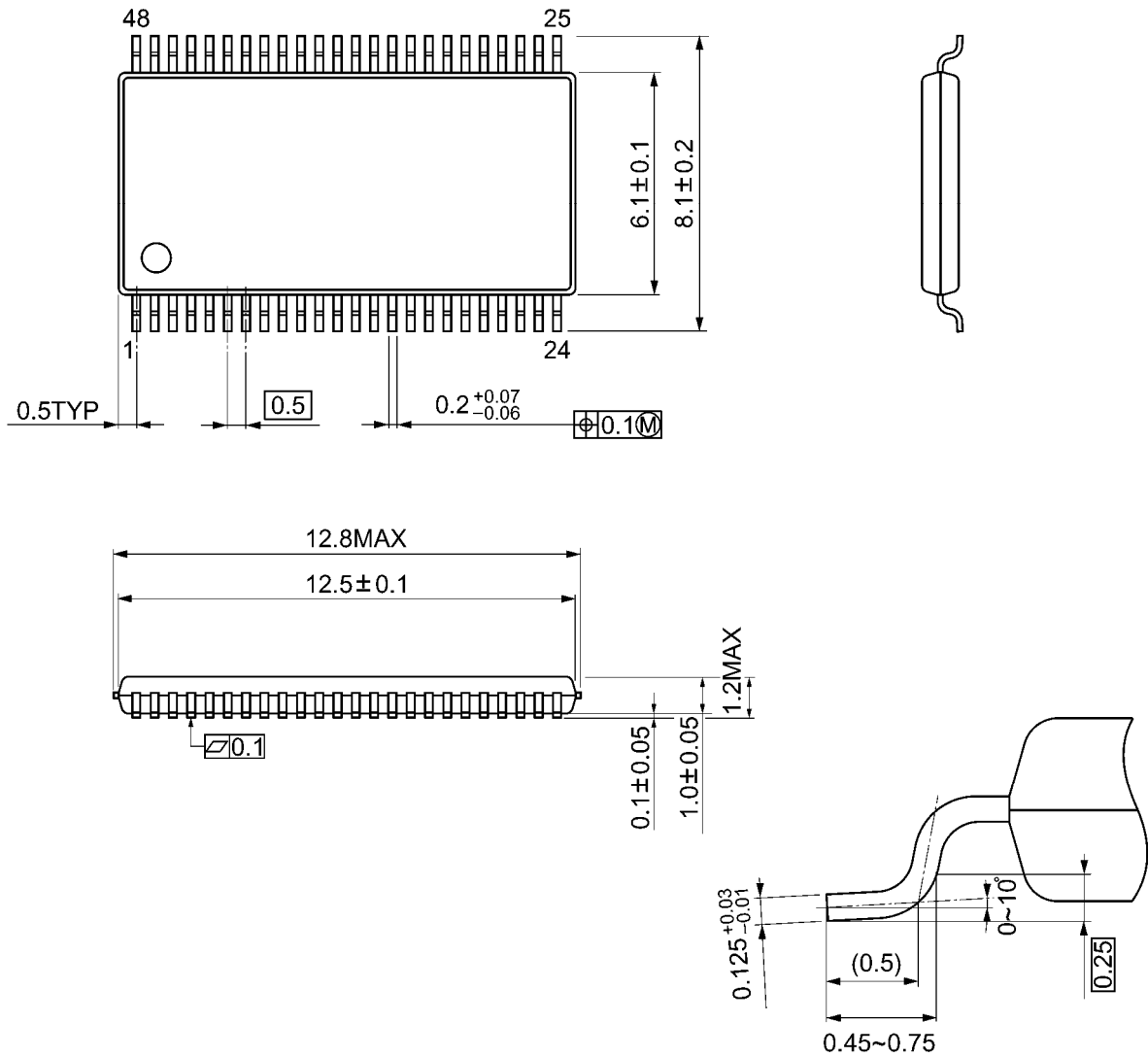
**Figure 3**  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$

Symbol	$V_{CC}$		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	$1.8 \text{ V}$
$V_{IH}$	$2.7 \text{ V}$	$V_{CC}$	$V_{CC}$
$V_M$	$1.5 \text{ V}$	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
$V_Y$	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

**Package Dimensions**

TSSOP48-P-0061-0.50A

Unit: mm



Weight: 0.25 g (typ.)

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