

Advance Information

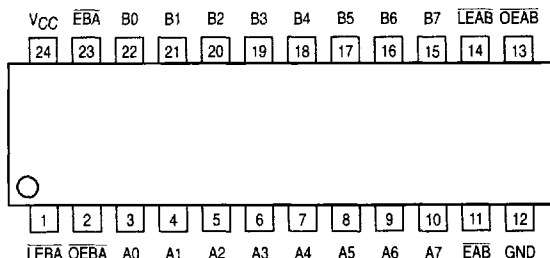
Low-Voltage CMOS Octal Latching Transceiver With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX543 is a high performance, non-inverting octal latching transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX543 inputs to be safely driven from 5V devices. The MC74LCX543 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

For data flow from A to B with the $\bar{E}A\bar{B}$ LOW, the A-to-B Output Enable ($\bar{O}EAB$) must be LOW in order to enable data to the B bus, as indicated in the Function Table. With $\bar{E}A\bar{B}$ LOW, a LOW signal on the A-to-B Latch Enable ($\bar{L}EAB$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\bar{L}EAB$ signal will latch the A latches, and the outputs no longer change with the A inputs. With $\bar{E}A\bar{B}$ and $\bar{O}EAB$ both LOW, the 3-State B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is symmetric to that above, but uses the EBA , $\bar{L}EBA$, and $\bar{O}EBA$ inputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- IOFF Specification Guarantees High Impedance When $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

Pinout: 24-Lead Package (Top View)



MC74LCX543

LCX

**LOW-VOLTAGE CMOS
OCTAL LATCHING
TRANSCEIVER**

DW SUFFIX
PLASTIC SOIC
CASE 751E-04

SD SUFFIX
PLASTIC SSOP
CASE 940D-03

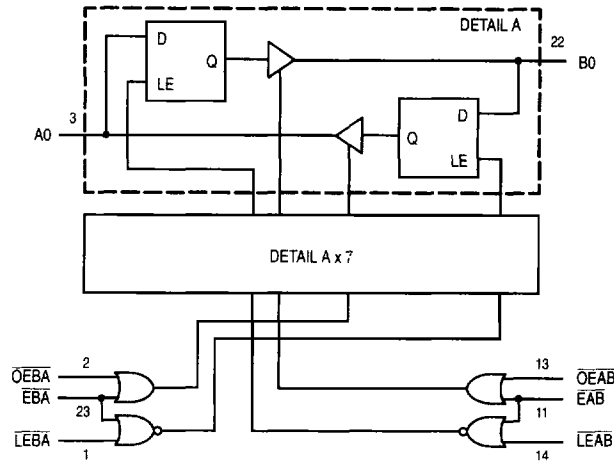
DT SUFFIX
PLASTIC TSSOP
CASE 948H-01

PIN NAMES

Pins	Function
$\bar{O}E_{xx}$	Output Enable Inputs
\bar{E}_{xx}	Enable Inputs
$\bar{L}E_{xx}$	Latch Enable Inputs
A0-A7	3-State Inputs/Outputs
B0-B7	3-State Inputs/Outputs

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM



FUNCTION TABLE

Inputs						Data Ports		Operating Mode		
OEAB	OEBA	EAB	EBA	LEAB	LEBA	An	Bn			
H	H					Input	Input			
		X	X	X	X	X	X	Disable Outputs		
		L	L	L	L	L	L	X	X	Transparent Data; Outputs Disabled
H	H			l	h	l	h	Latch and Outputs Disabled		
L	H	H	X*	L	X	l	Z	Z	Load and B Outputs Disabled	
				H	X	X	Z	Z	Hold; B Outputs Disabled	
		L	X*	L	X	L	H	L	H	Transparent A to B
				H	X	l	H	L	H	Latch and Display B Outputs
H	L	X*	H	X	L	Z	l	h	Load and A Outputs Disabled	
				X	H	Z	X	X	Hold; A Outputs Disabled	
		X*	L	X	L	L	H	L	H	Transparent B to A
				X	H	L	l	h	L	h

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; X = Don't Care; * = The latches are not internally gated with the Output Enables. Therefore, data at the A or B ports may enter the latches at any time, provided that the LExx and Exx pins are set accordingly. For I_{CC} reasons, Do Not Float Inputs.

MC74LCX543

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0		V
V _I	DC Input Voltage	-0.5 ≤ V _I ≤ +7.0		V
V _O	DC Output Voltage	-0.5 ≤ V _O ≤ +7.0	Output in 3-State	V
		-0.5 ≤ V _O ≤ V _{CC} + 0.5	Note 1.	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	Operating	2.0	3.3	3.6	V
		Data Retention Only	1.5	3.3	3.6	
V _I	Input Voltage	0		5.5	V	
V _O	Output Voltage (HIGH or LOW State) (3-State)	0		V _{CC}	V	
		0		5.5		
I _{OH}	HIGH Level Output Current, V _{CC} = 3.0V – 3.6V			-24	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 3.0V – 3.6V			24	mA	
I _{OH}	HIGH Level Output Current, V _{CC} = 2.7V – 3.0V			-12	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 2.7V – 3.0V			12	mA	
T _A	Operating Free-Air Temperature	-40		+85	°C	
Δt/ΔV	Input Transition Rise or Fall Rate, V _I from 0.8V to 2.0V. V _{CC} = 3.0V	0		10	ns/V	

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V _{CC} ≤ 3.6V	2.0		V
V _{IL}	LOW Level Input Voltage (Note 2.)	2.7V ≤ V _{CC} ≤ 3.6V		0.8	V
V _{OH}	HIGH Level Output Voltage	2.7V ≤ V _{CC} ≤ 3.6V; I _{OH} = -100μA	V _{CC} - 0.2		V
		V _{CC} = 2.7V; I _{OH} = -12mA	2.2		
		V _{CC} = 3.0V; I _{OH} = -18mA	2.4		
		V _{CC} = 3.0V; I _{OH} = -24mA	2.2		
V _{OL}	LOW Level Output Voltage	2.7V ≤ V _{CC} ≤ 3.6V; I _{OL} = 100μA		0.2	V
		V _{CC} = 2.7V; I _{OL} = 12mA		0.4	
		V _{CC} = 3.0V; I _{OL} = 16mA		0.4	
		V _{CC} = 3.0V; I _{OL} = 24mA		0.55	

2. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
I _I	Input Leakage Current	2.7V ≤ V _{CC} ≤ 3.6V; 0V ≤ V _I ≤ 5.5V		±5.0	μA
I _{OZ}	3-State Output Current	2.7 ≤ V _{CC} ≤ 3.6V; 0V ≤ V _O ≤ 5.5V; V _I = V _{IH} or V _{IL}		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _{CC} = 0V; V _I or V _O = 5.5V		10	μA
I _{CC}	Quiescent Supply Current	2.7 ≤ V _{CC} ≤ 3.6V; V _I = GND or V _{CC}		10	μA
		2.7 ≤ V _{CC} ≤ 3.6V; 3.6 ≤ V _I or V _O ≤ 5.5V		±10	μA
ΔI _{CC}	Increase in I _{CC} per Input	2.7 ≤ V _{CC} ≤ 3.6V; V _{IH} = V _{CC} - 0.6V		500	μA

AC CHARACTERISTICS (Note 3.; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T _A = -40°C to +85°C				
			V _{CC} = 3.0V to 3.6V		V _{CC} = 2.7V		
			Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay An to Bn or Bn to An	1	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to An or LEAB to Bn	4	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t _{PZH} t _{PZL}	Output Enable Time OEBA to An or OEAB to Bn	2	1.5 1.5	9.0 9.0	1.5 1.5	10.0 10.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time OEBA to An or OEAB to Bn	2	1.5 1.5	7.0 7.0	1.5 1.5	7.5 7.5	ns
t _{PZH} t _{PZL}	Output Enable Time EBA to An or EAB to Bn	2	1.5 1.5	9.0 9.0	1.5 1.5	10.0 10.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time EBA to An or EAB to Bn	2	1.5 1.5	7.0 7.0	1.5 1.5	7.5 7.5	ns
t _s	Setup Time, HIGH to LOW Data to \overline{LE}_{xx}	4	2.5		2.5		ns
t _h	Hold Time, HIGH to LOW Data to \overline{LE}_{xx}	4	1.5		1.5		ns
t _s	Setup Time, HIGH to LOW Data to \overline{E}_{xx}	4	2.5		2.5		ns
t _h	Hold Time, HIGH to LOW Data to \overline{E}_{xx}	4	1.5		1.5		ns
t _w	Latch Enable or Enable Pulse Width, LOW	4	3.3		3.3		ns
t _{OSSL} t _{OSLH}	Output-to-Output Skew (Note 4.)			1.0 1.0			ns

3. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

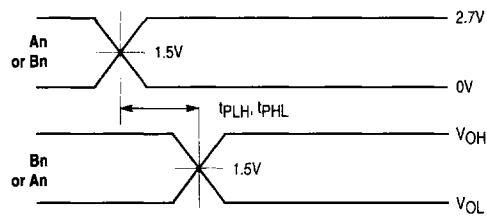
Symbol	Characteristic	Condition	T _A = +25°C			Unit
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 5.)	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V		0.8		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 5.)	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V		0.8		V

5. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

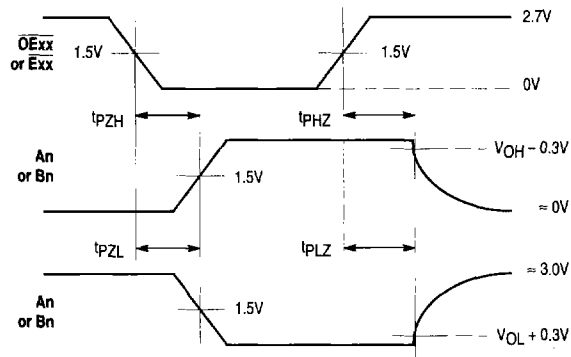
MC74LCX543

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	25	pF

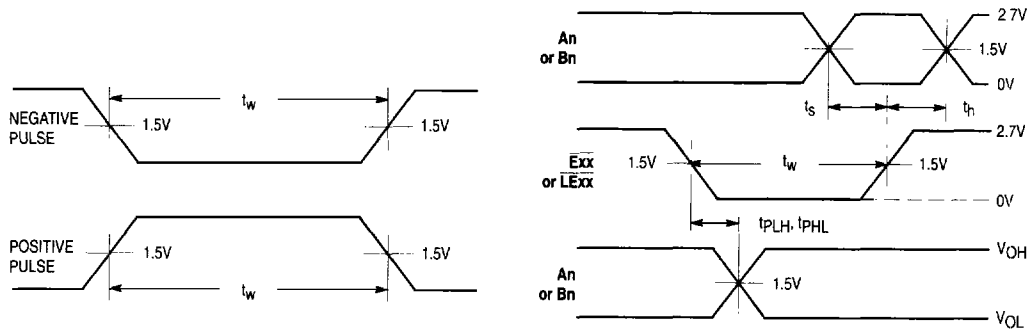


WAVEFORM 1 – A/B to B/A PROPAGATION DELAYS
 $t_R = t_F = 2.5ns, 10\% \text{ to } 90\%; f = 1MHz; t_W = 500ns$



WAVEFORM 2 – $\overline{OE_{xx}}$ / \overline{Exx} to A or B OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.5ns, 10\% \text{ to } 90\%; f = 1MHz; t_W = 500ns$

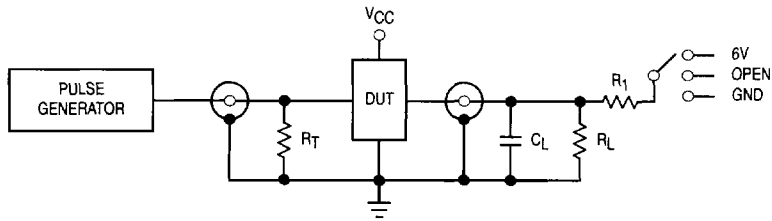
Figure 1. AC Waveforms



WAVEFORM 3 – INPUT PULSE DEFINITION
 $t_R = t_F = 2.5\text{ns}$, 10% to 90% of 0V to 2.7V

WAVEFORM 4 – Enable to A or B PROPAGATION DELAYS, Enable MINIMUM PULSE WIDTH, A or B to Enable SETUP AND HOLD TIMES
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$ except when noted

Figure 2. AC Waveforms (continued)



TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH} , t_{PHZ}	GND

$C_L = 50\text{pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 3. Test Circuit