

OKI semiconductor

MSM51257BLL

32,768-Word x 8-Bit CMOS STATIC RAM

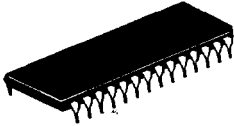
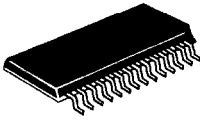

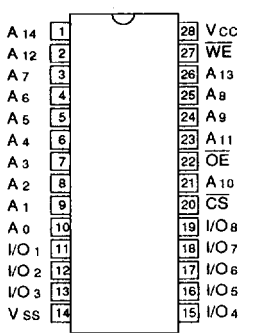
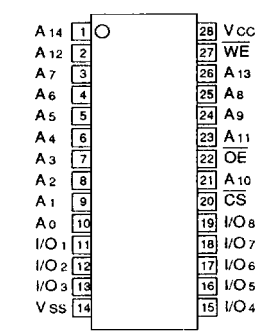
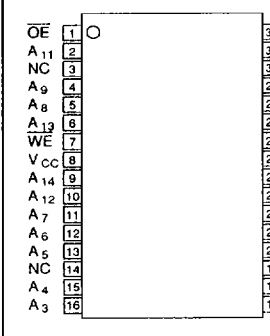
GENERAL DESCRIPTION

The MSM51257BLLRS/GS/TS is a 32768-word by 8-bit CMOS RAM static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device easy to use. The MSM51257BLLRS/GS/TS is also a CMOS silicon gate device that requires very low power during standby (standby current of 20 μ A) when there is no chip selection. The pins \overline{CS} and \overline{OE} are provided as control signals which permit the outputs to be tri-stated, allowing easy memory expansion on system bus.

FEATURES

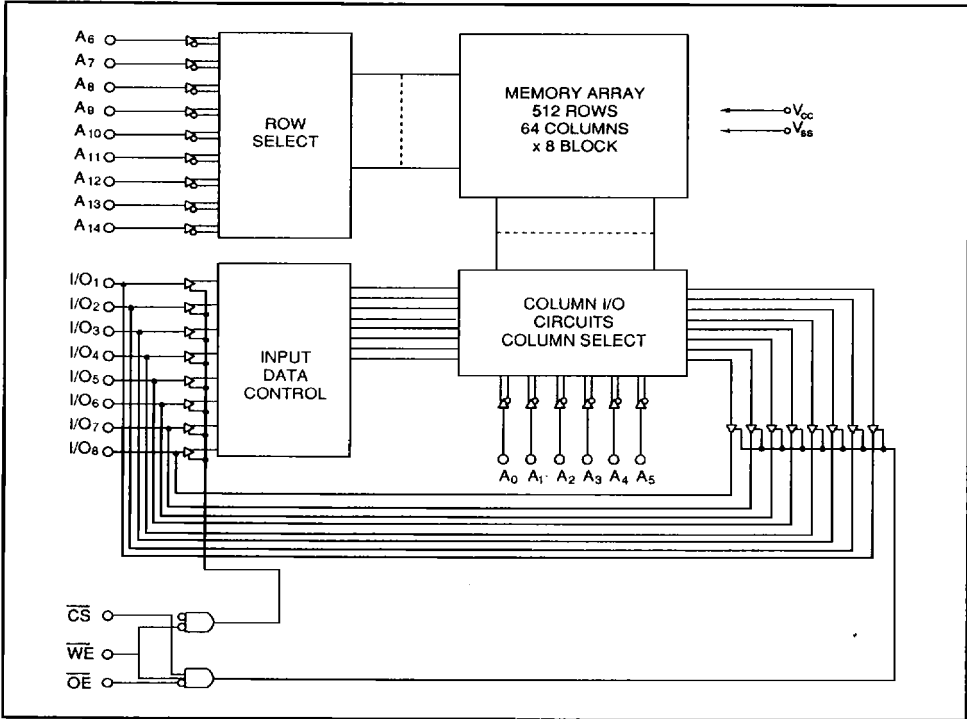
- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
 - Standby: 0.11 mW MAX
 - Operation: 385 mW MAX
- High Speed (Equal Access and Cycle Time)
 - 85-120 ns MAX
- Direct TTL Compatible (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 28-pin FLAT PKG
- 32-pin THIN FLAT PKG

PIN CONFIGURATION (TOP VIEW)

MSM51257BLLRS	MSM51257BLLGS	MSM51257BLLTS
		
		

Pin Names	Function
$A_0 \sim A_{14}$	Address input
$I/O_1 \sim I/O_8$	Data input/output
\overline{CS}	Chip select
NC	No connect
\overline{WE}	Write enable
\overline{OE}	Output enable
V_{cc}, V_{ss}	Supply voltage

BLOCK DIAGRAM



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FUNCTION TABLE

Operating Mode	\overline{CS}	\overline{WE}	\overline{OE}	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D _{OUT}
Write	L	L	X	D _{IN}

X: H or L

**ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Conditions	Value	Unit
Supply Voltage	V _{CC}	Respect to GND	-0.3~7.0	V
Input Voltage	V _{IN}		-0.3*~V _{CC} +0.3	V
Operating Temperature	T _{opr}	—————	0~70	°C
Storage Temperature	T _{slg}	—————	-55~150	°C
Power Dissipation	P _D	T _a = 25°C	1.0	W

* Pulse width < 30 ns: -3.0V MIN

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V _{CC}	5V ± 10%	4.5	5	5.5	V
	V _{SS}	—————	—	0	—	V
Data Retention Voltage	V _{CCH}	—————	2	5	5.5	V
Input Voltage	V _{IH}	5V ± 10%	2.2	—	V _{CC} +0.3	V
	V _{IL}		-0.3*	—	0.8	V
Output Voltage	C _L	—————	—	—	100	pF
	TTL		—	—	1	

* Pulse width < 30 ns: -3.0V MIN

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

Rating	Symbol	Conditions	MSM51257BLL			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I _{LI}	V _{IN} = 0~V _{CC}	-1	—	1	μA
Output Leakage Current	I _{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ V _{IO} =0~V _{CC}	-1	—	1	μA
Output Voltage	V _{OH}	I _{OH} = -1mA	2.4	—	—	V
	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	V
Standby Supply Current	I _{CCS}	$\overline{CS} \geq V_{CC} - 0.2 V$ V _{IN} = 0~V _{CC}	—	—	20*	μA
	I _{CCS1}	$\overline{CS} = V_{IH}$	—	—	3	mA
Operating Supply Current	I _{CCA}	Min cycle, I _{OUT} = 0mA	—	—	70	mA
		f=1 MHz, I _{OUT} = 0mA V _{IH} = V _{CC} , V _{IL} = GND	—	—	15	

* T_a = 0 to 40°C : 6 μA MAX

AC CHARACTERISTICS

Timing conditions

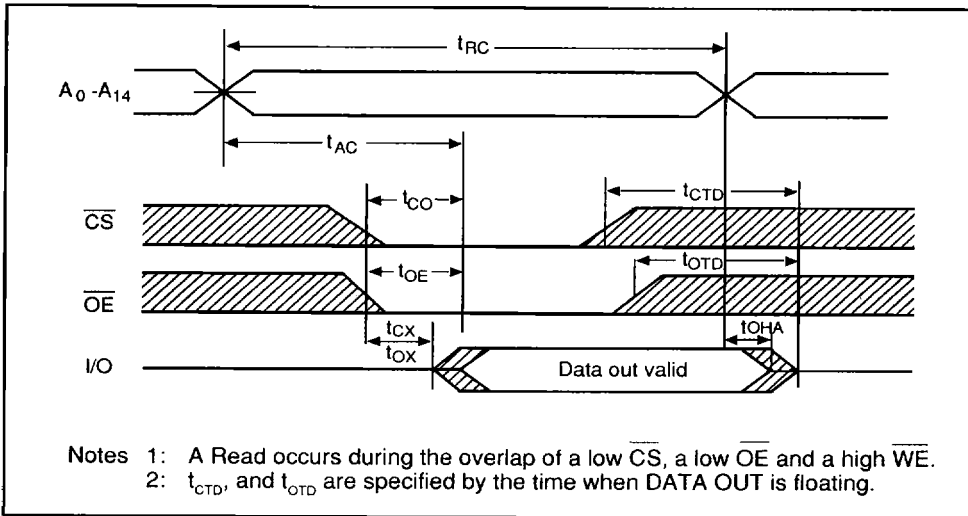
Rating	Conditions
Input Pulse Level	V _{IH} = 2.4V, V _{IL} = 0.6V
Input Rise and Fall Times	5 ns
I/O Timing Level Reference Level	1.5V
Output Load	C _L = 100pF, 1TTL Gate

READ CYCLE

(V_{CC} = 5 V ±10%, T_a = 0 ~ +70°C)

Rating	Symbol	MSM51257BLL-85		MSM51257BLL-10		MSM51257BLL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t _{RC}	85	—	100	—	120	—	ns
Address Access Time	t _{AC}	—	85	—	100	—	120	ns
Chip Enable Access Time	t _{CO}	—	85	—	100	—	120	ns
Output Enable to Output Valid	t _{OE}	—	45	—	50	—	60	ns
Chip Selection to Output Active	t _{CX}	10	—	10	—	10	—	ns
Output Hold Time from Address Change	t _{OHA}	5	—	10	—	10	—	ns
Output 3-State from Output Disable	t _{OTD}	—	30	—	35	—	35	ns
Output 3-State from Chip Deselection	t _{CTD}	—	30	—	35	—	35	ns
Output Enable to Output Active	t _{OX}	5	—	5	—	5	—	ns

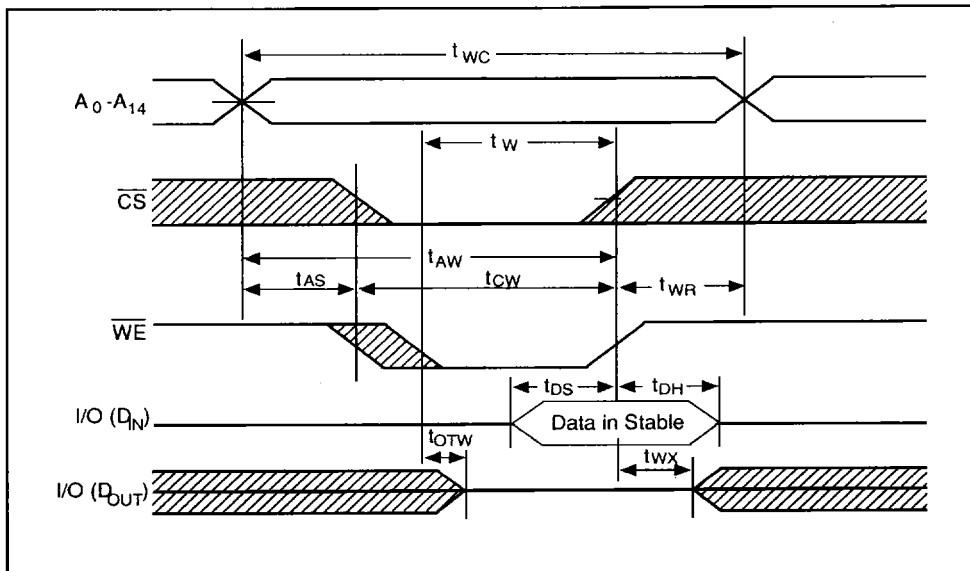
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WRITE CYCLE

(V_{CC} = 5 V ±10%, T_a = 0 ~ +70°C)

Rating	Symbol	MSM51257BLL-85		MSM51257BLL-10		MSM51257BLL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t _{wc}	85	—	100	—	120	—	ns
Address to Write Setup Time	t _{AS}	0	—	0	—	0	—	ns
Write Time	t _w	70	—	75	—	90	—	ns
Write Recovery Time	t _{wr}	5	—	5	—	5	—	ns
Data Setup Time	t _{DS}	40	—	40	—	50	—	ns
Data Hold from Write Time	t _{DH}	0	—	0	—	0	—	ns
Output 3-State from Write	t _{OTW}	0	30	0	35	0	35	ns
Chip Selection to End of Write	t _{CW}	75	—	90	—	100	—	ns
Address Valid to End of Write	t _{AW}	75	—	90	—	100	—	ns
Output Active from End of Write	t _{wx}	5	—	5	—	5	—	ns



- Notes
1. A Write Cycle occurs during the overlap of a low \overline{CS} , and a low \overline{WE} .
 2. OE may be both high and low in a Write Cycle.
 3. t_{AS} is specified from \overline{CS} or \overline{WE} , whichever occurs last.
 4. t_w is an overlap time of a low \overline{CS} , and a low \overline{WE} .
 5. t_{wr}, t_{DS}, and t_{DH} are specified from \overline{CS} or \overline{WE} , whichever occurs first.
 6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
 7. When I/O pins are Data output mode, don't force inverse signals to those pins.

• LOW V_{CC} DATA RETENTION CHARACTERISTICS

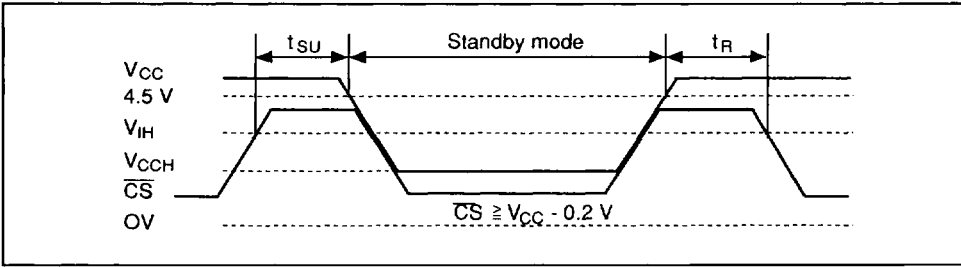
(T_a = 0 ~ +70°C, unless otherwise noted)

Rating	Symbol	Conditions	Specified Value			Unit
			Min.	Typ.	Max.	
V _{CC} for Data Retention	V _{CCH}	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$	2.0	—	—	V
Data Retention Current	I _{CCH}	V _{CC} = 3 V, $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$	—	—	10*	μA
CS to Data Retention Time	t _{SU}	—	0	—	—	ns
Operation Recovery Time	t _R	—	t _{RC} **	—	—	ns

* T_a = 0 to 40°C : 3 μA Max.

** t_{RC} = Read Cycle Time

\overline{CS} CONTROL



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I/O CAPACITANCE

(T_a=25°C, f=1MHz)

Rating	Symbol	Conditions	Specified Value		Unit
			Min.	Max.	
Input Capacitance	C _{IO}	—	—	10	pF
I/O Capacitance	C _{IN}	—	—	10	pF