

**PSRAM**

**4-Mbit (256K x 16) Pseudo Static RAM**

**Features**

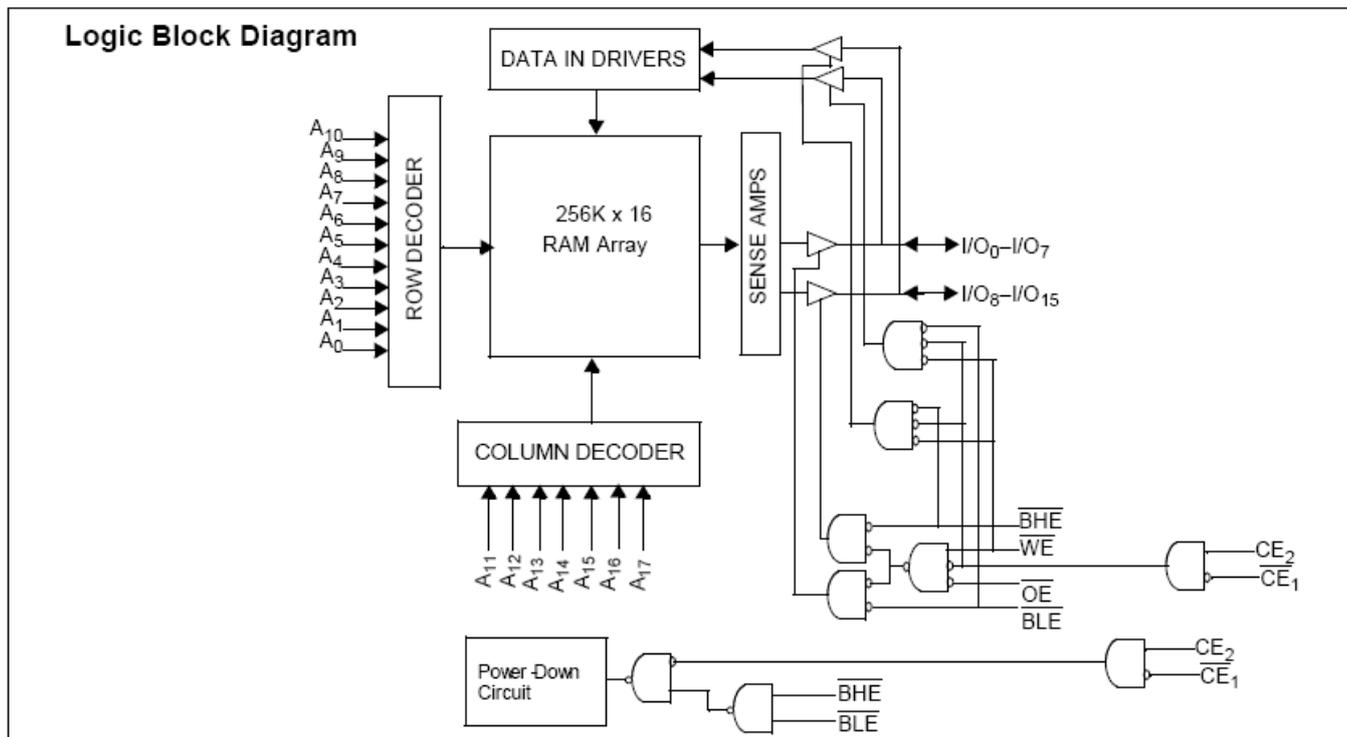
- Advanced low-power architecture
- High speed: 55 ns, 60 ns and 70 ns
- Wide voltage range: 2.7V to 3.6V
- Typical active current: 1 mA @ f = 1 MHz
- Low standby power
- Automatic power-down when deselected

**Functional Description**

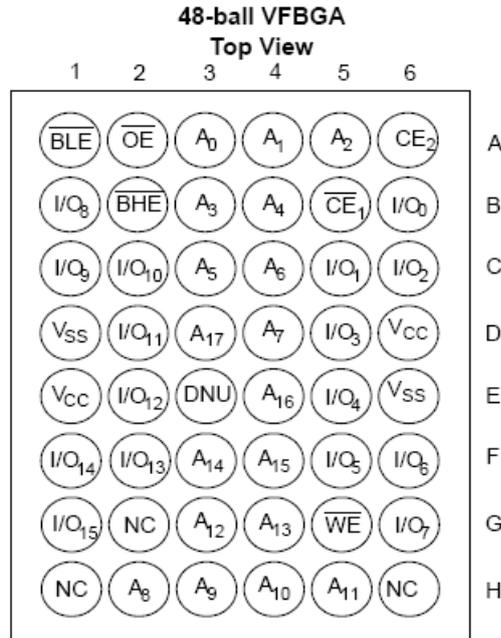
The M24L416256DA is a high-performance CMOS pseudo static RAM (PSRAM) organized as 256K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for portable applications such as cellular telephones. The device can be put into standby mode

reducing power consumption dramatically when deselected ( $\overline{CE1}$  HIGH,  $CE2$  LOW or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE1}$  HIGH,  $CE2$  LOW,  $\overline{OE}$  is HIGH), or during a write operation (Chip Enabled and Write Enable  $\overline{WE}$  LOW).

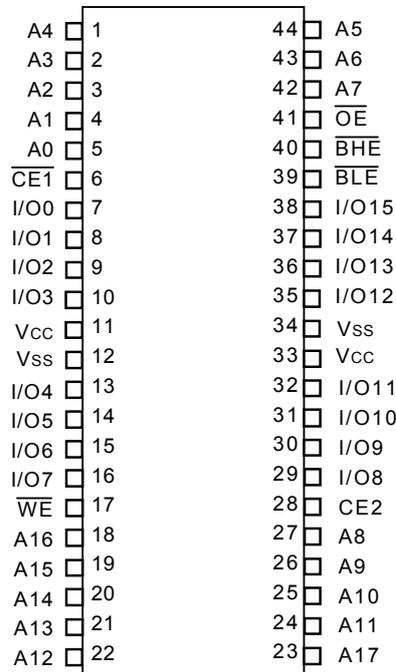
Reading from the device is accomplished by asserting the Chip Enables ( $\overline{CE1}$  LOW and  $CE2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins  $A_0$  through  $A_7$  will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the Truth Table for a complete description of read and write modes.



Pin Configuration[3, 4, 5]



**44-pin TSOPII**  
Top View



## Product Portfolio

Product	V <sub>CC</sub> Range(V)			Speed (ns)	Power Dissipation					
					Operating, I <sub>CC</sub> (mA)				Standby, I <sub>SB2</sub> (μA)	
	f = 1 MHz		f = f <sub>MAX</sub>							
	Min.	Typ.	Max.		Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.
M24L416256DA	2.7	3.0	3.6	55	1	5	14	22	17	40
				60						
				70						

## Notes:

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub> and T<sub>A</sub> = 25°C.
- Ball H1, G2, H6 are the address expansion pins for the 8-Mb, 16-Mb, and 32-Mb densities, respectively.
- NC "no connect"—not connected internally to the die.
- DNU (Do Not Use) pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application.

## Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature .....-65°C to +150°C  
 Ambient Temperature with Power Applied .....-55°C to +125°C  
 Supply Voltage to Ground Potential .....-0.4V to 4.6V  
 DC Voltage Applied to Outputs in High-Z State[6, 7, 8] .....-0.4V to 3.7V  
 DC Input Voltage[6, 7, 8] .....-0.4V to 3.7V  
 Output Current into Outputs (LOW) .....20 mA  
 Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current .....> 200 mA

## Operating Range

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub>
Extended	-25°C to +85°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

## DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	-55, 60, 70			Unit
			Min.	Typ.[2]	Max.	
V <sub>CC</sub>	Supply Voltage		2.7	3.0	3.6	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		0.8 * V <sub>CC</sub>		V <sub>CC</sub> + 0.4	V
V <sub>IL</sub>	Input LOW Voltage	F = 0	-0.4		0.62	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		14 for -55 14 for -60 08 for -70	22 for -55 22 for -60 15 for -70	mA
		f = 1 MHz	V <sub>CC</sub> = 3.6V, I <sub>OUT</sub> = 0 mA, CMOS level	1 for all speeds	5 for all speeds	
I <sub>SB1</sub>	Automatic $\overline{CE1}$ Power-down Current —CMOS Inputs	$\overline{CE1} \geq V_{CC} - 0.2V$ , $CE2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ , $V_{IN} \leq 0.2V$ , $f = f_{MAX}$ (Address and Data Only), $f = 0$ ( $\overline{OE}$ , $\overline{WE}$ , $BHE$ and $\overline{BLE}$ )		150	250	μA
I <sub>SB2</sub>	Automatic $\overline{CE1}$ Power-down Current —CMOS Inputs	$\overline{CE1} \geq V_{CC} - 0.2V$ , $CE2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $V_{CC} = 3.6V$		17	40	μA

## Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>	8	pF

## Thermal Resistance[9]

Parameter	Description	Test Conditions	VFPGA	Unit
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	55	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		17	°C/W

Notes:

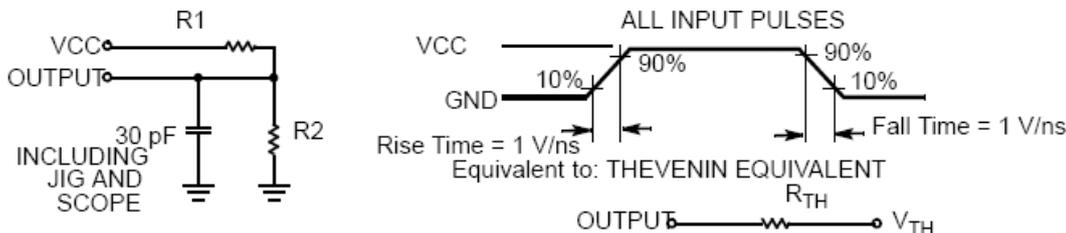
6. V<sub>IH(MAX)</sub> = V<sub>CC</sub> + 0.5V for pulse durations less than 20 ns.

7. V<sub>IL(MIN)</sub> = -0.5V for pulse durations less than 20 ns.

8. Overshoot and undershoot specifications are characterized and are not 100% tested.

9. Tested initially and after design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Parameters	3.0V V <sub>CC</sub>	Unit
R1	22000	Ω
R2	22000	Ω
R <sub>TH</sub>	11000	Ω
V <sub>TH</sub>	1.50	V

Switching Characteristics (Over the Operating Range)[10]

Parameter	Description	-55		-60		-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t <sub>RC</sub>	Read Cycle Time	55 <sup>[14]</sup>		60		70		ns
t <sub>AA</sub>	Address to Data Valid		55		60		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		8		10		ns
t <sub>ACE</sub>	$\overline{CE1}$ LOW and CE2 HIGH to Data Valid		55		60		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z[11, 12]	5		5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z[11, 12]		25		25		25	ns
t <sub>LZCE</sub>	$\overline{CE1}$ LOW and CE2 HIGH to Low Z[11, 12]	5		5		5		ns
t <sub>HZCE</sub>	$\overline{CE1}$ HIGH and CE2 LOW to High Z[11, 12]		25		25		25	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		55		60		70	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[11, 12]	5		5		5		ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z[11, 12]		10		10		25	ns
t <sub>SK</sub> <sup>[14]</sup>	Address Skew		0		5		10	ns
Write Cycle[13]								
t <sub>WC</sub>	Write Cycle Time	55		60		70		ns
t <sub>SCE</sub>	$\overline{CE1}$ LOW and CE2 HIGH to Write End	45		45		60		ns
t <sub>AW</sub>	Address Set-up to Write End	45		45		55		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		ns

Notes:

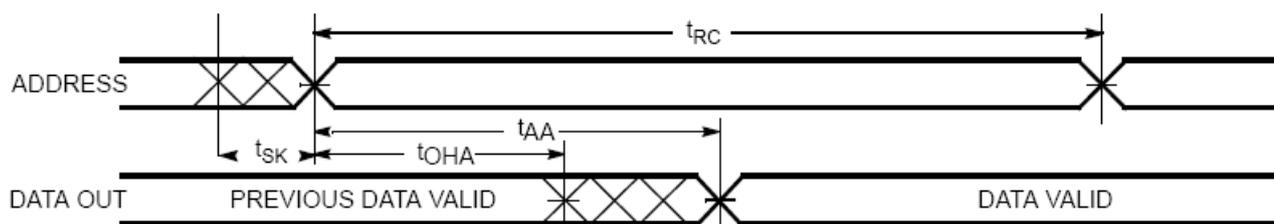
- Test conditions assume signal transition time of 1 V/ns or higher, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0V to V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub> and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE1} = V_{IL}$ , CE2 = V<sub>IH</sub>, BHE and/or BLE = V<sub>IL</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.
- To achieve 55-ns performance, the read access should be  $\overline{CE}$  controlled. In this case t<sub>ACE</sub> is the critical parameter and t<sub>SK</sub> is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Characteristics (Over the Operating Range)[10] (continued)

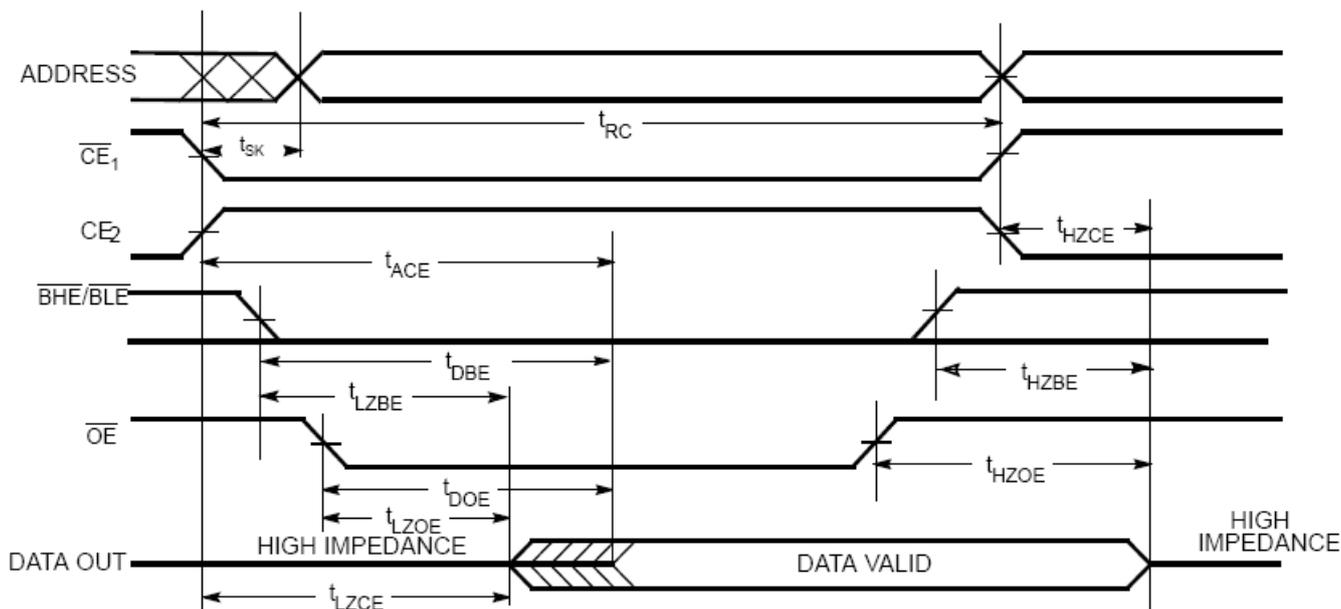
Parameter	Description	-55		-60		-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		40		45		ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to Write End	50		50		55		ns
$t_{SD}$	Data Set-up to Write End	25		25		25		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z[11, 12]		25		25		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z[11, 12]	5		5		5		ns

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[14, 15, 16]



Read Cycle 2 ( $\overline{OE}$  Controlled)[14, 16]



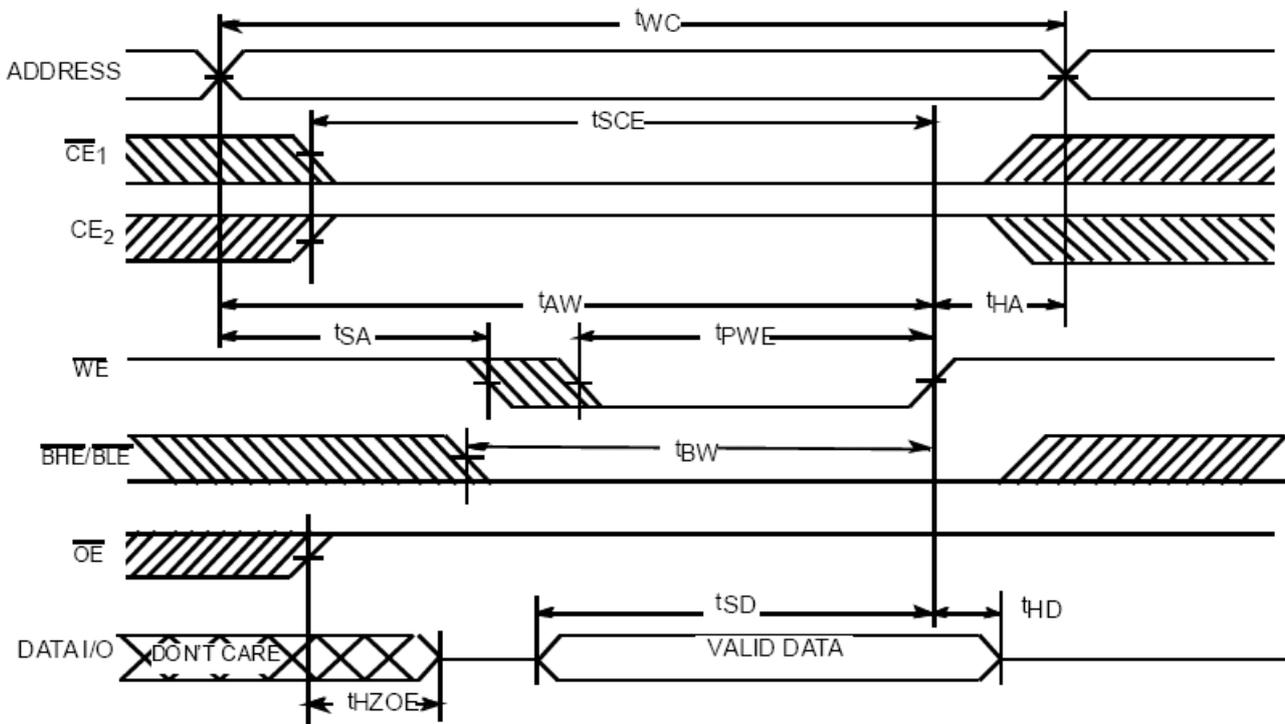
Notes:

15. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ .

16.  $\overline{WE}$  is HIGH for Read Cycle.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{WE}$  Controlled)[12, 13, 17, 18, 19]



Notes:

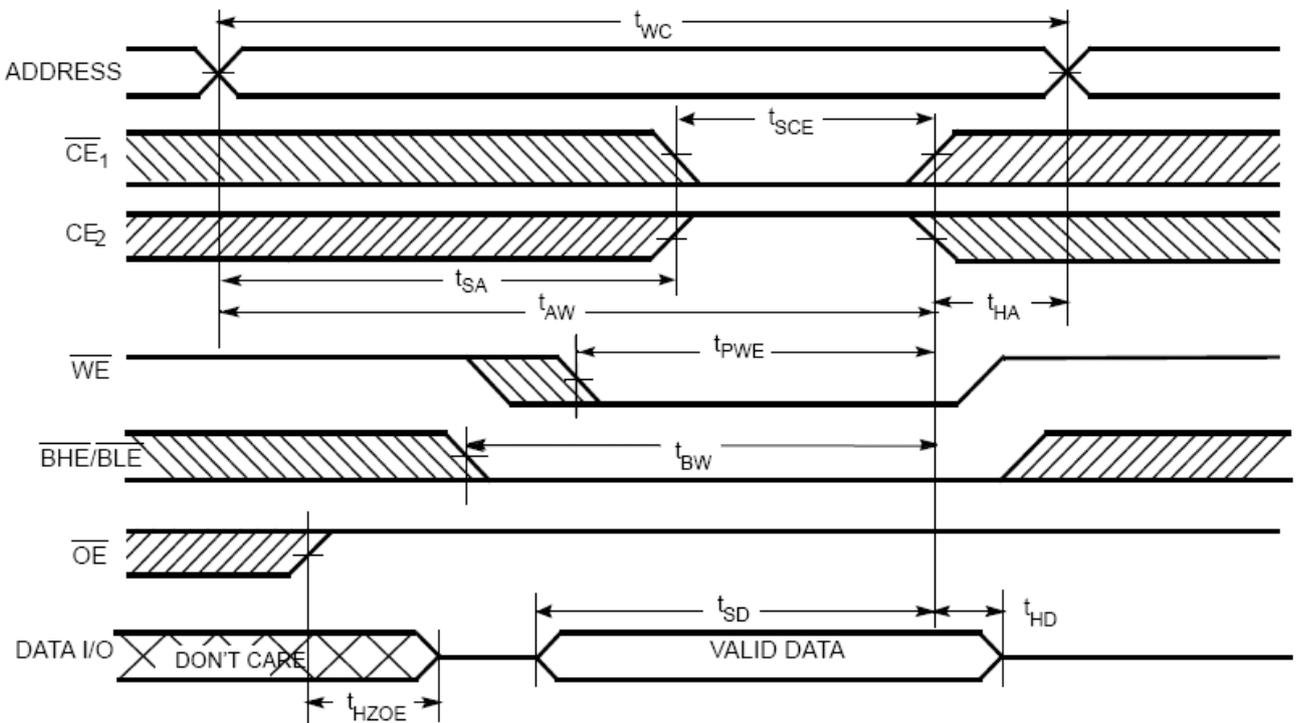
17.Data I/O is high impedance if  $\overline{OE} > V_{IH}$ .

18.If Chip Enable goes INACTIVE simultaneously with  $\overline{WE} = \text{HIGH}$ , the output remains in a high-impedance state.

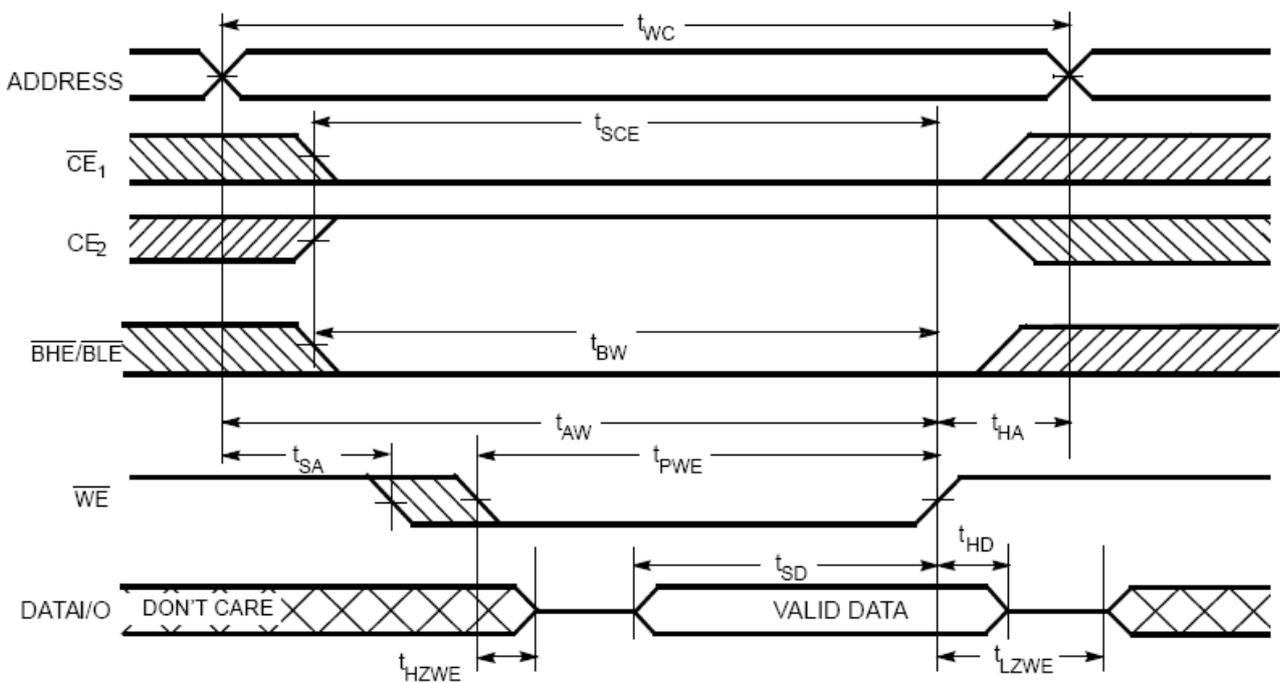
19.During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled)[12, 13, 17, 18, 19]

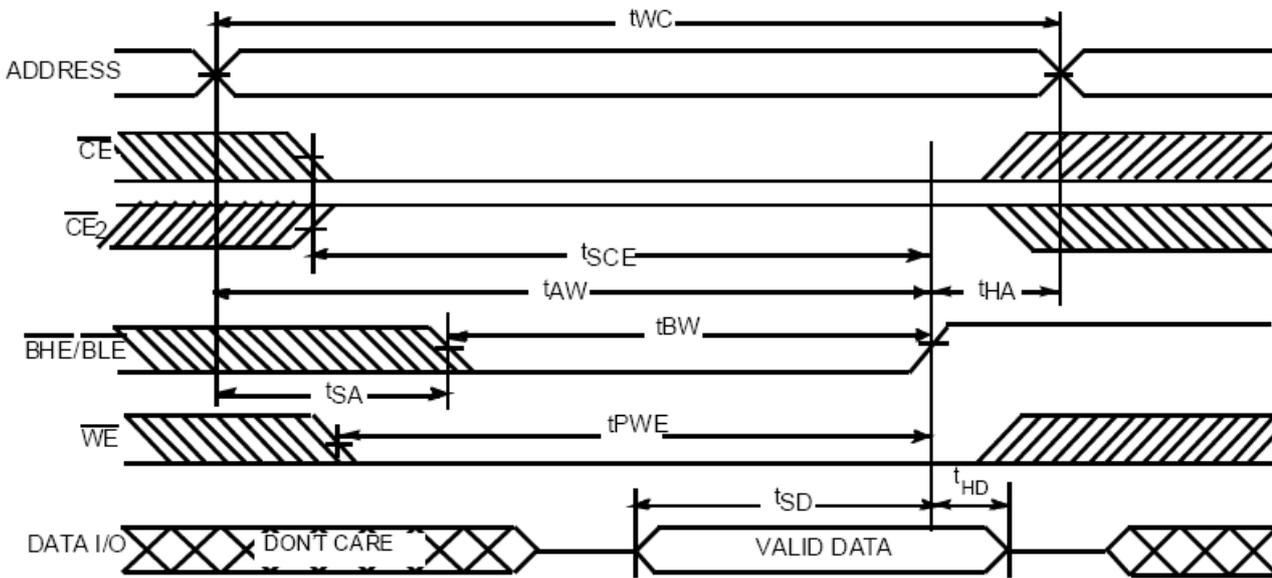


Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)[18, 19]



Switching Waveforms (continued)

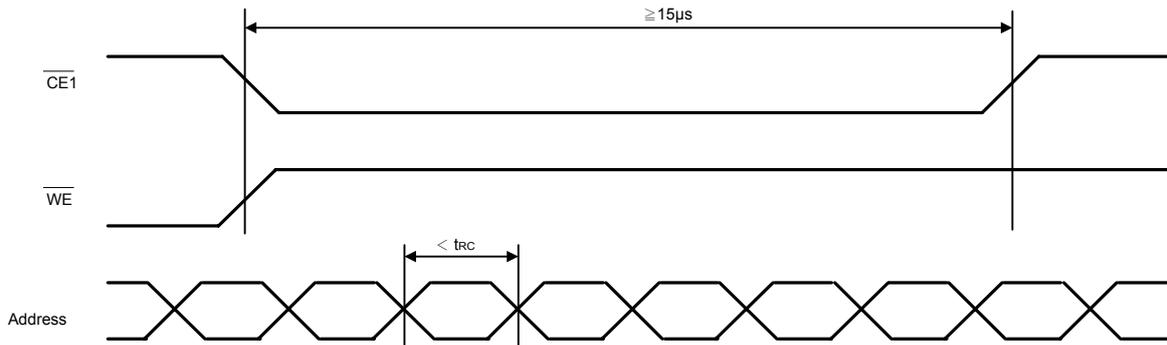
Write Cycle No. 4 (BHE/BL $\bar{E}$  Controlled,  $\bar{O}E$  LOW)[18, 19]



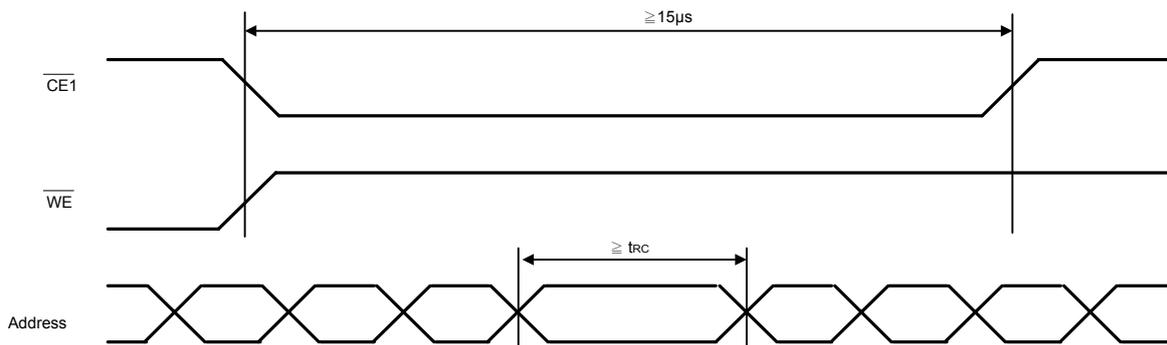
**Avoid Timing**

ESMT Pseudo SRAM has a timing which is not supported at read operation, If your system has multiple invalid address signal shorter than  $t_{RC}$  during over  $15\mu s$  at read operation shown as in Abnormal Timing, it requires a normal read timing at least during  $15\mu s$  shown as in Avoidable timing 1 or toggle  $\overline{CE1}$  to high ( $\geq t_{RC}$ ) one time at least shown as in Avoidable Timing 2.

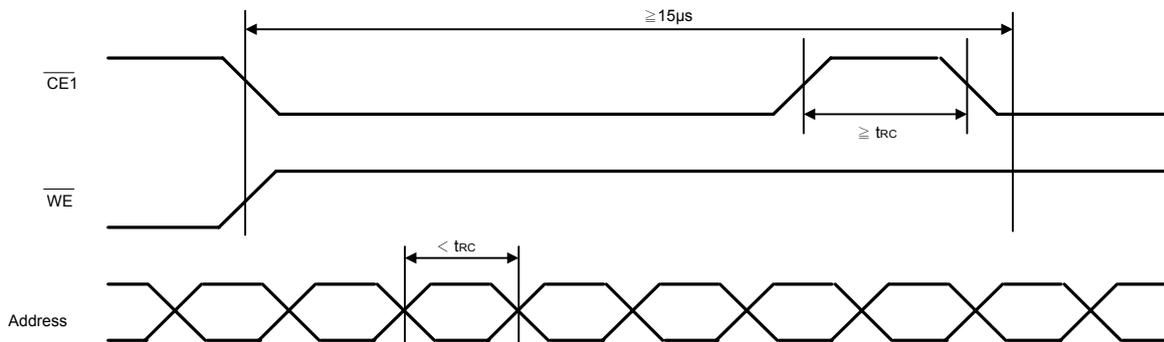
**Abnormal Timing**



**Avoidable Timing 1**



**Avoidable Timing 2**



Truth Table[20]

CE1	CE2	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
X	X	X	X	H	H	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
L	H	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read (Upper Byte and Lower Byte)	Active (I <sub>CC</sub> )
L	H	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Read (Upper Byte only)	Active (I <sub>CC</sub> )
L	H	H	L	L	H	Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Read (Lower Byte only)	Active (I <sub>CC</sub> )
L	H	H	H	L	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	H	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	L	H	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write (Upper Byte and Lower Byte)	Active (I <sub>CC</sub> )
L	H	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Write (Lower Byte Only)	Active (I <sub>CC</sub> )
L	H	L	X	L	H	Data In (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Write (Upper Byte Only)	Active (I <sub>CC</sub> )

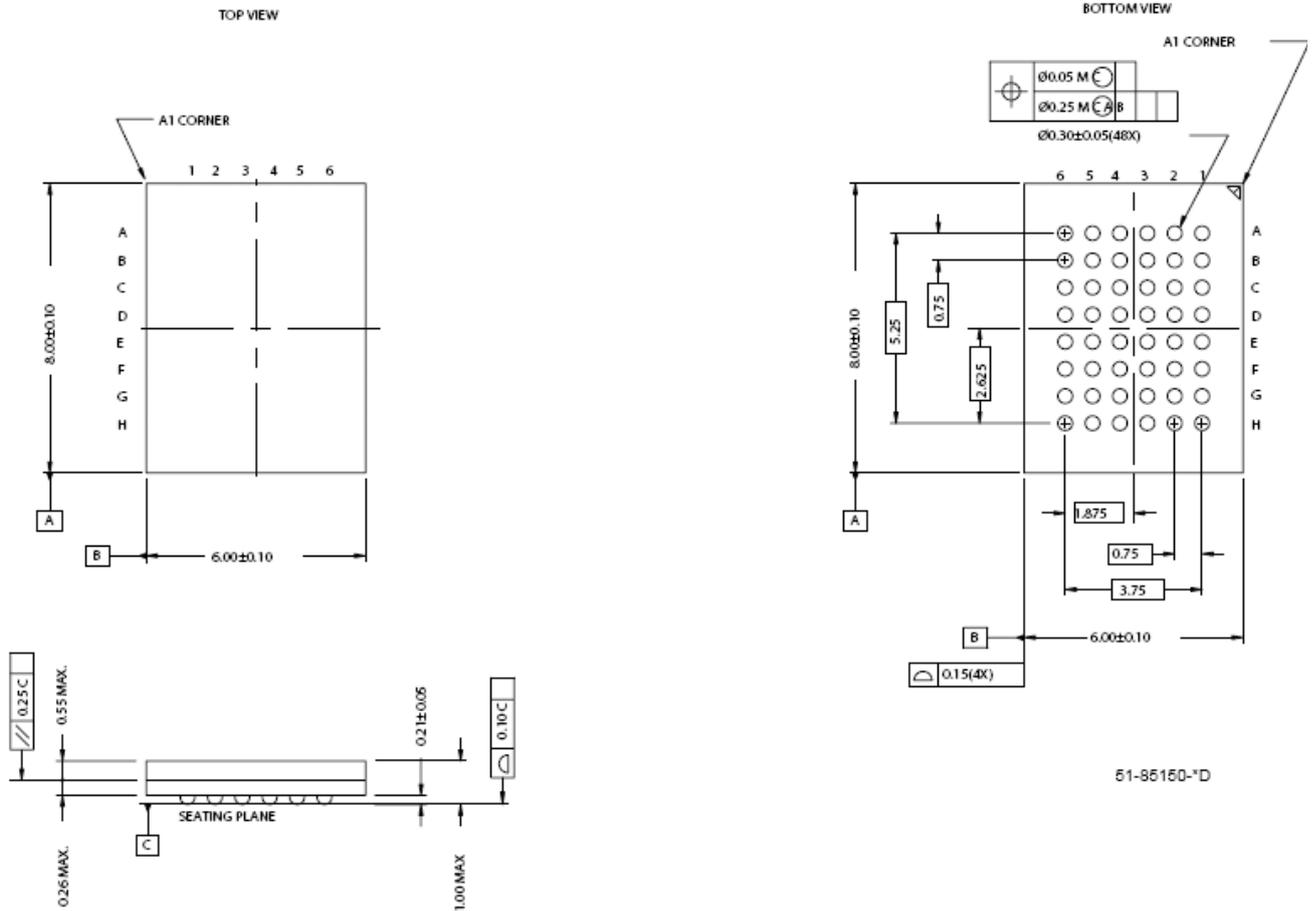
Note:  
20.H = Logic HIGH, L = Logic LOW, X = Don't Care.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
55	M24L416256DA-55BEG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.0 mm) (Pb-Free)	Extended
60	M24L416256DA-60BEG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.0 mm) (Pb-Free)	Extended
70	M24L416256DA-70BEG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.0 mm) (Pb-Free)	Extended
55	M24L416256DA-55TEG	44-pin TSOPII (Pb-Free)	Extended
60	M24L416256DA-60TEG	44-pin TSOPII (Pb-Free)	Extended
70	M24L416256DA-70TEG	44-pin TSOPII (Pb-Free)	Extended
55	M24L416256DA-55BIG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.0 mm) (Pb-Free)	Industrial
60	M24L416256DA-60BIG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.0 mm) (Pb-Free)	Industrial
70	M24L416256DA-70BIG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.0 mm) (Pb-Free)	Industrial
55	M24L416256DA-55TIG	44-pin TSOPII (Pb-Free)	Industrial
60	M24L416256DA-60TIG	44-pin TSOPII (Pb-Free)	Industrial
70	M24L416256DA-70TIG	44-pin TSOPII (Pb-Free)	Industrial

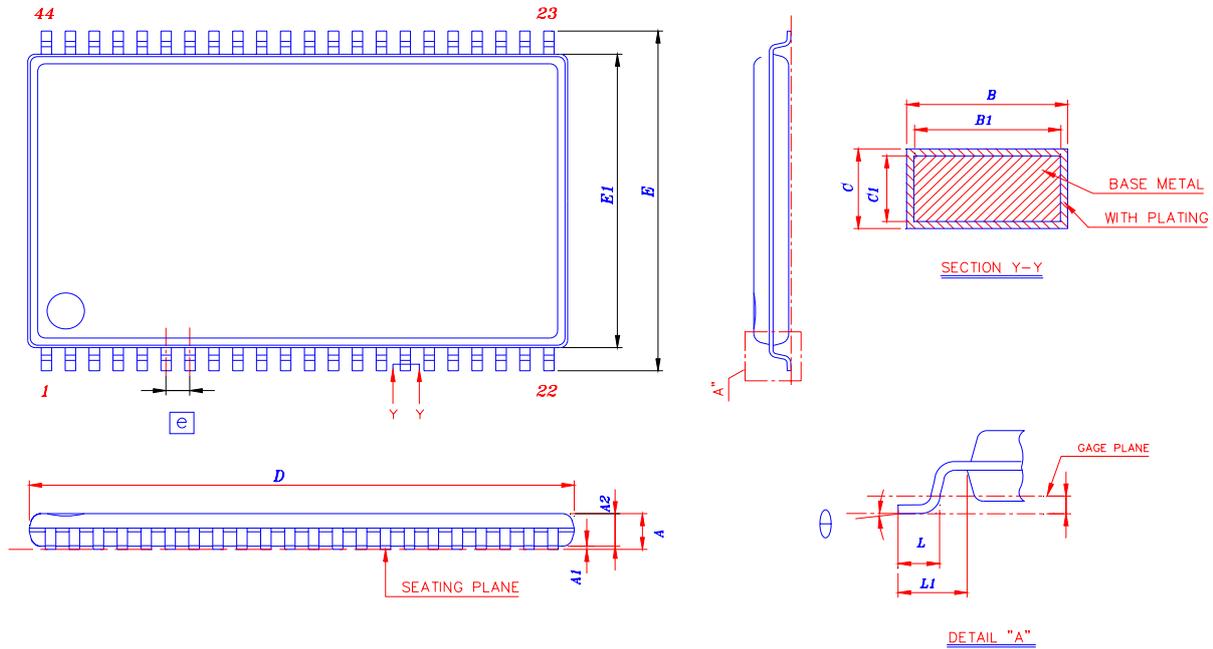
Package Diagram

48-ball VFBGA (6 x 8 x 1 mm)



44-LEAD TSOP(II)

PSRAM(400mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
B	0.30	—	0.45	0.012	—	0.018
B1	0.30	0.35	0.40	0.012	0.014	0.016
C	0.12	—	0.21	0.005	—	0.008
C1	0.10	—	0.16	0.004	—	0.006
D	18.28	18.41	18.54	0.720	0.725	0.730
ZD	0.805 REF			0.0317 REF		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.4
L	0.40	0.59	0.69	0.016	0.023	0.027
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.0315 BSC		
θ	0°	—	8°	0°	—	8°

## Revision History

Revision	Date	Description
1.0	2007.07.04	Original
1.1	2007.11.20	Modify the descriptive error for standby mode, $t_{HZWE}$ and $t_{LZWE}$ description
1.2	2007.11.22	Modify $t_{HZBE}$ and $t_{LZBE}$ descriptive and restore $t_{HZWE}$ and $t_{LZWE}$ description
1.3	2008.02.27	1.Add 44-pin TSOPII package 2. Add Avoid timing
1.4	2008.03.24	Add I-grade for TSOPII package
1.5	2008.07.04	1. Move Revision History to the last 2. Modify voltage range 2.7V~3.3V to 2.7V~3.6V 3. Add Industrial grade for BGA package

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