HARRIS

HI-5042/883
HI-5050/883

January 1989

SPDT CMOS Analog Switch

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Wide Analog Signal Range ..... ±15V**
- **Low "ON" Resistance**
  - **HI-5042 ..... 50Ω (Typ) 150Ω (Max)**
  - **HI-5050 ..... 25Ω (Typ) 50Ω (Max)**
- **High Current Capability ..... 70mA (Max)**
- **Break-Before-Make Switching**
  - **Turn-On Time ..... 370ns (Typ) 800ns (Max)**
  - **Turn-Off Time ..... 280ns (Typ) 400ns (Max)**
- **No Latch-Up**
- **Input MOS Gates Are Protected From Electrostatic Discharge**
- **DTL, TTL, CMOS, PMOS Compatible**

Applications

- **High Frequency Switching**
- **Sample and Hold**
- **Digital Filters**
- **Operational Amplifier Gain Switching**

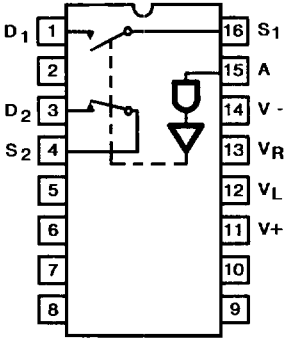
Description

These CMOS analog switches offer low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 50Ω for the HI-5042/883 and 25Ω for the HI-5050/883.

These devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). They also feature very low power operation (1.5mW at +25°C). The HI-5042/883 and HI-5050/883 are available in a 16 pin Ceramic DIP and operate over the -55°C to +125°C temperature range.

Pinout

LOGIC "0" INPUT
TOP VIEW

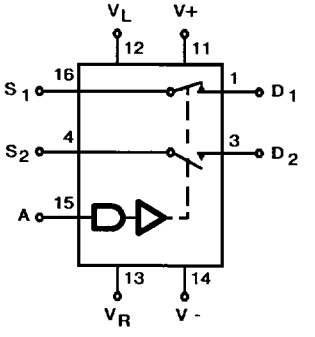


HI1-5042/883 (CERAMIC DIP)
HI1-5050/883 (CERAMIC DIP)

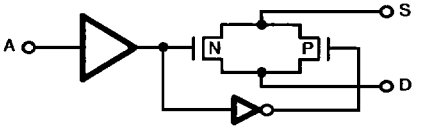
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) ..... ±18V
V_R to Ground ..... $-V_{SUPPLY}$
V_L to Ground ..... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
ESD Rating ..... <2000V
Lead Temperature (Soldering 10 sec) ..... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	20°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package ..... 12.3mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±15V
Logic Supply Voltage (V_L) ..... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) ..... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) ..... 0V to 0.8V
Address High Level (V_{AH}) ..... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance For HI-5042/883	R_{DS}	V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
		V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
Switch "ON" Resistance For HI-5050/883	R_{DS}	V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
		V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Low Level Address Current	I_{AL}	V_A = 0V	1	+25°C	-1	1	µA
			2,3	-55°C to +125°C	-10	1	µA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V	1	+25°C	-1	1	µA
			2,3	-55°C to +125°C	-1	10	µA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V	1	+25°C	-	200	µA
			2,3	-55°C to +125°C	-	300	µA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V	1	+25°C	-200	-	µA
			2,3	-55°C to +125°C	-300	-	µA
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25°C	-	200	µA
			2,3	-55°C to +125°C	-	300	µA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25°C	-200	-	µA
			2,3	-55°C to +125°C	-300	-	µA

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel) for HI-5042/883	R_{ON1} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
"On" Resistance Match (Channel to Channel) for HI-5050/883	R_{ON2} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	$V_S = 2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Crosstalk	V_{CT}	$V_S = 2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

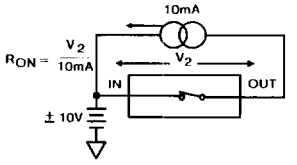
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

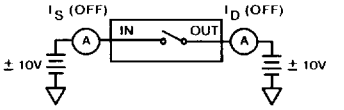
* PDA applies to Subgroup 1 only.

Test Circuits

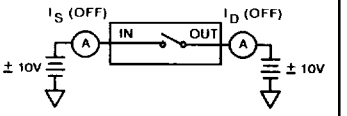
R_{DS}



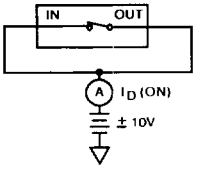
$I_{S(OFF)}$



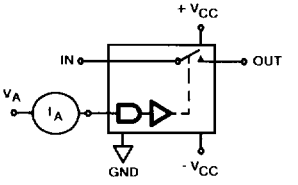
$I_{D(OFF)}$



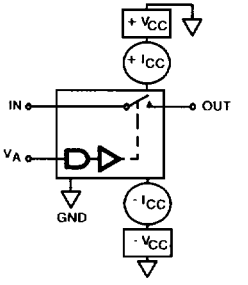
$I_{D(ON)}$



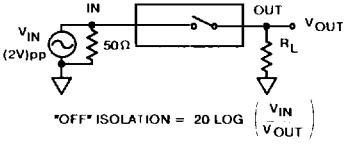
ADDRESS CURRENT



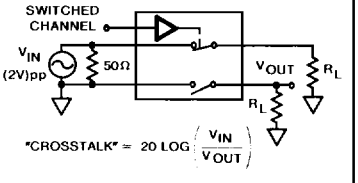
SUPPLY CURRENTS



OFF ISOLATION

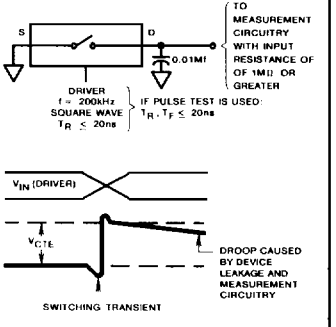


CROSSTALK



NOTE: Applies only to DUAL or DOUBLE THROW switches.

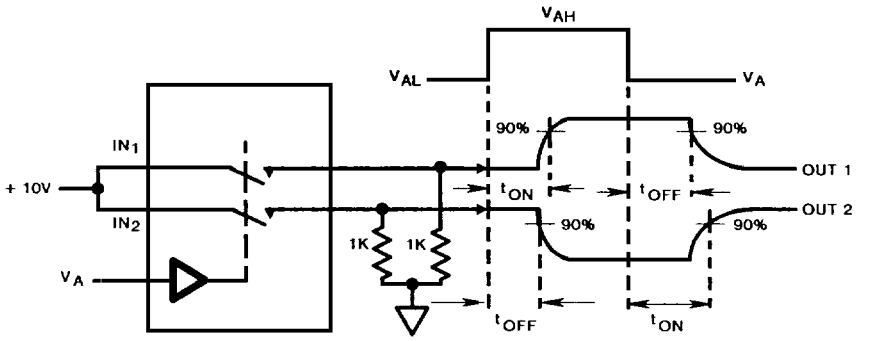
CHARGE TRANSFER



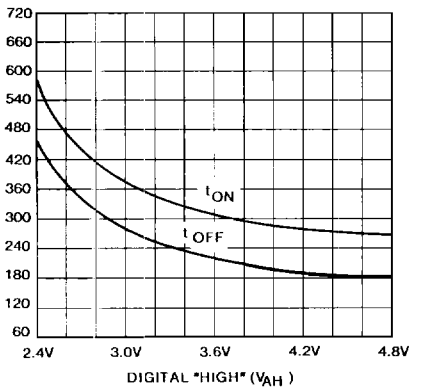
NOTE: V_{CTE} may be a positive or negative value.

Test Characteristics

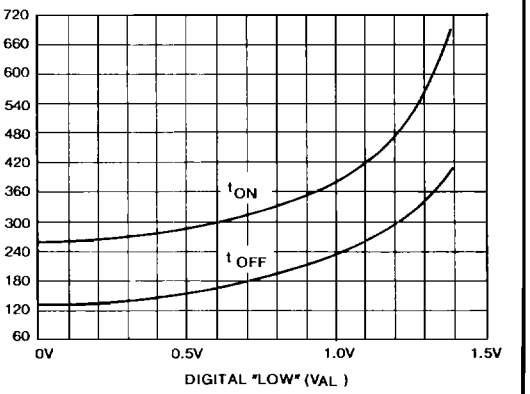
ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION

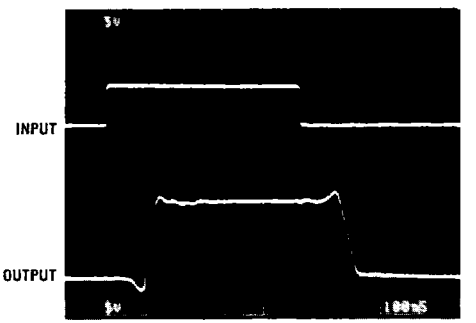


SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION

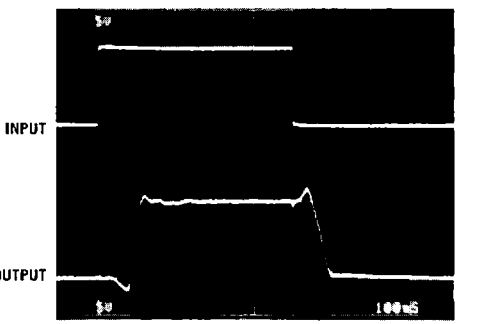


Test Waveforms

Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.
Horizontal Scale: 100ns/Div.

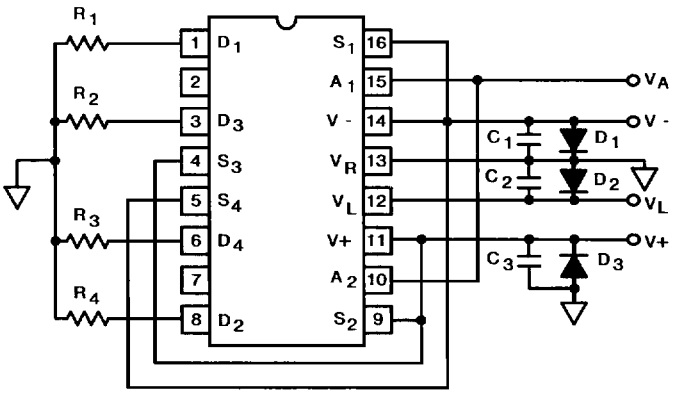


Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.
Horizontal Scale: 100ns/Div.



Burn-In Circuit

HI-5042/883 HI-5050/883 CERAMIC DIP

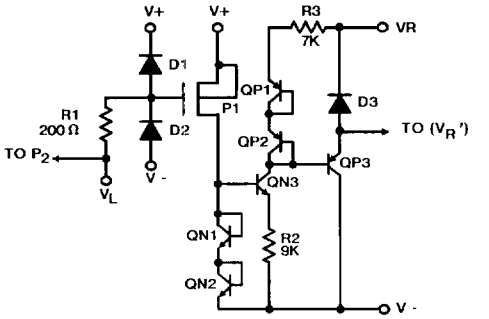


NOTES:

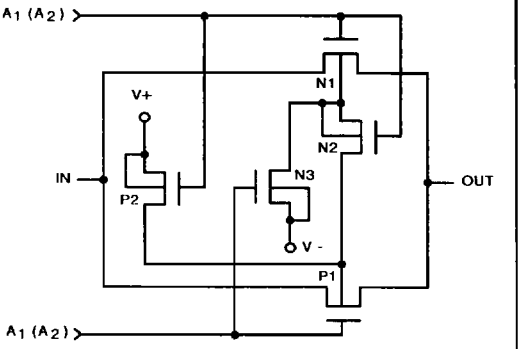
R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)
C_1, C_2, C_3, = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)
D_1, D_2, D_3 = IN4002 or Equivalent/Board
V_L = 5.5 ± 0.5V
$A_1 = A_2$ = 5.5 ± 0.5V
$|(V+) - (V-)|$ = 30V

Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

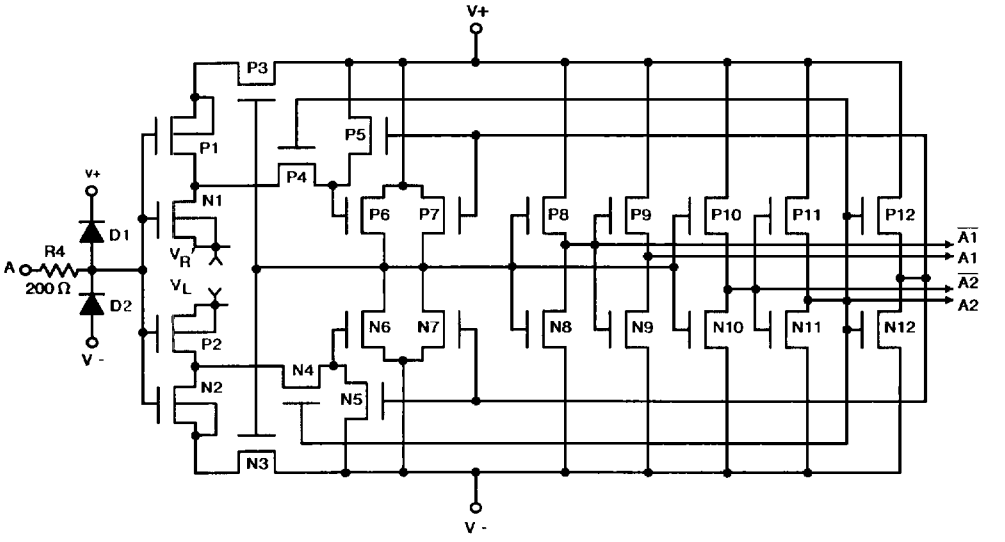


SWITCH CELL



* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V-
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

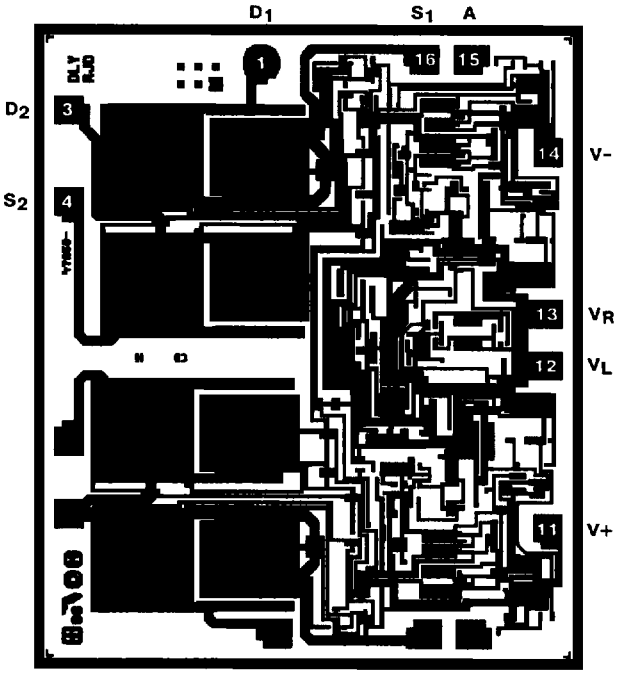
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

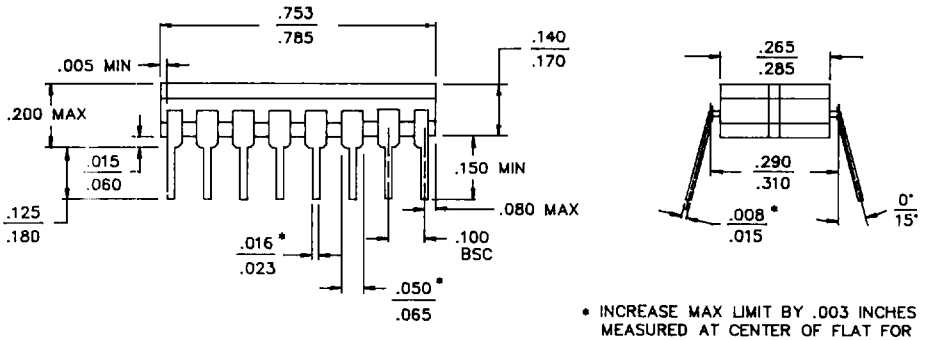
HI-5042/883 HI-5050/883



NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging†

16 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

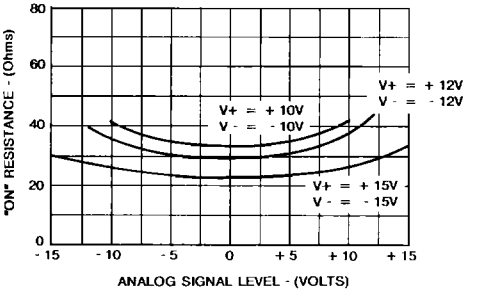
NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

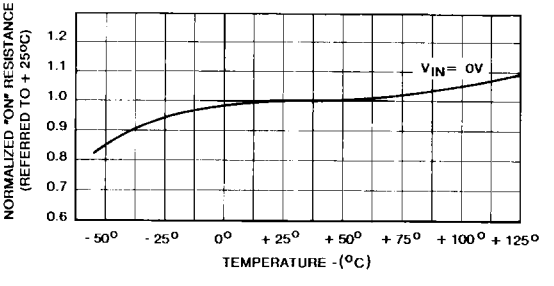
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT