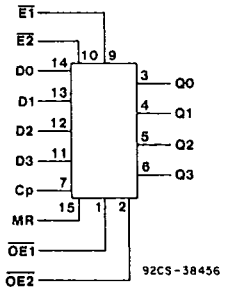
T-46-07-09

CD54/74HC173
CD54/74HCT173

File Number **1641**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad D-Type Flip-Flop, 3-State

Positive-Edge Triggered

Type Features:

- *3-state buffered outputs*
- *gated input and output enables*

The RCA CD54/74HC173 and CD54/74HCT173 high speed 3-STATE QUAD D TYPE FLIP-FLOPS are fabricated with silicon gate CMOS technology. They possess the low power consumption of standard CMOS Integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky devices. The buffered outputs can drive 15 LSTTL loads. The large output drive capability and 3-STATE feature make these parts ideally suited for interfacing with bus lines in bus oriented systems.

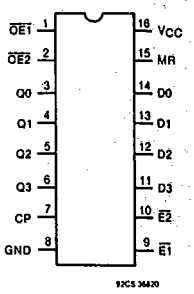
The four D TYPE FLIP-FLOPS operate synchronously from a common clock. The outputs are in the 3-STATE mode when either of the two output disable pins are at the logic "1" level. The input ENABLES allow the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input ENABLES are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip flops to remain in the same state. Reset is enabled by taking the MASTER RESET (MR) input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

The CD54/74HCT173 logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC173 and CD54HCT173 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC173 and D74HCT173 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

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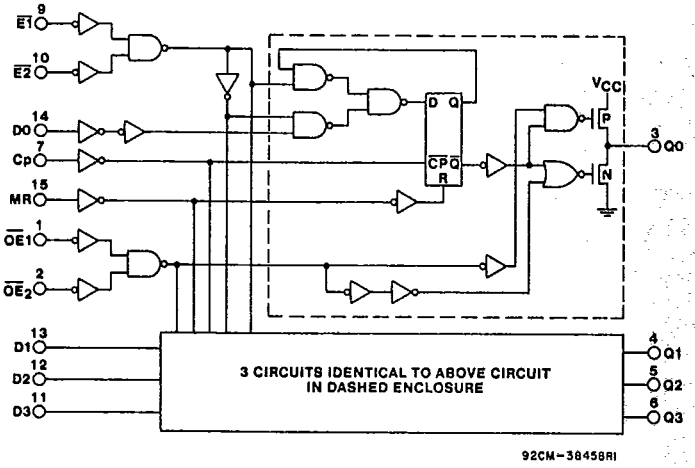
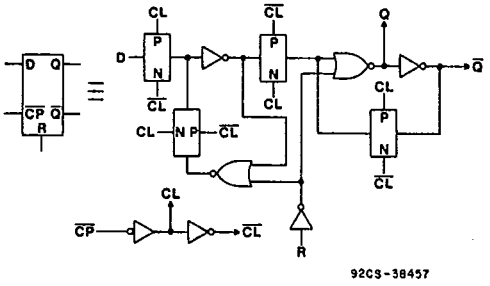


Fig. 1 — Logic diagram for the CD54/74HC/HCT173.



Flip-Flop Detail

TRUTH TABLE

Inputs					Output
		Data Enable		Data	
MR	CP	$\overline{E1}$	$\overline{E2}$	D	Q
H	X	X	X	X	L
L	↓	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either $\overline{OE1}$ or $\overline{OE2}$ (or both) is (are) high the output is disabled to the high-impedance state, however, sequential operation of the flip-flops is not affected.

H = high level (steady state) X = don't care (any input including transitions)
L = low level (steady state) Q_0 = the level of Q before the indicated steady-state input conditions were established.
↑ = low-to-high level transition

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) ..... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) ..... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} +0.5$ V) ..... ± 35 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ± 70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC173/CD54HC173										CD74HCT173/CD54HCT173									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O=V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D0-D3	0.15
$\overline{E1}$ & $\overline{E2}$	0.15
CP	0.25
MR	0.2
$\overline{OE1}$ & $\overline{OE2}$	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay, Clock to Q	t_{PLH}, t_{PHL}	15	17	18	ns
Propagation Delay, Output Disable and Enable to Q	t_{PLZ}, t_{PHZ}	15	12	12	ns
	t_{PZL}, t_{PZH}	15	12	14	ns
Maximum Clock Frequency	f_{max}	—	60	60	MHz
Power Dissipation Capacitance*	C_{PD}	—	29	34	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where: f_i = input frequency, f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Maximum Clock Frequency f_{max} Fig. 3	2	6		—		5		—		4		—		MHz
	4.5	30		20		24		16		20		13		
	6	35		—		28		—		24		—		
MR Pulse Width t_w Fig. 4	2	80		—		100		—		120		—		ns
	4.5	16		15		20		19		24		22		
	6	14		—		17		—		20		—		
Clock Pulse Width t_w Fig. 3	2	80		—		100		—		120		—		ns
	4.5	16		25		20		31		24		38		
	6	14		—		17		—		20		—		
Set-up Time Data to Clock Fig. 5 t_{SU}	2	60		—		75		—		90		—		ns
	4.5	12		12		15		15		18		18		
	6	10		—		13		—		15		—		
Set-up Time $\overline{E}$ to Clock t_{SU}	2	60		—		75		—		90		—		ns
	4.5	12		18		15		23		18		27		
	6	10		—		13		—		15		—		
Hold Time Data to Clock Fig. 5 t_H	2	3		—		3		—		3		—		ns
	4.5	3		0		3		0		3		0		
	6	3		—		3		—		3		—		
Hold Time $\overline{E}$ to Clock t_H	2	0		—		0		—		0		—		ns
	4.5	0		0		0		0		0		0		
	6	0		—		0		—		0		—		
Removal Time MR to Clock t_{REM}	2	60		—		75		—		90		—		ns
	4.5	12		12		15		15		18		18		
	6	10		—		13		—		15		—		

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SWITCHING CHARACTERISTICS (V_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay	t_{PLH}	2	—	200	—	—	—	250	—	—	—	300	—	—	
Clock to Output	t_{PHL}	4.5	—	40	—	43	—	50	—	54	—	60	—	65	ns
Fig. 3		6	—	34	—	—	—	43	—	—	—	51	—	—	
Propagation Delay		2	—	175	—	—	—	220	—	—	—	265	—	—	
MR to Output	t_{PHL}	4.5	—	35	—	37	—	44	—	46	—	53	—	56	ns
Fig. 4		6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay,	t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Output Enable to Q	t_{PHZ}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
		6	—	26	—	—	—	33	—	—	—	38	—	—	
	t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PZH}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
Fig.6		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
Fig. 3		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10		10		10		10		10		10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF

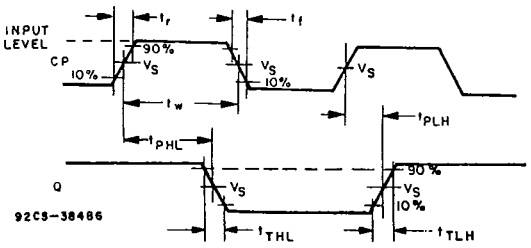

Fig. 3 — Clock to output delays and clock pulse width.

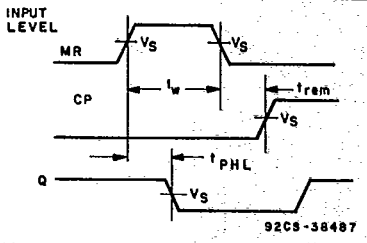

Fig. 4 — Master reset pulse width, Master reset to output delay and master reset to clock recovery time.

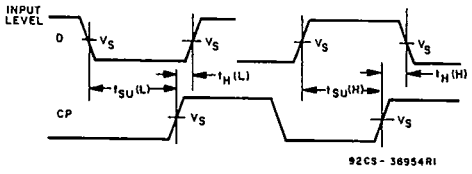

Fig. 5 — Data set-up and hold times.

	CD54/74HC	CD54/74HCT
Input Level	V_{CC}	3 V
Vs	0.5 V_{CC}	1.3 V

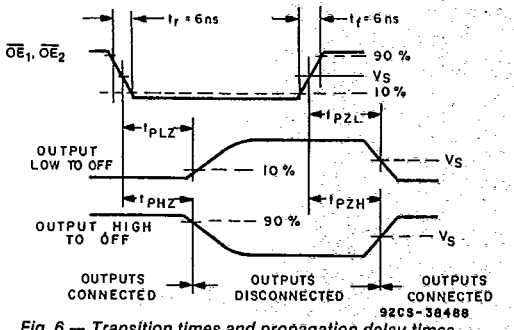

Fig. 6 — Transition times and propagation delay times.