HARRIS Semiconductor

IH5140 thru IH5145

April 1999

High-Level CMOS Analog Switches

OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
IH5140, IH5141: DG401
IH5142: HI-5042, DG403, HI-5043
IH5143: DG403, HI-5043, HI-0390
IH5144, IH5145: HI-5049, HI-5045
NOTE: Pinout and pin count of single devices allow dual devices to be pin compatible replacements.

Features

- **Super Fas**
- **SPST Switc**
  - **t_{ON} 80ns**
  - **t_{OFF} 50ns**
- **Power Supply Currents . . . . . <1μA**
- **OFF Leakages at 25°C (Typ) . . . . . <100pA**
- **Non-Latching with Supply Turn-Off**
- **Single Monolithic CMOS Chip**
- **Plug-In Replacements for IH5040 Family and Part of the DG180 Family to Upgrade Speed and Leakage**
- **Toggle Rate . . . . . >1MHz**
- **Switches Signals with ±15V Supplies . . . . . >20V_{P-P}**
- **TTL, CMOS Direct Compatibility**
- **Internal Diode in Series with V+ for Fault Protection**

Description

The IH5140 Family of CMOS switches utilizes Harris' latch-free junction isolated processing to build the fastest switches currently available. These switches can be toggled at a rate of greater than 1MHz with fast t_{ON} times (80ns typical) and faster t_{OFF} times (50ns typical), guaranteeing break before make switching. This family of switches combines the speed of the hybrid FET DG180 family with the reliability and low power consumption of a monolithic CMOS construction.

Very low quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 10μA (at 25°C) from any supply and typical quiescent currents are in the 10nA which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic. It is pin compatible with Harris' IH5040 family and part of the DG180/DG190 family as shown in the switching state diagrams.

Part Number Information

PART NUMBER	FUNCTION	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
IH5140MJE	SPST	-55 to 125	16 Ld CerDIP	
IH5140CJE	SPST	0 to 70	16 Ld CERDIP	
IH5140CPE	SPST	0 to 70	16 Ld PDIP	
IH5141MJE	Dual SPST	-55 to 125	16 Ld CerDIP	
IH5141CJE	Dual SPST	0 to 70	16 Ld CERDIP	
IH5141CPE	Dual SPST	0 to 70	16 Ld PDIP	
IH5142MJE	SPDT	-55 to 125	16 Ld CerDIP	
IH5142CJE	SPDT	0 to 70	16 Ld CERDIP	
IH5142CPE	SPDT	0 to 70	16 Ld PDIP	
IH5143MJE	Dual SPDT	-55 to 125	16 Ld CERDIP	
IH5143CJE	Dual SPDT	0 to 70	16 Ld CerDIP	
IH5143CPE	Dual SPDT	0 to 70	16 Ld PDIP	
IH5144MJE	DPST	-55 to 125	16 Ld CERDIP	
IH5144CJE	DPST	0 to 70	16 Ld CERDIP	
IH5144CPE	DPST	0 to 70	16 Ld PDIP	
IH5145MJE	Dual DPST	-55 to 125	16 Ld CerDIP	
IH5145CJE	Dual DPST	0 to 70	16 Ld CerDIP	
IH5145CPE	Dual DPST	0 to 70	16 Ld PDIP	
IH5140MJE/883B	SPST	-55 to 125	16 Ld CERDIP	
IH5141MJE/883B	Dual SPST	-55 to 125	16 Ld CERDIP	
IH5142MJE/883B	SPDT	-55 to 125	16 Ld CERDIP	
IH5143MJE/883B	Dual SPDT	-55 to 125	16 Ld CERDIP	
IH5144MJE/883B	DPST	-55 to 125	16 Ld CERDIP	
IH5145MJE/883B	Dual DPST	-55 to 125	16 Ld CERDIP	

NOTE:

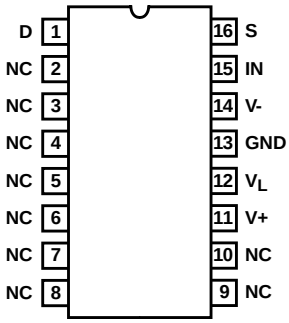
1. For MIL-STD-883 compliant parts, request the /883 datasheet on the above products.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

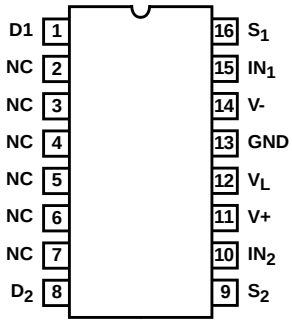
File Number **3132.2**

Pinouts

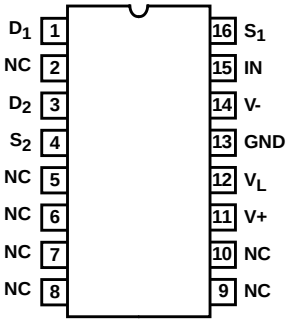
IH5140
(PDIP, CERDIP)
TOP VIEW



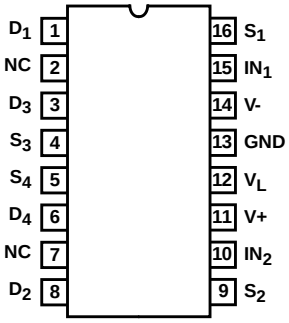
IH5141
(PDIP, CERDIP)
TOP VIEW



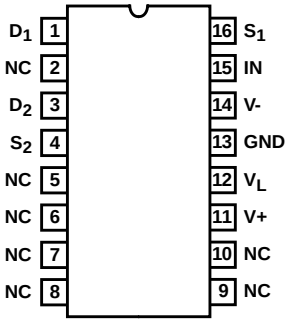
IH5142
(PDIP, CERDIP)
TOP VIEW



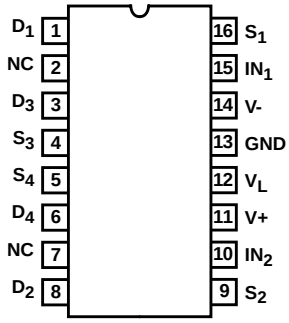
IH5143
(PDIP, CERDIP)
TOP VIEW



IH5144
(PDIP, CERDIP)
TOP VIEW

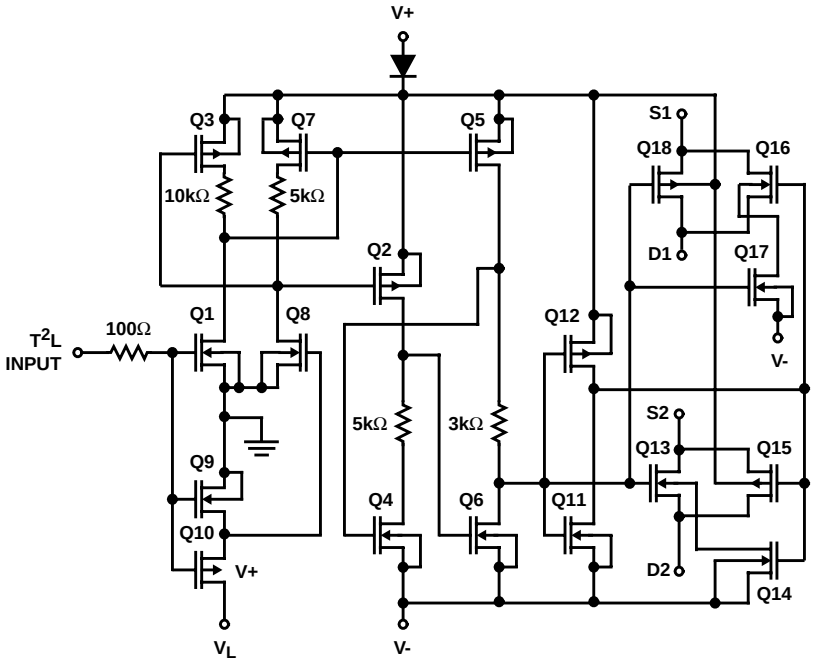


IH5145
(PDIP, CERDIP)
TOP VIEW



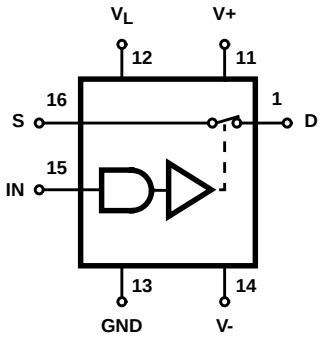
Functional Block Diagram

TYPICAL DRIVER/GATE - IH5142

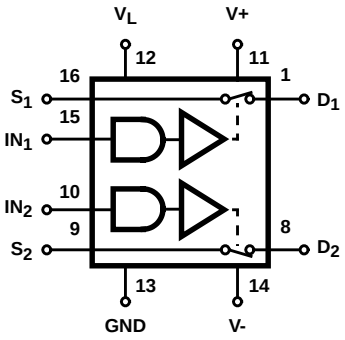


Switching State Diagrams

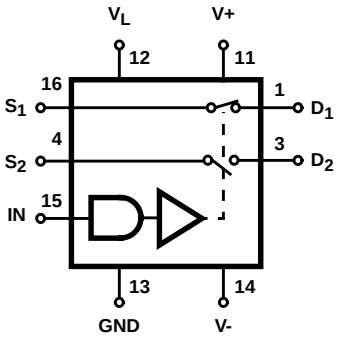
DIP (JE, PE)
SPST IH5140



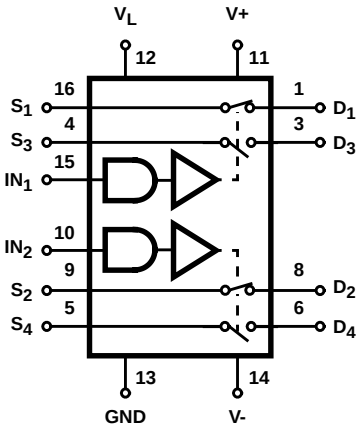
DIP (JE, PE)
DUAL SPST IH5141



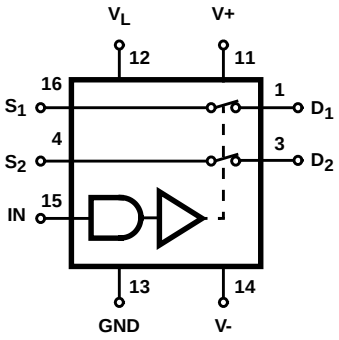
DIP (JE, PE)
SPDT IH5142



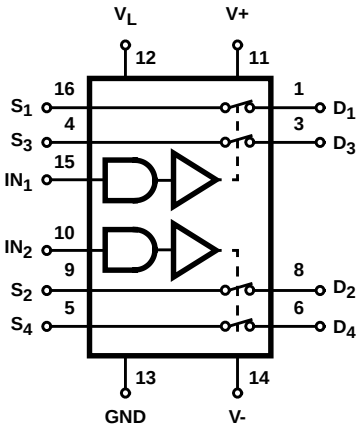
DIP (JE, PE)
DUAL SPDT IH5143



DIP (JE, PE)
DPST IH5144



DIP (JE, PE)
DUAL DPST IH5145



Absolute Maximum Ratings

V+ to V- . . . . . <36V
V+ to V_D . . . . . <30V
V_D to V- . . . . . <30V
V_D to V_S . . . . . <±22V
V_L to V- . . . . . <33V
V_L to V_{IN} . . . . . <30V
V_L to GND . . . . . <20V
V_{IN} to GND . . . . . <20V
Current (Any Terminal) 30mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	80	24
PDIP Package	100	N/A

Maximum Junction Temperature
CERDIP Package . . . . . 175^oC
PDIP Package . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions

Temperature Ranges
Military . . . . . -55^oC to 125^oC
Commercial . . . . . 0^oC to 70^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

25^oC, V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNITS
		-55^oC	25^oC	125^oC	0^oC	25^oC	70^oC	
LOGIC INPUT								
Input Logic Current, I_{INH}	V_{IN} = 2.4V, Note 1	±1	±1	10	–	±10	10	µA
Input Logic Current, I_{INL}	V_{IN} = 0.8V, Note 1	±1	±1	10	–	±10	10	µA
SWITCH								
Drain Source On Resistance, $r_{DS(ON)}$	I_S = -10mA, V_{ANALOG} = -10V to +10V	50	50	75	75	75	100	Ω
Channel to Channel $r_{DS(ON)}$ Match, $\Delta r_{DS(ON)}$		-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±11 (Typ)	-	-	±10 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}+I_{S(OFF)}$	V_D = +10V, V_S = -10V	-	±0.5	100	-	±5	100	nA
	V_D = -10V, V_S = +10V	-	±0.5	100	-	±5	100	nA
Switch On Leakage Current, $I_{D(ON)}+I_{S(ON)}$	V_D = V_S = -10V to +10V	-	±1	200	-	±2	200	nA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off; Any Other Channel Switches, See Performance Characteristics	-	54 (Typ)	-	-	50 (Typ)	-	dB
Switch "ON" Time, t_{ON}	See Switching Time Specifications and Timing Diagrams							
Switch "OFF" Time, t_{OFF}	See Switching Time Specifications and Timing Diagrams							
Charge Injection, $Q_{(INJ)}$	See Performance Characteristics	-	10 (Typ)	-	-	15 (Typ)	-	pC
Minimum Off Isolation Rejection Ratio, OIRR	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF, See Performance Characteristics	-	54 (Typ)	-	-	50 (Typ)	-	dB
SUPPLY								
+ Power Supply Quiescent Current, I+	V+ = +15V, V- = -15V, V_L = +5V, See Performance Characteristics	1.0	1.0	10	10	10	100	µA
- Power Supply Quiescent Current, I-		1.0	1.0	10	10	10	100	µA
+5V Supply Quiescent Current, I_L		1.0	1.0	10	10	10	100	µA
Ground Supply Quiescent Current, I_{GND}		1.0	1.0	10	10	10	100	µA

NOTES:

1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.

Switching Time Specifications t_{ON}, t_{OFF} are Maximum Specifications and t_{ON} - t_{OFF} is Minimum Specification

PART NUMBER	SPECIFICATIONS	TEST CONDITIONS	MILITARY			COMMERCIAL			UNITS
			-55°C	25°C	125°C	0°C	25°C	70°C	
IH5140, IH5141	Switch “ON” Time, t_{ON}	Figure 8, Note 2	-	100	-	-	150	-	ns
	Switch “OFF” Time, t_{OFF}		-	75	-	-	125	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
	Switch “ON” Time, t_{ON}	Figure 7	-	150	-	-	175	-	ns
	Switch “OFF” Time, t_{OFF}		-	125	-	-	150	-	ns
IH5142, IH5143	Switch “ON” Time, t_{ON}	Figure 8, Note 2	-	175	-	-	250	-	ns
	Switch “OFF” Time, t_{OFF}		-	125	-	-	150	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
	Switch “ON” Time, t_{ON}	Figure 7	-	200	-	-	300	-	ns
	Switch “OFF” Time, t_{OFF}		-	125	-	-	150	-	ns
	Switch “ON” Time, t_{ON}	Figure 2, Note 2	-	175	-	-	250	-	ns
	Switch “OFF” Time, t_{OFF}		-	125	-	-	150	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
	Switch “ON” Time, t_{ON}	Figure 3, Note 2	-	200	-	-	300	-	ns
	Switch “OFF” Time, t_{OFF}		-	125	-	-	150	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
IH5144, IH5145	Switch “ON” Time, t_{ON}	Figure 8, Note 2	-	175	-	-	250	-	ns
	Switch “OFF” Time, t_{OFF}		-	125	-	-	150	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
	Switch “ON” Time, t_{ON}	Figure 7	-	200	-	-	300	-	ns
	Switch “OFF” Time, t_{OFF}		-	125	-	-	150	-	ns

NOTES:

1. Switching times are measured at 90% points.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.

Typical Performance Curves

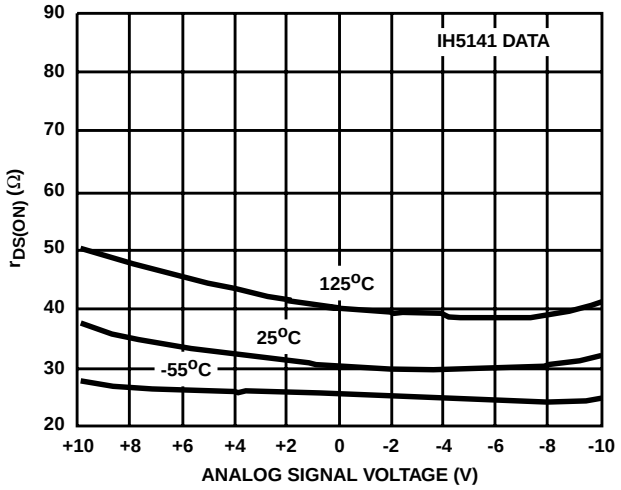


FIGURE 1. $r_{DS(ON)}$ vs TEMPERATURE AT ±15V, +5V SUPPLIES

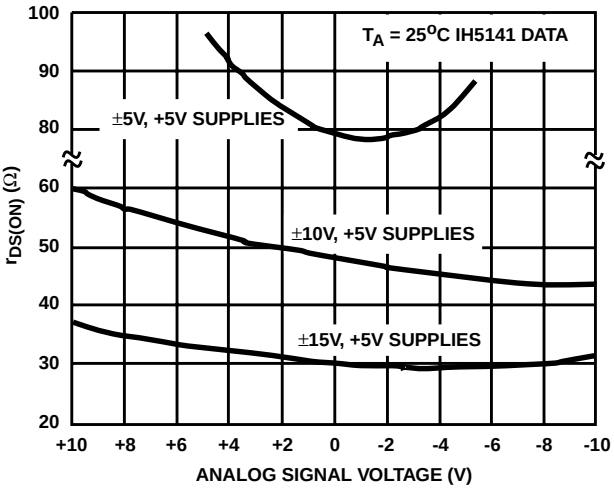


FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLIES

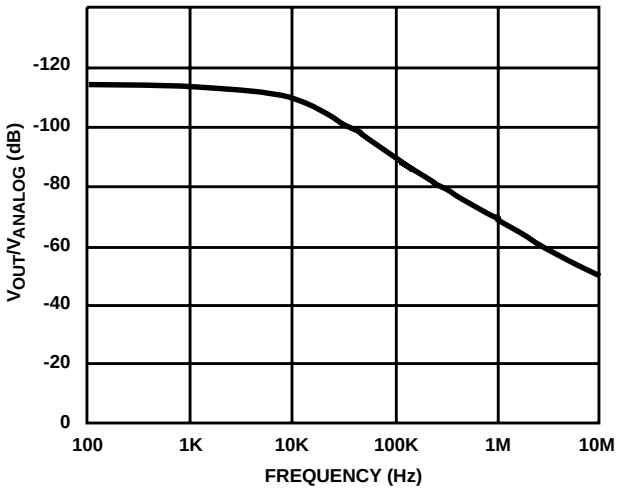


FIGURE 3A.

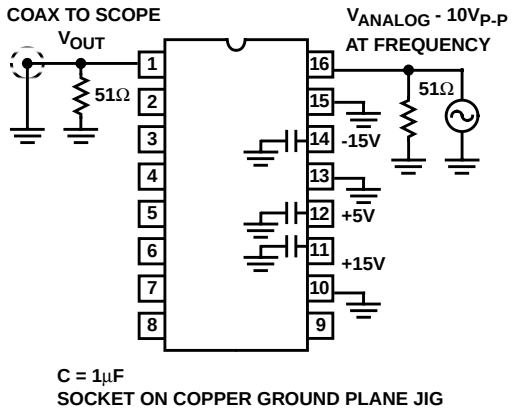


FIGURE 3B.

FIGURE 3. "OFF" ISOLATION vs FREQUENCY

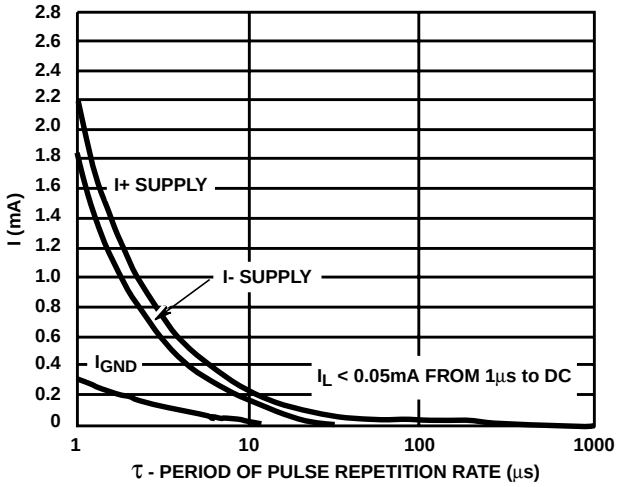


FIGURE 4A.

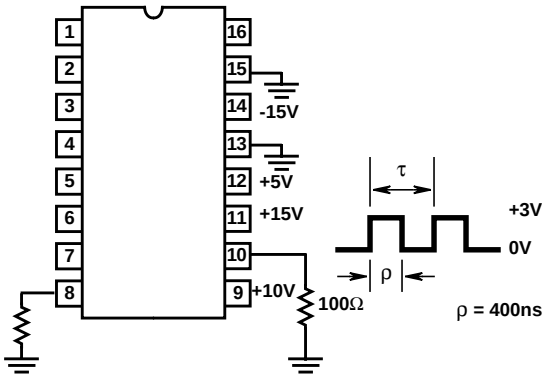


FIGURE 4B.

FIGURE 4. POWER SUPPLY CURRENTS vs LOGIC STROBE RATE

Typical Performance Curves (Continued)

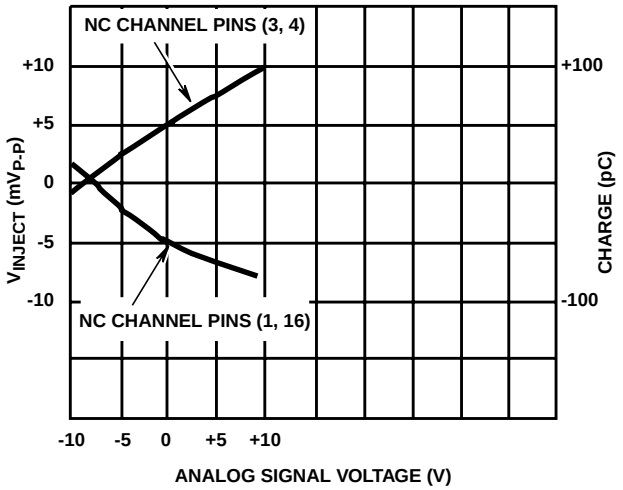


FIGURE 5A.

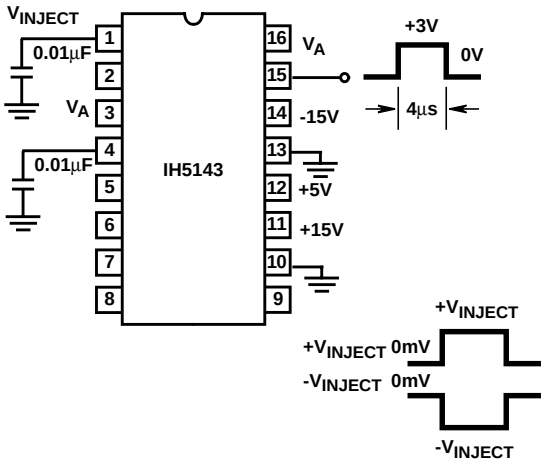


FIGURE 5B.

FIGURE 5. CHARGE INJECTION vs ANALOG SIGNAL

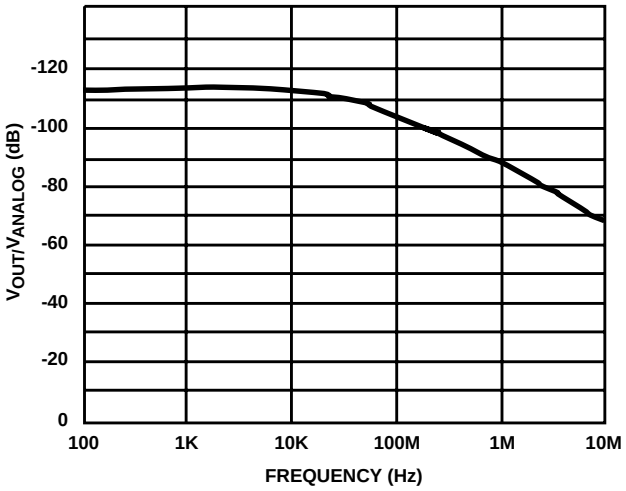


FIGURE 6A.

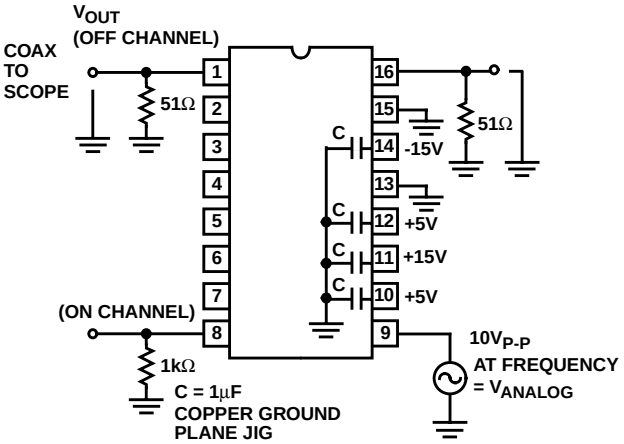


FIGURE 6B.

FIGURE 6. CHANNEL TO CHANNEL CROSS COUPLING REJECTION vs FREQUENCY

Test Circuits and Waveforms

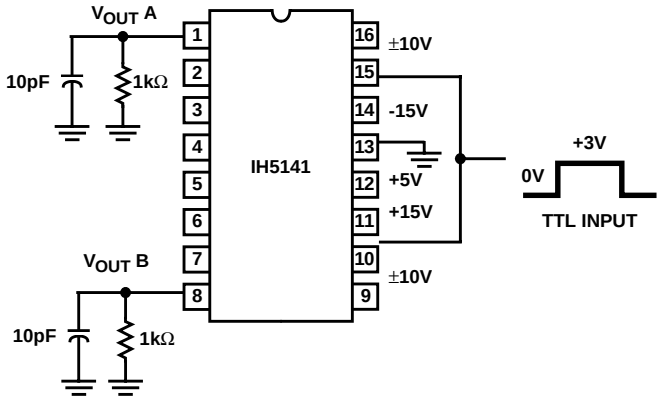
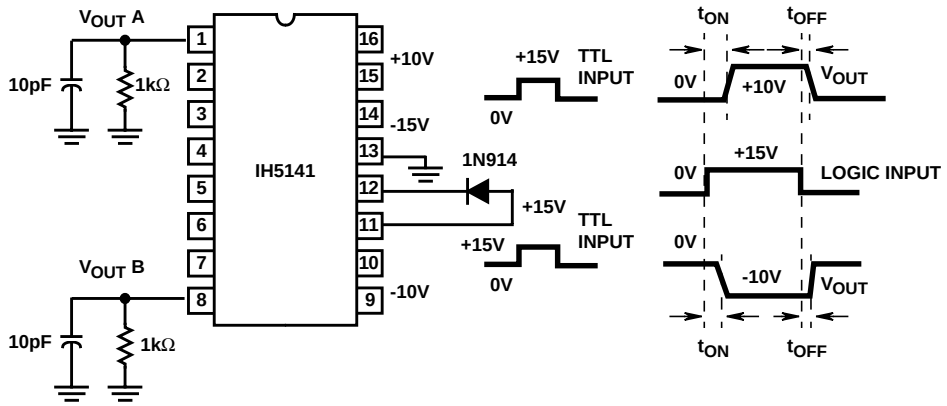


FIGURE 7. IH5141 t_{ON} AND t_{OFF} (3V DIGITAL INPUT)

Test Circuits and Waveforms (Continued)



NOTE: Switching times are measured at 90% points.

FIGURE 8. IH5141 t_{ON} AND t_{OFF} (15V DIGITAL INPUT)

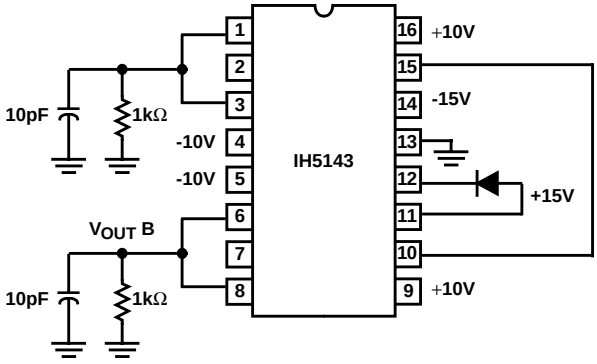


FIGURE 9A.

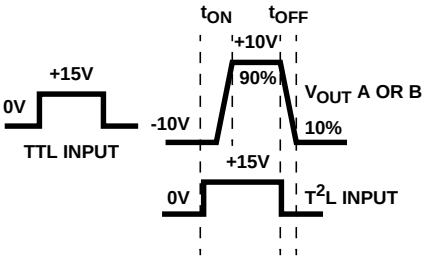


FIGURE 9B.

FIGURE 9. IH5143 t_{ON} AND t_{OFF} (15V DIGITAL INPUT)

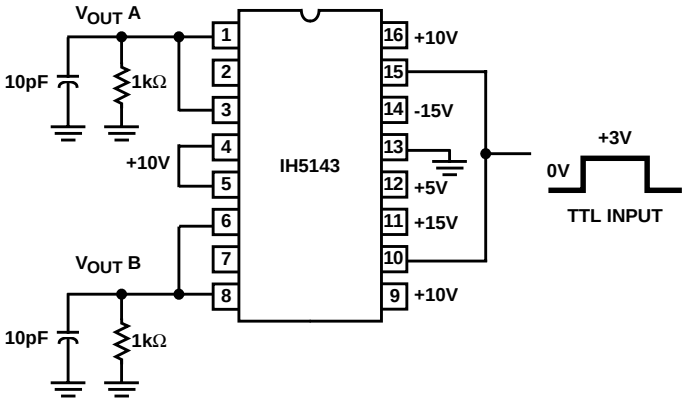


FIGURE 10. IH5143 t_{ON} AND t_{OFF} (3V DIGITAL INPUT)

Typical Applications

To maximize switching speed on the IH5140 family, TTL open collector logic (15V with a 1kΩ or less collector resistor) should be used. This configuration will result in (SPST) t_{ON} and t_{OFF} times of 80ns and 50ns, for signals between -10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both t_{ON} and t_{OFF} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns → 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus t_{ON} is about 105ns, and t_{OFF} 75ns for SPST switches, and 135ns and 105ns (t_{ON}, t_{OFF}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V → +3.0V drive. Pin 13 is taken to -5V instead of the usual GND and strobe input is taken from +5V to -5V levels as shown in Figure 11.

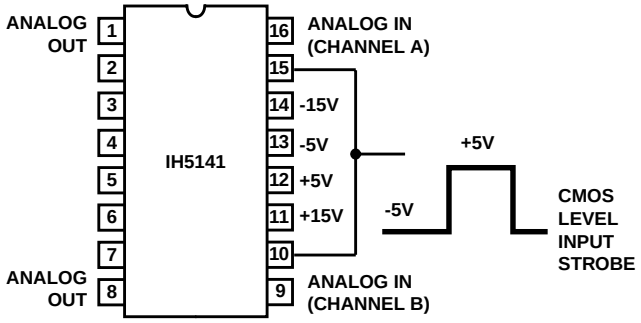


FIGURE 11.

The typical channel of the IH5140 family consists of both P-Channel and N-channel MOSFETs. The N-channel MOSFET uses a "Body Puller" FET to drive the body to -15V (±15V supplies) to get good breakdown voltages when the switch is in the off state (see Figure 12). This "Body Puller" FET also allows the N-Channel body to electrically float when the switch is in the on state producing a fairly constant $r_{DS(ON)}$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 13.

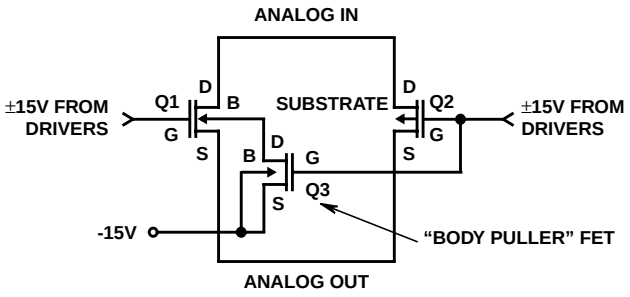


FIGURE 12.

Current will flow from -10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

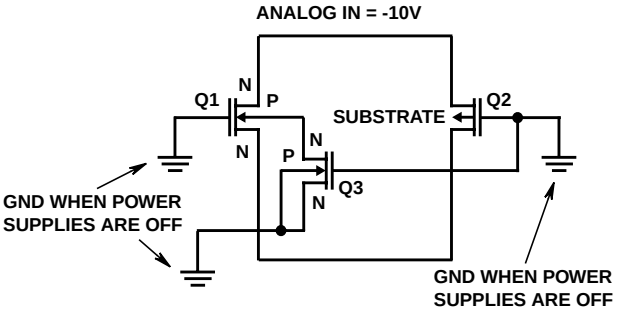


FIGURE 13.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 14. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.

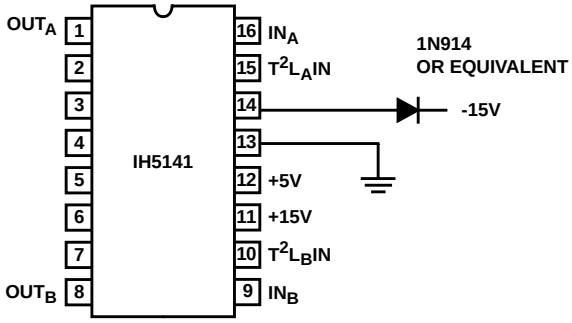


FIGURE 14.

Typical Switching Waveforms

Scale: Vertical = 5V/Div., Horizontal = 100ns/Div.

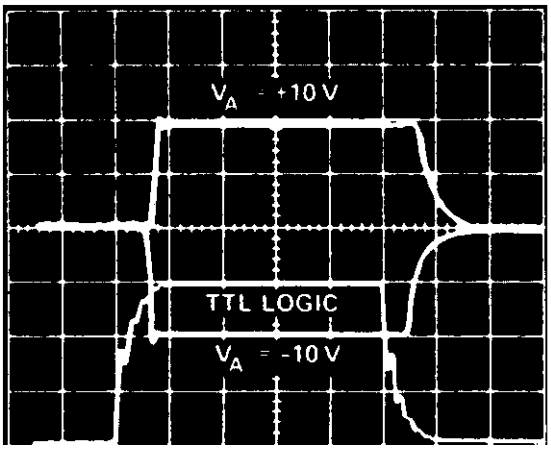


FIGURE 15A. -55°C

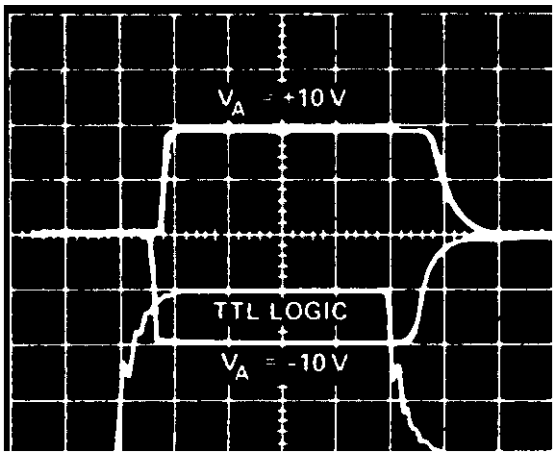


FIGURE 15B. 25°C

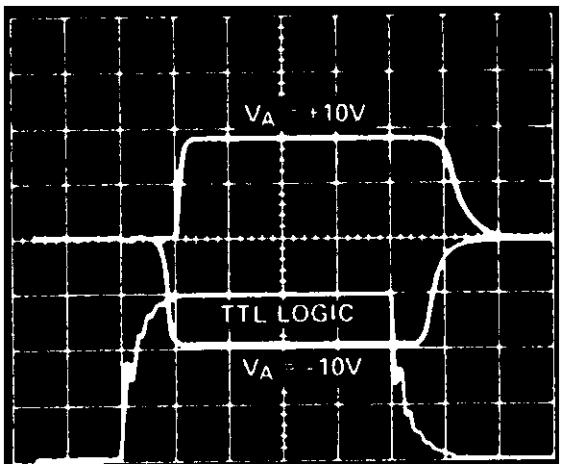


FIGURE 15C. 125°C

NOTE: Corresponds to Figure 12

FIGURE 15. TTL OPEN COLLECTOR LOGIC DRIVE

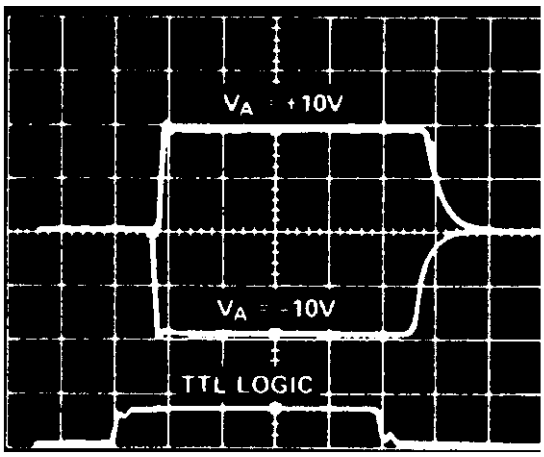


FIGURE 16A. -55°C

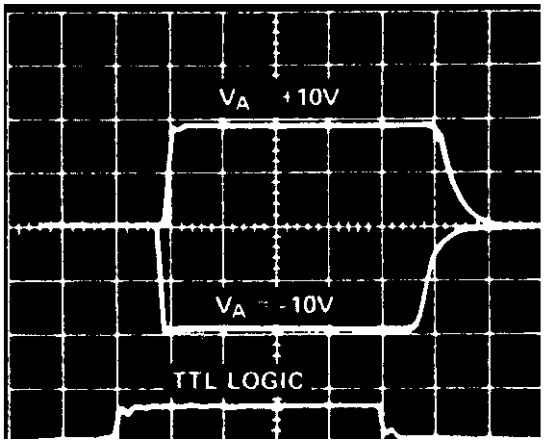


FIGURE 16B. 25°C

Typical Switching Waveforms

Scale: Vertical = 5V/Div., Horizontal = 100ns/Div. **(Continued)**

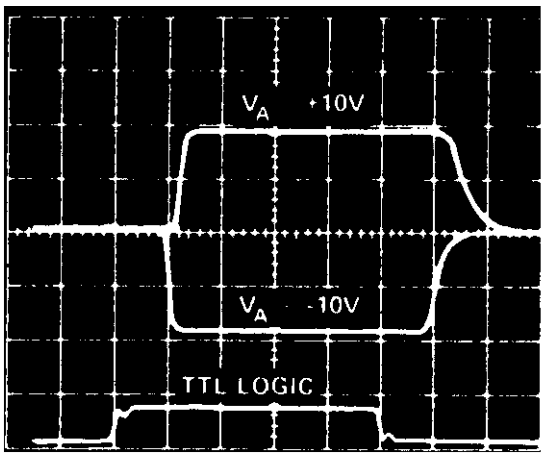
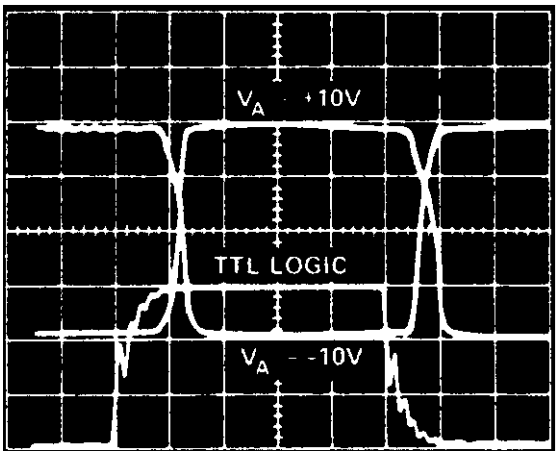


FIGURE 16C. 125°C

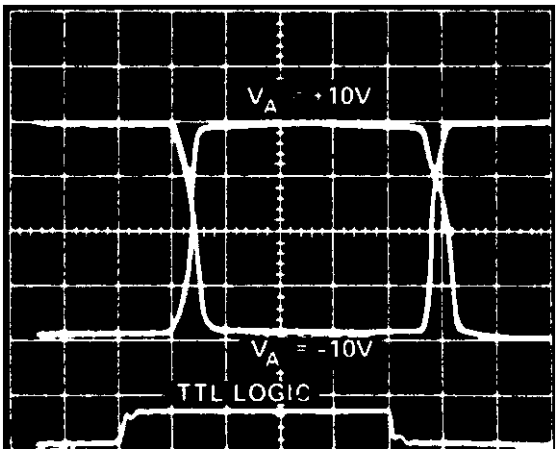
NOTE: Corresponds to Figure 13

FIGURE 16. TTL OPEN COLLECTOR LOGIC DRIVE



NOTE: Corresponds to Figure 14

FIGURE 17. 25°C TTL OPEN COLLECTOR LOGIC DRIVE



NOTE: Corresponds to Figure 19

FIGURE 18. 25°C TTL OPEN COLLECTOR LOGIC DRIVE

Typical Applications

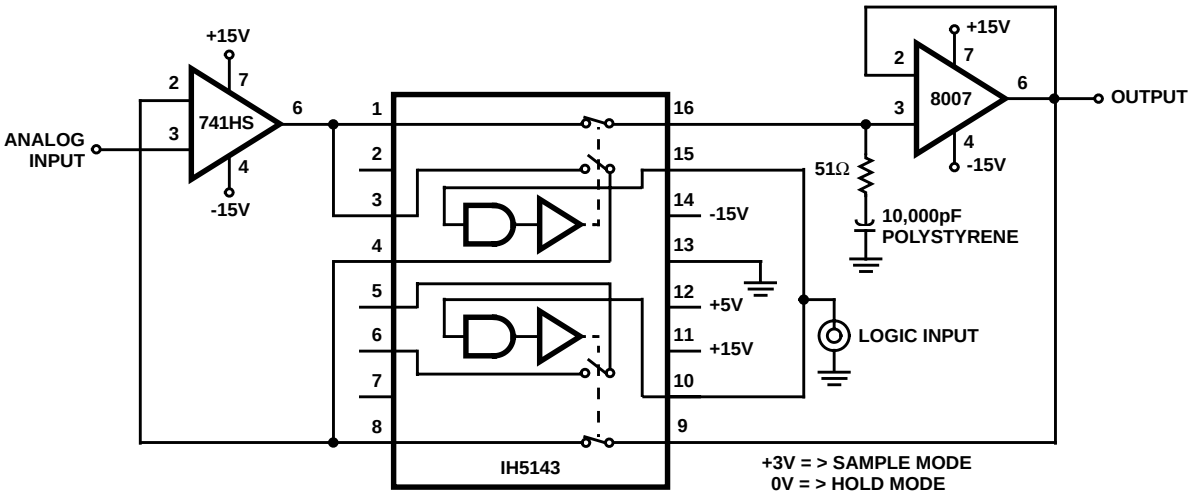


FIGURE 19. FIGURE 19. IMPROVED SAMPLE AND HOLD USING IH5143

Typical Applications (Continued)

EXAMPLE: If $-V_{ANALOG} = -10V_{DC}$ and $+V_{ANALOG} = +10V_{DC}$ then Ladder Legs are switched between $\pm 10V_{DC}$, depending upon state of Logic Strobe.

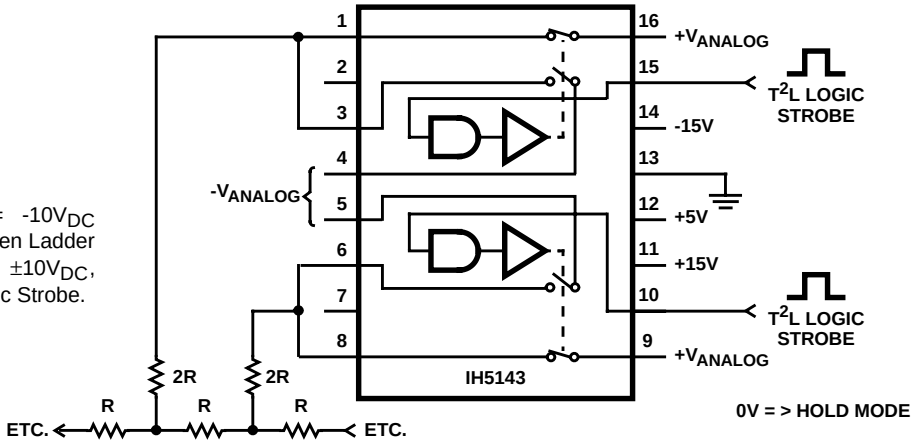
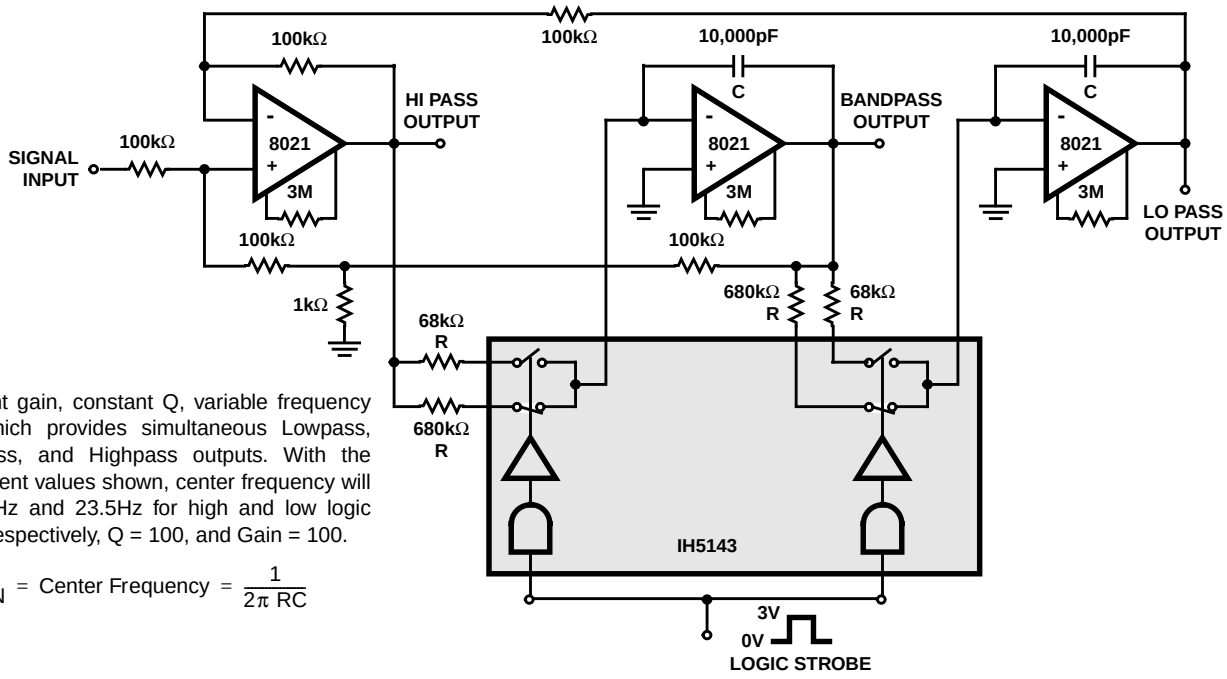


FIGURE 20. USING THE CMOS SWITCH TO DRIVE AN R/2R LADDER NETWORK (2 LEGS)



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_N = \text{Center Frequency} = \frac{1}{2\pi RC}$$

FIGURE 21. DIGITALLY TUNED LOW POWER ACTIVE FILTER