Hex Parallel D Register With Enable

Military 54F378

ELECTRICALLY TESTED PER:
MIL-M-38510/34108

The 54F378 is a 6-Bit register with a buffered common enable. This device is similar to the 'F174, but features the common Enable rather than common Master Reset.

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP. This circuit is designed to prevent false clocking by transitions on the $\overline{E}$ input.

- 6-Bit High-Speed Parallel Register
- Positive Edge Triggered D Type Inputs
- Fully Buffered Common Clock and Enable Inputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Full TTL and CMOS Compatible

AVAILABLE AS:

1) JAN: JM38510/34108BXA
2) SMD: 5962-8855501
3) 883: 54F378/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

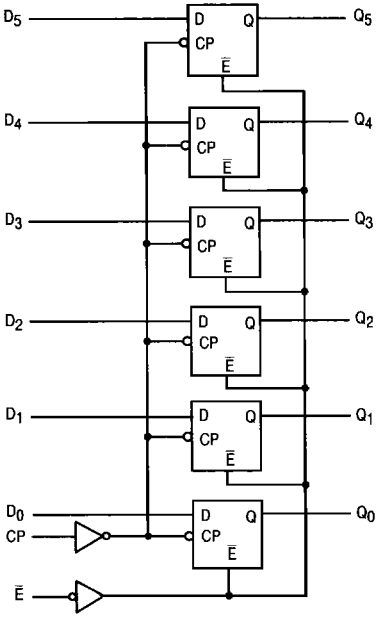
THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{E}$	1	1	2	GND
Q_0	2	2	3	OPEN
D_0	3	3	4	V_{CC}
D_1	4	4	5	V_{CC}
Q_1	5	5	7	OPEN
D_2	6	6	8	V_{CC}
Q_2	7	7	9	OPEN
GND	8	8	10	GND
CP	9	9	12	V_{CC}
Q_3	10	10	13	OPEN
D_3	11	11	14	V_{CC}
Q_4	12	12	15	OPEN
D_4	13	13	17	V_{CC}
D_5	14	14	18	V_{CC}
Q_5	15	15	19	OPEN
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

LOGIC DIAGRAM



Please note that this logic diagram is provided for the understanding of logic operations and should not be used to estimate propagation delays.

TRUTH TABLE

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	⎍⎺	X	No Change
L	⎍⎺	H	H
L	⎍⎺	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
⎍⎺ = Transition from Low to High Level

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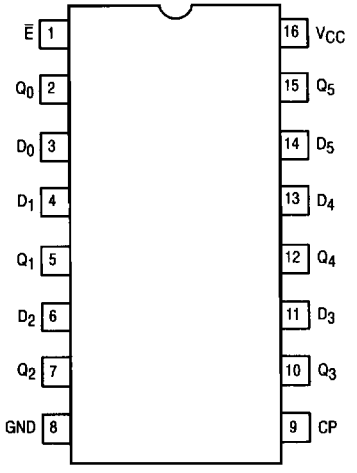
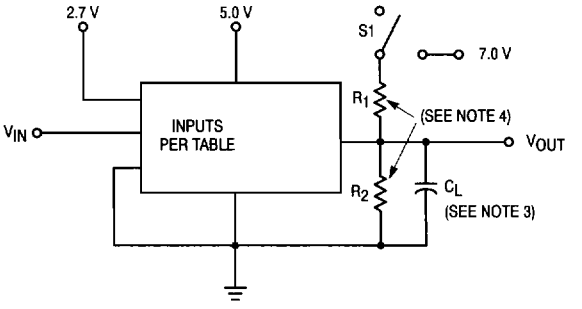
CONNECTION DIAGRAM

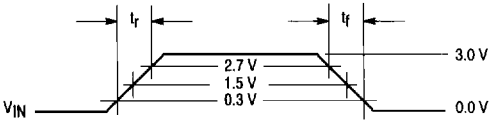


AC TEST CIRCUIT



Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

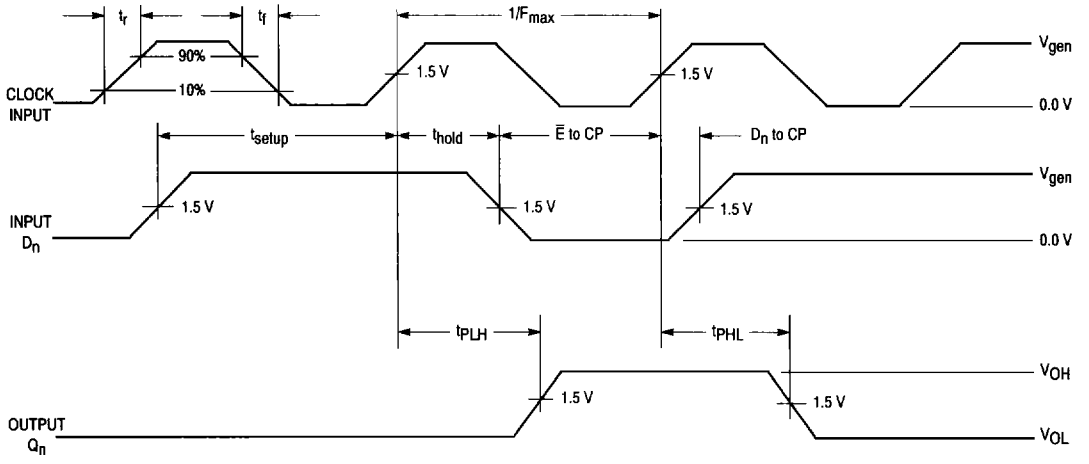
WAVEFORM



NOTES:

1. V_{IN} = Input pulse and has the following characteristics: PRR ≤ 1.0 MHz, $t_r = t_f \leq 2.5$ ns.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. $R_1 = R_2 = 499\ \Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.

WAVEFORMS



NOTES:
1. Clock input pulse has the following characteristics:
   V_{gen} = 3.0 ± 0.2 V, $t_r = t_f \leq$ 2.5 ns and PRR ≤ 1.0 MHz.
2. D input has the following characteristics:
   V_{gen} = 3.0 ± 0.2 V, $\overline{E}$ to CP = t_{setup} = 3.0 ns minimum
   (D_n > CLK), t_{hold} = 1.0 ns minimum, D_n to CP = t_{hold} (D_n > CLK).
3. For f_{MAX} testing, see table.

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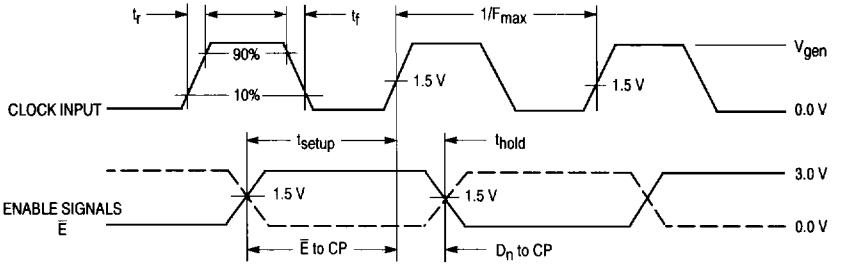

NOTES:
1. Clock input pulse has the following characteristics:
   V_{gen} = 3.0 ± 0.2 V, $t_r = t_f \leq$ 2.5 ns and PRR ≤ 1.0 MHz.
2. Enable characteristics are: $t_{setup} = \overline{E}$ to CP = 6.0 ns ($\overline{E}$ > CP),
   $t_{hold} = D_n$ to CP = 2.0 ns ($\overline{E}$ > CP).

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IN} = 2.0 V (all inputs), $\overline{E}$ = 0.8 V, CP = (See Note 1).
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, $\overline{E}$ = 0.8 V, V_{IN} = 0.8 V, (all inputs), CP = (See Note 1).
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, other inputs are open.
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 4.5 V, V_{IN} = GND (all inputs), $\overline{E}$ = GND, V_{OUT} = 2.5 V, CP = (See Note 1).
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (all inputs) CP = (See Note 1), $\overline{E}$ = GND, V_{OUT} = GND.
I_{CC}	Power Supply Current		45		45		45	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), CP = (See Note 1), $\overline{E}$ = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**). V_{CC} = 5.5 V, V_{INL} = 0.5 V, V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output Output High-Low	3.0	8.5	2.5	10.5	2.5	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ±5.0%.
t_{PLH1}	Propagation Delay /Data-Output Output Low-High	2.5	7.5	2.0	9.5	2.0	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ±5.0%.
f_{MAX}	Maximum Clock Frequency	80		60		60		MHz	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ±5.0%.

NOTES:
1. Apply all voltages, then apply 0 V, 3.0 V, 0 V to clock pulse, then make measurement.
2. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to clock pulse, then make measurement.
3. Apply all voltages, then apply 0 V, 3.0 V to clock pulse, then make measurement.
4. f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.