TC74HC373AP/AF/AFW
TC74HC533AP/AF

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
TC74HC373AP/AF/AFW NON-INVERTING
TC74HC533AP/AF INVERTING

The TC74HC373A and TC74HC533A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HC373A has non-inverting outputs, and TC74HC533A has inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.
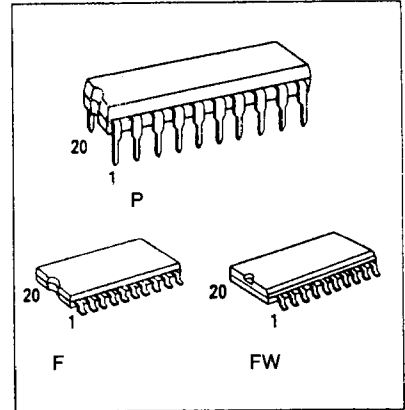
FEATURES:
- High Speed ···························· t_{pd}=11ns(typ.)at V_{CC}=5V
- Low Power Dissipation ············· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ············· V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ·········· 15 LSTTL Loads
- Symmetrical Output Impedance ··· |I_{OH}|=I_{OL}=6mA(Min.)
- Balanced Propagation Delays ······ t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
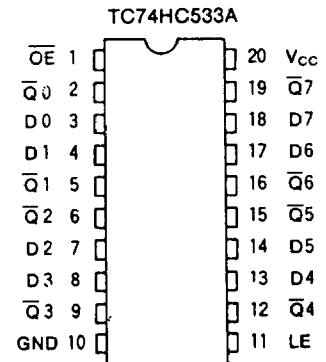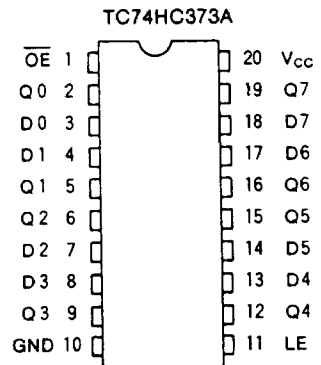- Pin and Function Compatible with 74LS373/533

P

F   FW

PIN ASSIGNMENT

TC74HC373A

$\overline{OE}$	1	20	V_{CC}
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	LE

TC74HC533A

$\overline{OE}$	1	20	V_{CC}
$\overline{Q0}$	2	19	$\overline{Q7}$
D0	3	18	D7
D1	4	17	D6
$\overline{Q1}$	5	16	$\overline{Q6}$
$\overline{Q2}$	6	15	$\overline{Q5}$
D2	7	14	D5
D3	8	13	D4
$\overline{Q3}$	9	12	$\overline{Q4}$
GND	10	11	LE

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HC373A)	$\overline{Q}$(HC533A)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
Q_n ($\overline{Q_n}$) : Q ($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.
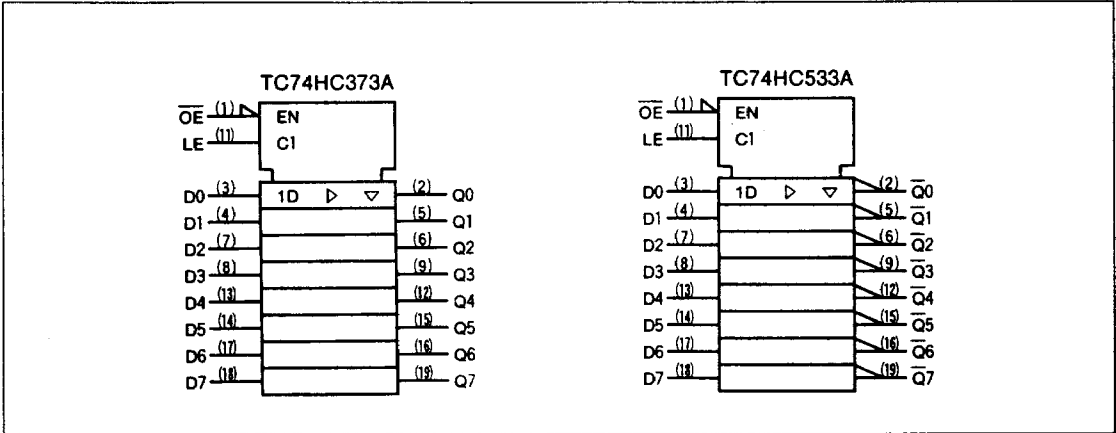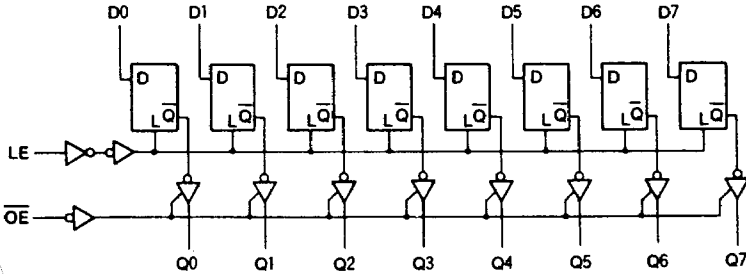
IEC LOGIC SYMBOL

TC74HC373A

OE (1) — EN
LE (11) — C1

D0 (3) — 1D ▷ ▽ — (2) Q0
D1 (4) — (5) Q1
D2 (7) — (6) Q2
D3 (8) — (9) Q3
D4 (13) — (12) Q4
D5 (14) — (15) Q5
D6 (17) — (16) Q6
D7 (18) — (19) Q7

TC74HC533A

OE (1) — EN
LE (11) — C1

D0 (3) — 1D ▷ ▽ — (2) $\overline{Q0}$
D1 (4) — (5) $\overline{Q1}$
D2 (7) — (6) $\overline{Q2}$
D3 (8) — (9) $\overline{Q3}$
D4 (13) — (12) $\overline{Q4}$
D5 (14) — (15) $\overline{Q5}$
D6 (17) — (16) $\overline{Q6}$
D7 (18) — (19) $\overline{Q7}$

SYSTEM DIAGRAM

TC74HC373A

TC74HC533A
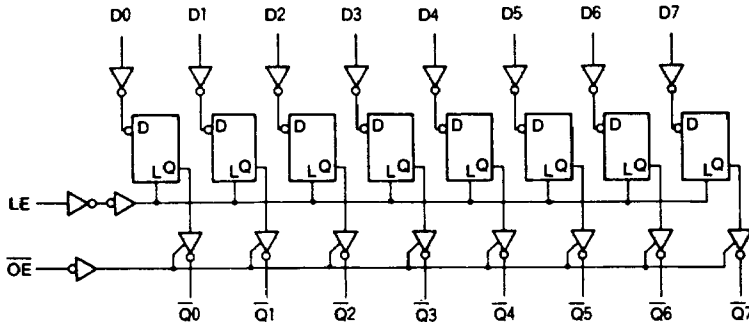
TC74HC373AP/AF/AFW   533AP/AF-2

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)∗/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

∗500mW in the range of Ta=
−40℃∼ 65℃. From Ta=65℃
to 85℃ a derating factor of
−10mW/℃ shall be applied
until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r , t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ∼85℃ MIN.	Ta=−40 ∼85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} =-20\mu A$	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			$I_{OH} =-6$ mA	4.5	4.18	4.31	−	4.13	−	
			$I_{OH} =-7.8$mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} =20 \mu A$	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			$I_{OL} =6$ mA	4.5	−	0.17	0.26	−	0.33	
			$I_{OL} =7.8$mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		−	−	−	4.0	−	40.0	

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TIMING REQUIREMENTS(Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40～85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time (Data)	t_s		2.0	−	50	65	ns
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (Data)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS(Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	42	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	12	21	−	26	
	t_{pHL}		150	2.0	−	57	175	−	220	
				4.5	−	19	35	−	44	
				6.0	−	16	30	−	37	
Propagation Delay Time (D−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	42	125	−	155	ns
				4.5	−	14	25	−	31	
				6.0	−	12	21	−	26	
	t_{pHL}		150	2.0	−	57	175	−	220	
				4.5	−	19	35	−	44	
				6.0	−	16	30	−	37	
Output Enable time	t_{pZL}	$R_L = 1 k\Omega$	50	2.0	−	39	125	−	155	
				4.5	−	13	25	−	31	
				6.0	−	11	21	−	26	
	t_{pZH}		150	2.0	−	54	175	−	220	
				4.5	−	18	35	−	44	
				6.0	−	15	30	−	37 ・	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1 k\Omega$	50	2.0	−	30	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	13	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	
Output Capacitance	C_{OUT}				−	10	−	−	−	pF
Power Dissipation Capacitance	$C_{PD}(1)$				−	38	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$$I_{CC\ (opt)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8(\text{per Latch})$$
And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:
$$C_{PD}(\text{total}) = 22 + 16 \cdot n$$

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