

OVERVIEW

The SM8760CA is a compact clock generator IC with 4-times multiplication clock signal output that has a spread spectrum (SS) function to reduce undesirable EMI radiation. The SM8760CA has built-in crystal oscillator circuit, PLL, and loop filter. It accepts an input clock signal, generated using an external crystal or direct external clock input, and outputs 1 SS-modulated 4-times multiplication clock signal and 1 unmodulated reference signal. In addition, the SM8760CA features control pins to select SS modulation function ON/OFF and power-down modes.

FEATURES

- Spread spectrum clock output to reduce EMI
- Modulation rate: Center spread: $\pm 1.0\%$
- Input frequency
 - Using crystal element connection: 12.75MHz (fundamental frequency)
 - Using external input clock: 12.75MHz
- Multiplication: 4-time multiplication
- Operating supply voltage: $3.3 \pm 0.3V$
- Low jitter: 350ps typ (Cycle-to-Cycle)
- Functions: Power-down function, SS modulation ON/OFF
- Mode control pins: Pull-up resistors built-in
- Package: 8-pin VSOP

APPLICATIONS

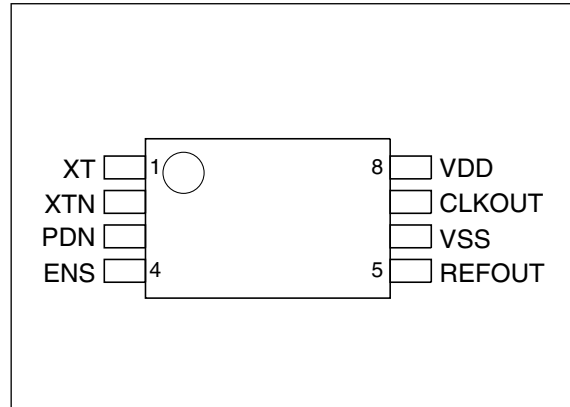
- Printer (laser/inkjet)
- Photocopiers, scanners
- LCD/PDP displays
- Projectors
- Miscellaneous electronic equipment

ORDERING INFORMATION

Device	Package
SM8760CAV	8-pin VSOP

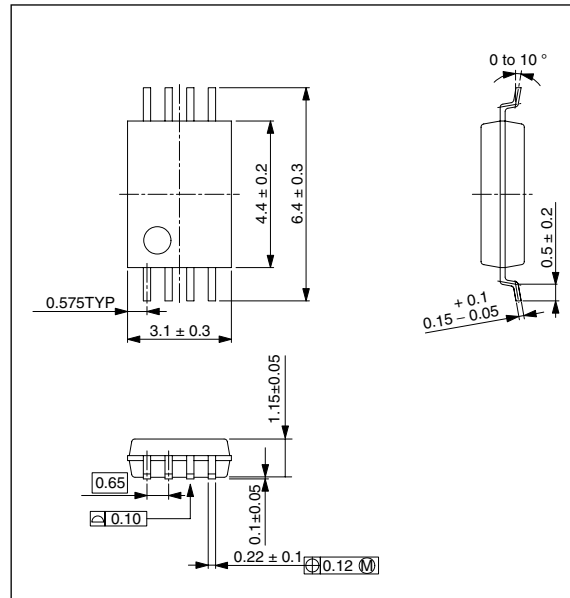
PINOUT

(Top view)

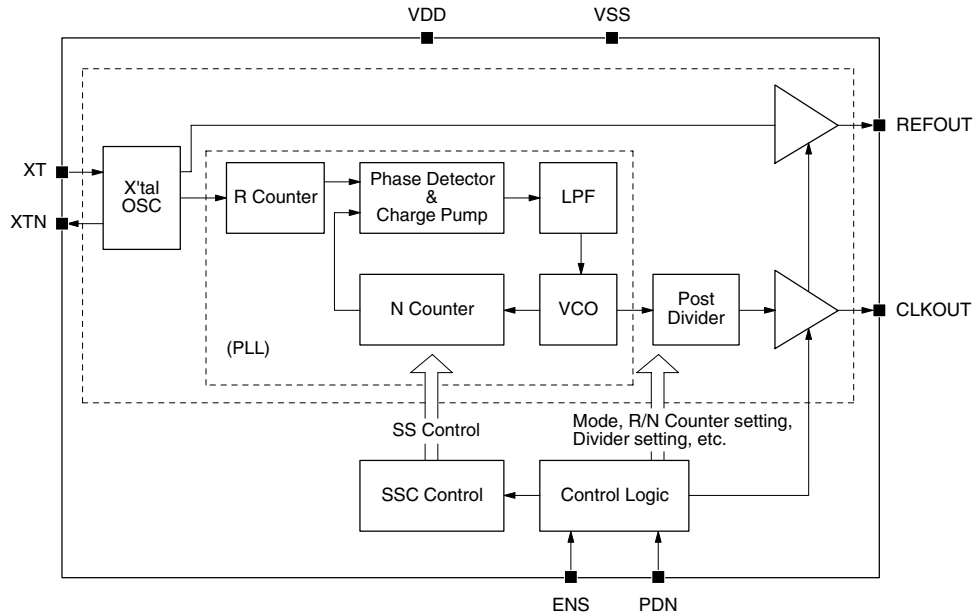


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Function
1	XT	I	Crystal oscillator element connection or external clock input
2	XTN	O	Crystal oscillator element connection
3	PDN	I	Power-down control (with built-in pull-up resistor)
4	ENS	I	SS modulation function ON/OFF (with built-in pull-up resistor)
5	REFOUT	O	Reference clock output
6	VSS	GND	Ground
7	CLKOUT	O	SS clock output
8	VDD	PWR	Supply voltage

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to +6.5	V
Input voltage range	V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Output voltage range	V_{OUT}	-0.3 to $V_{DD} + 0.3$	V
Power dissipation	P_D	150	mW
Storage temperature range	T_{STG}	-55 to +125	°C

Recommended Operating Conditions

$V_{SS} = 0V$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage range	V_{DD}		+3.0	-	+3.6	V
Output load capacitance	C_L	CLKOUT, REFOUT output pins	-	-	15	pF
Master clock frequency	f_{XTAL}	Crystal oscillator element connection	-	12.75	-	MHz
		External clock input	-	12.75	-	
Operating temperature range	T_{OPR}		-20	-	+80	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

$V_{DD} = 3.3 \pm 0.3V$, $V_{SS} = 0V$, $T_a = -20$ to $+80^\circ C$, $f_{XTAL} = 12.75MHz$ unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
Current consumption	I_{DD}	VDD	$V_{DD} = 3.3V$, $T_a = 25^\circ C$, crystal oscillator element connection, all outputs unloaded	-	9	14	mA
Input voltage	V_{IH1}	PDN, ENS	$V_{DD} = 3.3V$	$0.85V_{DD}$	-	-	V
	V_{IL1}			-	-	$0.15V_{DD}$	
	V_{IH2}	XT	$V_{DD} = 3.3V$	$0.80V_{DD}$	-	-	
	V_{IL2}			-	-	$0.20V_{DD}$	
Input current	I_{IH1}	PDN, ENS	$V_{IN} = V_{DD}$, built-in pull-up resistor	-	-	1	μA
	I_{IL1}		$V_{IN} = 0V$, built-in pull-up resistor	-100	-	-	
	I_{IH2}	XT	$V_{IN} = V_{DD}$	-	-	40	
	I_{IL2}		$V_{IN} = 0V$	-40	-	-	
Output voltage	V_{OH}	All outputs excluding XTN pin	$I_{OH} = -2mA$	$V_{DD} - 0.4$	-	-	V
	V_{OL}		$I_{OL} = 2mA$	-	-	0.4	

AC Characteristics

$V_{DD} = 3.3 \pm 0.3V$, $V_{SS} = 0V$, $T_a = -20$ to $+80^\circ C$ unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
Clock frequency	f_{in}	XT	Crystal connection	-	12.75	-	MHz
			External clock input ^{*1}	-	12.75	-	
Output clock rise time ^{*2}	t_r	CLKOUT, REFOUT	$C_L = 15pF$, $V_{OL} = 0.2V_{DD}$ to $V_{OH} = 0.8V_{DD}$ transition time	-	2.0	-	ns
Output clock fall time ^{*2}	t_f	CLKOUT, REFOUT	$C_L = 15pF$, $V_{OH} = 0.8V_{DD}$ to $V_{OL} = 0.2V_{DD}$ transition time	-	2.0	-	ns
Output clock jitter ^{*2}	t_{jitter}	REFOUT	1-sigma jitter, $T_a = 25^\circ C$, $C_L = 15pF$, $V_O = 0.5V_{DD}$	-	25	-	ps
			Peak-to-peak jitter, $T_a = 25^\circ C$, $C_L = 15pF$, $V_O = 0.5V_{DD}$	-	180	-	
		CLKOUT	Cycle-to-cycle jitter, $T_a = 25^\circ C$, $C_L = 15pF$, $V_O = 0.5V_{DD}$	-	350	-	
Output clock duty cycle ^{*2}	Dt	CLKOUT, REFOUT	$T_a = 25^\circ C$, $C_L = 15pF$, $V_O = 0.5V_{DD}$	45	50	55	%
Power-up time ^{*2,*3}	t_p	CLKOUT, REFOUT		-	1	5	ms

*1. When using an external clock input, it is recommended that the clock on XT have 50% duty and V_{DD} level signal amplitude. Note that the input signal voltage must not exceed the absolute maximum rating, otherwise it may cause the device to breakdown.

*2. Measured using the circuit in Figure 1 on the NPC standard evaluation board.

*3. The power-up time is the time from when the supply reaches 3.0V after the supply is turned ON until each output clock reaches its designated frequency to within $\pm 0.1\%$.

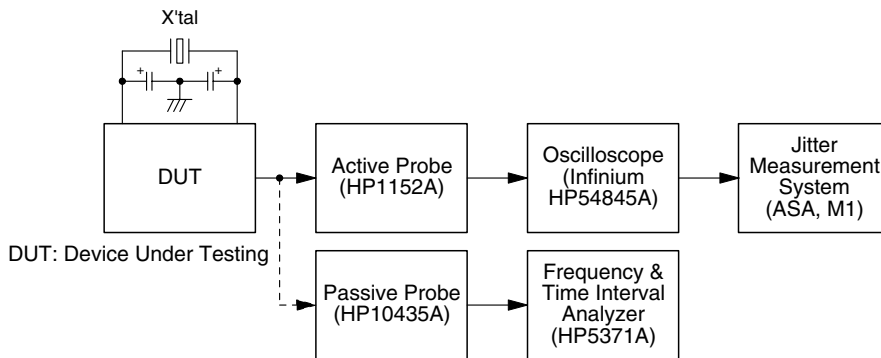


Figure 1. Measurement circuit

FUNCTIONAL DESCRIPTION

Master Clock

The SM8760CA master clock can be generated by the crystal oscillator formed by connecting a crystal (fundamental mode) between XT (pin 1) and XTN (pin 2) as shown in Figure 2. Alternatively, an external master clock can be input directly on XT (pin 1) as shown in Figure 3. If an external clock is input on XT, it is recommended that the clock have 50% duty and V_{DD} level voltage amplitude. Note that the input clock amplitude voltage must not exceed the absolute maximum rating, otherwise it may cause the SM8760CA to breakdown.

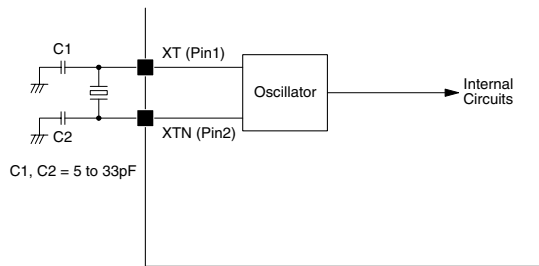


Figure 2. Crystal element connection

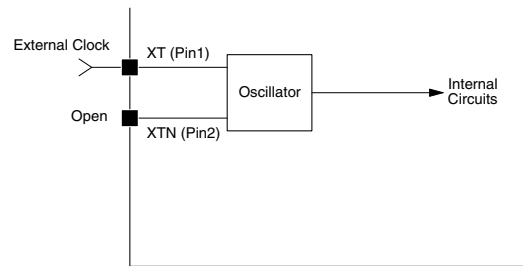


Figure 3. External clock input

Function Controls

The SM8760CA power-down and SS modulation ON/OFF functions are controlled using the PDN and ENS input pins as shown in Table 1.

The power-down function is controlled using the PDN input pin. When PDN (pin 3) is “H”, normal operating mode is selected. When PDN is “L”, power-down mode is selected. In power-down mode, the CLKOUT and REFOUT output pins are in a high impedance state.

The SS modulation function is controlled using the ENS input pin. When ENS (pin 4) is “H”, the SS modulation function is ON, and an SS-modulated clock is output on the CLKOUT pin. When ON, the modulation mode and amplitude is a fixed center spread modulation $\pm 1.0\%$. When ENS is “L”, the SS modulation function is OFF.

Table 1. Function summary

PDN (Pin 3)	ENS (Pin 4)	Power Down	Output (Pin 5, Pin 7)	SS ON/OFF	SS Mode	SS Modulation [%]
H	H	OFF	Clock out	ON	Center spread	± 1.0
H	L			OFF	—	0.0
L	H	ON	Hi-Z	—	—	—
L	L			—	—	—

Note. “H” signal represents V_{DD} level, and “L” represents V_{SS} level.

Typical Connection Circuit

A typical connection circuit diagram is shown in Figure 4.

- 1) The SM8760CA oscillator circuit between XT and XTN has a built-in feedback resistor (approximately 250k Ω).
- 2) The oscillator circuit capacitances C101 and C102 connected to XTN and XT, to match the crystal load capacitor.
- 3) R201 and R202 are impedance matching resistor for board pattern.
- 4) C201 and C202 are bypass capacitors inserted between the supply voltage lines.
 C201 is a 0.1 μ F (approximately) multi-layer ceramic capacitor connected directly alongside the SM8760CA.
 C202 is a 33 μ F (approximately) electrolytic capacitor.

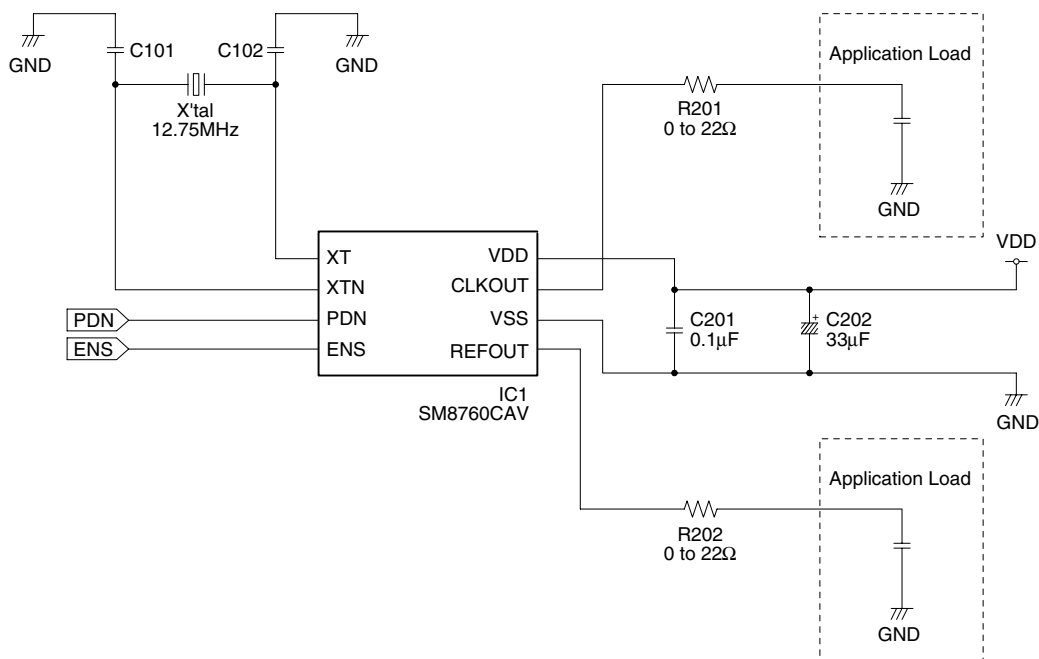
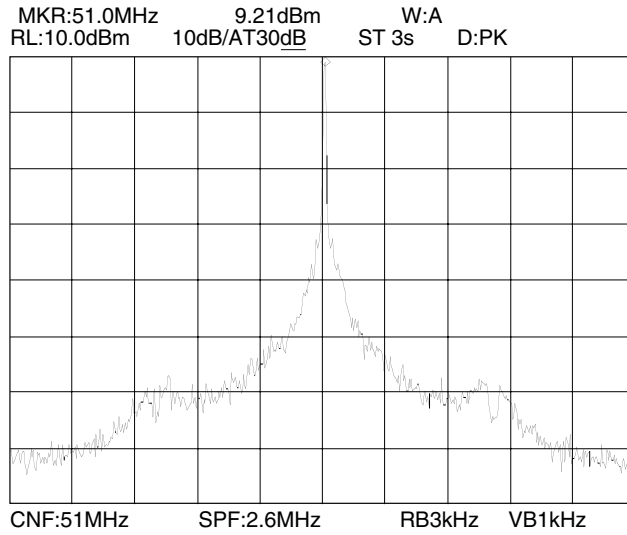


Figure 4. Typical connection circuit

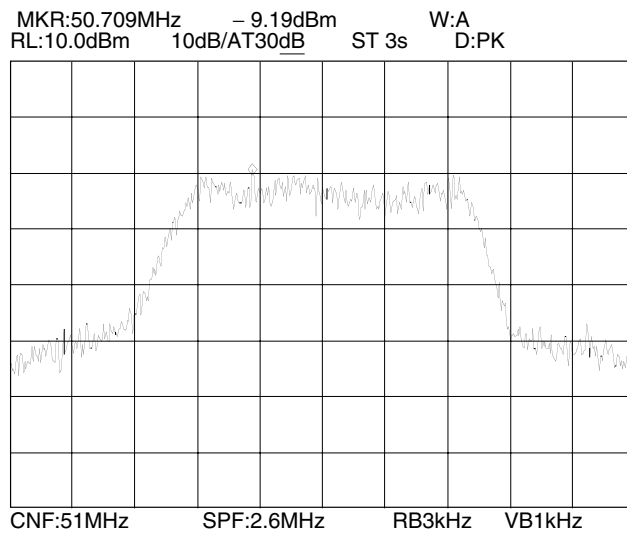
Note. This is a sample connection diagram only, and its use is not a guarantee of SM8760CA device characteristics.

CLKOUT Output Spectrum Sample

A sample SM8760CA CLKOUT output spectrum is shown in Figure 5.



(a) ENS = "L", SS OFF



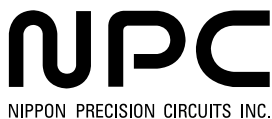
(b) ENS = "H", SS ± 1.0%

Figure 5. Output spectrum sample

Note. These spectrum diagrams were obtained using the NPC evaluation board. These spectrum diagrams are not guaranteed SM8760CA device characteristics.

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