256 × 8-bit CMOS EEPROMs with I²C-bus interface

PC.8582 Family

GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient.

Chip select is accomplished by the three address inputs, which also allows up to eight devices to be connected to the I²C-bus.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, and PCF8581
- Mini-pack package for SMD technology.

QUICK SELECTION GUIDE

TYPE	PCF8582A	PCA8582B	PCF8582C	PCD8582D	PCF8582E
extended temperature range	•	•	•	–	•
extended voltage supply range	–	–	•	•	–
no external RC required	–	–	•	•	•
single bit error correction for extended number of erase/write cycles	–	•	•	•	•

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8582BP	8	DIL	plastic	SOT97
PCA8582BT	16	SO16L	plastic	SOT162A
PCD8582DP	8	DIL	plastic	SOT97
PCD8582DT	8	SO8	plastic	SOT96A
PCF8582AP	8	DIL	plastic	SOT97
PCF8582AT	16	SO16L	plastic	SOT162A
PCF8582CP	8	DIL	plastic	SOT97
PCF8582CT	16	SO16L	plastic	SOT162A
PCF8582EP	8	DIL	plastic	SOT97
PCF8582ET	8	SO8	plastic	SOT96A

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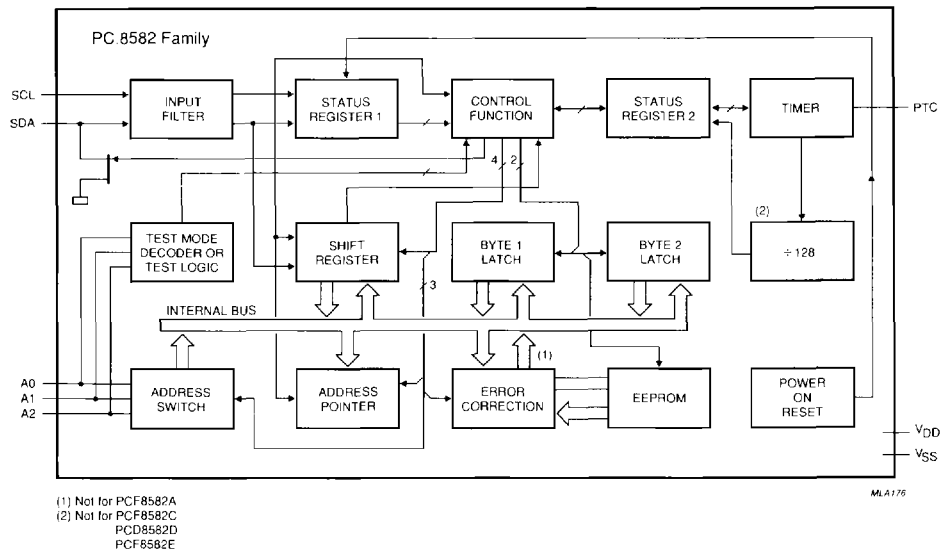


(1) Not for PCF8582A
(2) Not for PCF8582C
PCD8582D
PCF8582E

Fig.1 Block diagram.

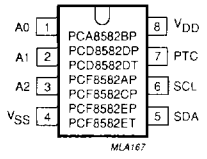


Fig.2 Pin configuration (SOT96A and SOT97).

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
A2	3	address input
V_{SS}	4	ground
SDA	5	serial data
SCL	6	serial clock
PTC	7	can be connected to V_{DD} or left open-circuit
V_{DD}	8	positive supply voltage

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is a bidirectional, 2-line communication between different ICs or modules. The two lines are for serial data (SDA) and serial clock (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- data transfer may be initiated only when the bus is not busy.
- during data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

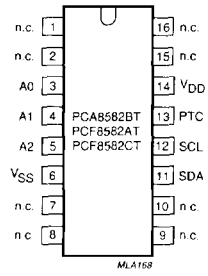


Fig.3 Pin configuration (SOT162A).

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
A0	3	address input
A1	4	address input
A2	5	address input
V_{SS}	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
SDA	11	serial data
SCL	12	serial clock
PTC	13	can be connected to V_{DD} or left open-circuit
V_{DD}	14	positive supply voltage
n.c.	15	not connected
n.c.	16	not connected

By definition a device that sends a signal is called a "transmitter" and the device which receives the signal is called a "receiver". The device which controls the signals is called the "master". The devices that are controlled by the master are called "slaves".

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.

The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

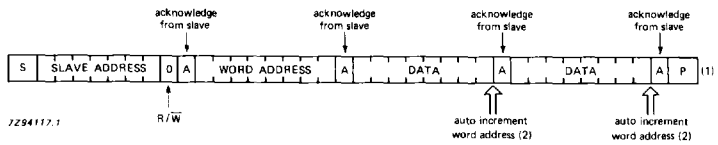
Set up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

(1)

(1) Detailed specifications of the I²C-bus are available on request.

I²C-bus protocol

The I²C-bus configuration for different READ and WRITE cycles of the EEPROM are shown in Figures 4, 5 and 6.



(1) After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to ERASE/WRITE more than two bytes.

Fig.4 Master transmitter transmits to EEPROM slave receiver (ERASE/WRITE mode).

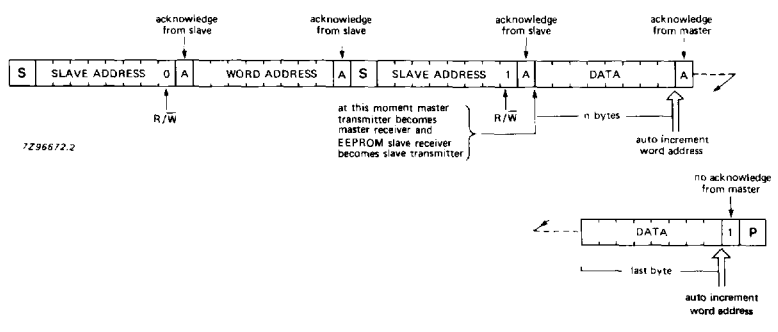


Fig.5 Master reads EEPROM slave after setting word address (write word address; READ data).

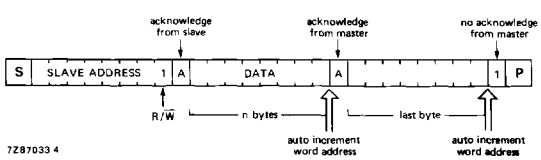


Fig.6 Master reads EEPROM slave immediately after first byte (READ mode). Write protection can be achieved by connecting pin PTC to V_{DD} (for PCF8582A and PCA8582B only).

The slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/W

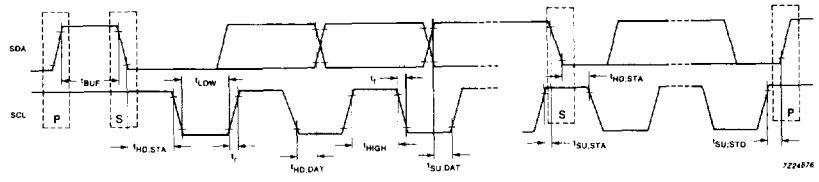


Fig.7 I²C-bus timing.

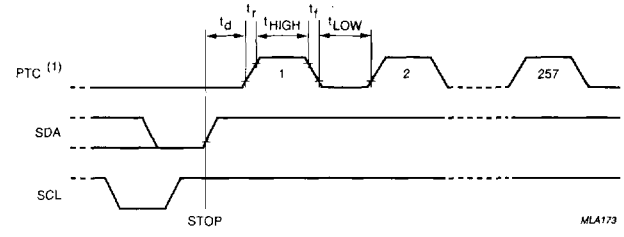


Fig.8 One byte ERASE/WRITE cycle.

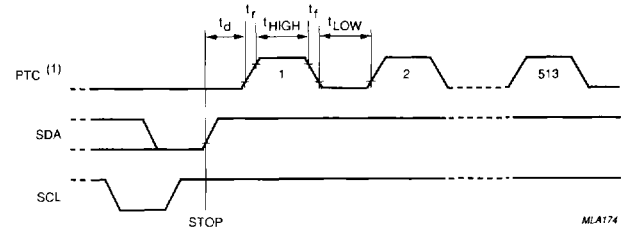
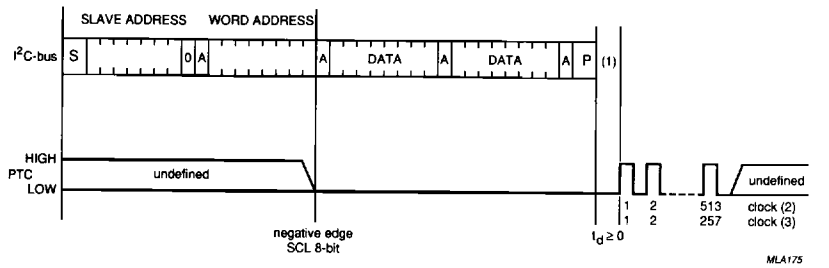


Fig.9 Two byte ERASE/WRITE cycles.



(1) If an external clock is chosen, this information is latched internally by leaving pin PTC LOW after transmission of the eigth bit of the word address (negative edge of SCL). The state of pin 7 then, may be previously undefined.

(2) 2 byte programming

(3) 1 byte programming

Fig.10 External clock.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input	$\|Z_I\| > 500\ \Omega$	V_{SS}−0.8	V_{DD} + 0.8	V
I_I	current on any input pin		-	1	mA
I_O	output current		-	10	mA
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range				
	PCF8582A/C/E		−40	+85	°C
	PCA8582B		−40	+125	°C
	PCD8582D		−25	+70	°C

CHARACTERISTICS

PCF8582A; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C
PCA8582B; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +125 °C
PCF8582C; V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C
PCD8582D; V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C
PCF8582E; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage					
	PCF8582A/E, PCA8582B		4.5	-	5.5	V
	PCF8582C		2.5	-	6.0	V
	PCD8582D		3	-	6	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
	PCF8582A	$V_{DD(max)}$	–	–	0.4	mA
	PCA8582B	$V_{DD(max)}$	–	–	0.8	mA
	PCF8582C/PCD8582D	V_{DD} = 3 V	–	–	0.25	mA
		V_{DD} = 6 V	–	–	1.6	mA
	PCF8582E	$V_{DD(max)}$	–	–	1.6	mA
$I_{DDE/W}$	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
	PCF8582A/PCA8582B	$V_{DD(max)}$	–	–	2	mA
	PCF8582C/PCD8582D	V_{DD} = 3 V	–	–	0.35	mA
		V_{DD} = 6 V	–	–	2.5	mA
	PCF8582E	$V_{DD(max)}$	–	–	2.5	mA
I_{stb}	supply current STANDBY					
	PCF8582A	$V_{DD(max)}$	–	–	10	µA
	PCA8582B	$V_{DD(max)}$	–	–	20	µA
	PCF8582C/PCD8582D	V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA
	PCF8582E	$V_{DD(max)}$	–	–	10	µA
PTC input (PCF8582A/PCA8582B)						
V_{IH}	input voltage HIGH		V_{DD}−0.3	–	V_{DD} + 0.8	V
V_{IL}	input voltage LOW		−0.8	–	V_{SS} + 0.3	V
PTC input (PCF8582C/PCD8582D/PCF8582E)						
V_{IH}	input voltage HIGH		0.9 V_{DD}	–	V_{DD} + 0.8	V
V_{IL}	input voltage LOW		−0.8	–	0.1 V_{DD}	V
SCL input						
V_{IH}	input voltage HIGH					
	PCF8582A/PCA8582B		3	–	V_{DD} + 0.8	V
	PCF8582C/PCD8582D/PCF8582E		0.7 V_{DD}	–	V_{DD} + 0.8	V
SDA input/output						
V_{IL}	input voltage LOW					
	PCF8582A/PCA8582B		−0.3	–	1.5	V
	PCF8582C/PCD8582D/PCF8582E		−0.8 V_{DD}	–	0.3 V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 3 mA				
	PCF8582A/PCA8582B	V_{DD} = 4.5 V	–	–	0.4	V
	PCF8582C	V_{DD} = 2.5 V	–	–	0.4	V
	PCD8582D	V_{DD} = 3 V	–	–	0.4	V
	PCF8582E	$V_{DD(min)}$	–	–	0.4	V
I_{LO}	output leakage current	V_{OH} = V_{DD}	–	–	1	µA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	–	–	1	µA
Data retention time						
t_S	data retention time	T_{amb} = 55 °C	10	–	–	yrs

WRITE CYCLE LIMITS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{EW}	ERASE/WRITE cycle time				
	PCF8582A/PCA8582B		5	40	ms
	PCF8582C/PCD8582D/PCF8582E		5	25	ms
Endurance					
N_{EW}	ERASE/WRITE cycles per byte				
	PCF8582A		–	10000	
	PCA8582B	T_{amb} = 125 °C; t_{EW} = 5 to 40 ms	–	50000	
		T_{amb} = 85 °C; t_{EW} = 5 to 40 ms	–	100000	
		T_{amb} = 33 °C; t_{EW} = 10 ms	-	500000	
	PCF8582C	T_{amb} = 85 °C; t_{EW} = 5 to 25 ms	–	100000	
		T_{amb} = 33 °C; t_{EW} = 10 ms	–	500000	
	PCD8582D	T_{amb} = –25 to +70 °C; t_{EW} = 5 to 25 ms	–	10000	
		T_{amb} = 0 to +40 °C; t_{EW} = 10 ms	–	100000	
	PCF8582E	T_{amb} = –40 to +85 °C; t_{EW} = 5 to 25 ms	–	100000	

I²C-BUS CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{SCL}	clock frequency		0	-	100	kHz
C_I	input capacitance (SDA; SCL)	$V_I = V_{SS}$	-	-	7	pF
t_{BUF}	time the bus must be free before new transmission can start		4.7	-	-	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4	-	-	µs
t_{LOW}	clock period LOW		4.7	-	-	µs
t_{HIGH}	clock period HIGH		4	-	-	µs
$t_{SU;STA}$	set up time for start condition	repeated start	4.7	-	-	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	-	-	µs
$t_{HD;DAT}$	data hold time for bus devices	note 1	0	-	-	ns
$t_{SU;DAT}$	data set up time		250	-	-	ns
t_r	SDA and SCL rise time		-	-	1	µs
t_f	SDA and SCL fall time		-	-	300	ns
$t_{SU;STO}$	set up time for stop condition		4.7	-	-	µs

Note

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

I²C

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

E/W programming time control

Using external resistor R_{EW} and capacitor C_{EW} (see Table 1).

Table 1 Recommended R_{EW} and C_{EW} combinations (PCF8582A/PCA8582B only).

R_{EW} (kΩ)	C_{EW} (nF)	T_{EW} (typ.) (ms)
56	3.3	34
56	2.2	21
22	3.3	13
22	2.2	7.5

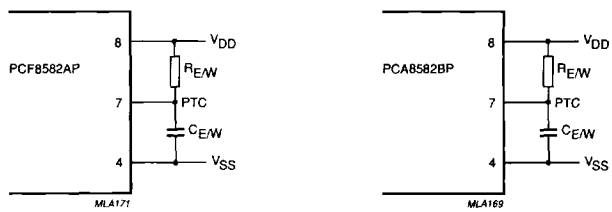


Fig.11 PTC circuit connections to PCF8582AP/PCA8582BP when using the internal oscillator.

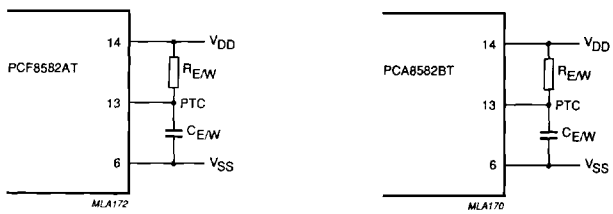


Fig.12 PTC circuit connections to PCF8582AT/PCA8582BT when using the internal oscillator.

Using external clock (see Table 2 and Figs 8, 9 and 10).

Table 2 E/W programming time control using an external clock.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
f_{CLK}	frequency	10	50	kHz
t_{LOW}	clock period LOW	10	-	µs
t_{HIGH}	clock period HIGH	10	-	µs
t_r	rise time	-	300	ns
t_f	fall time	-	300	ns
t_d	delay time	0	t_{LOW}	µs

USING AN INTERNAL OSCILLATOR

When using an internal oscillator t_{EW} has a minimum value of 5 ms and a maximum value of 25 ms; a typical value is 10 ms.