PRELIMINARY

MX8335

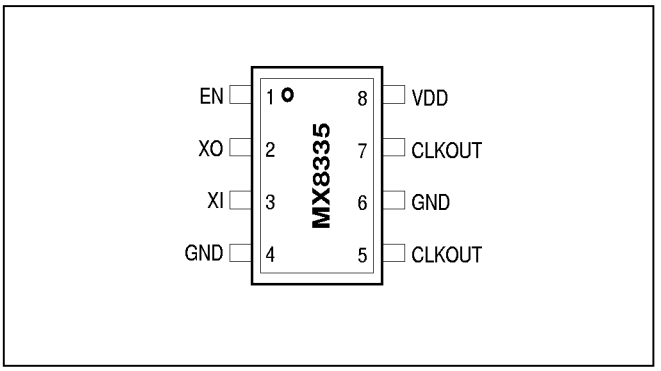
RAM BUS CLOCK GENERATOR

FEATURES

- Clock generator for Rambus™ Channel
- Provide two Rambus interface-level outputs with frequency from 200MHz to 267MHz
- Multiplication ratio 40/3 allows low cost crystal used as frequency reference
- Provide chip output enable pin (EN) for tri-state control
- 3.0V~3.6V power supply range
- 8-pin SOP (150mil) package

PIN CONFIGURATIONS

8-PIN SOP



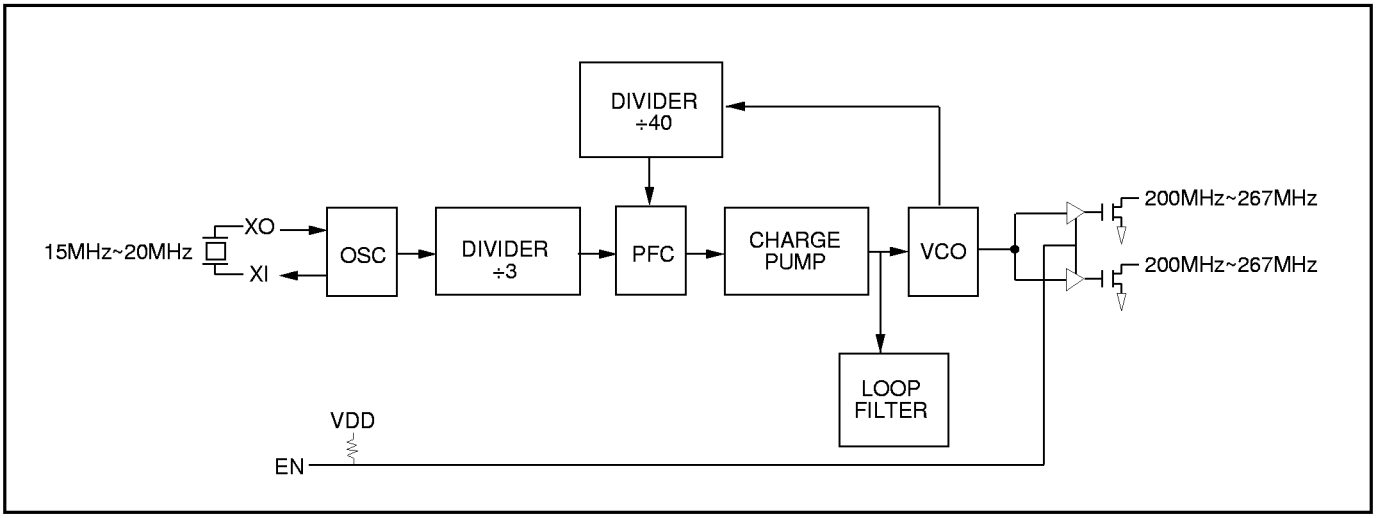
GENERAL DESCRIPTION

The MX8335 is a clock synthesizer chip for Rambus channel. With an advanced phase locked loop technology, the MX8335 provides two clock outputs (CLKOUT) with frequency ranging from 200MHz to 267MHz. The desired high speed clock is the 40/3 Multiplication ratio of a reference input clock. The reference clock could be supplied by an external crystal ranging from 15MHz to 20MHz.

PIN DESCRIPTION

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
EN	I	1	When high, CLKOUTs are enabled. When low, CLKOUTs are tristate. With an internal pull high resistor.
XO	O	2	Crystal output pin.
XI	I	3	Crystal input pin.
GND		4	Ground.
CLKOUT	O	5	200-267Mhz output.
GND		6	Ground.
CLKOUT	O	7	200-267Mhz output.
VDD		8	Power supply.

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The Rambus clock generator is an integrated circuit of the phase locked loop frequency synthesizer. It provides two clock outputs for dual Rambus channel systems.

As shown in the block diagram, a phase locked loop consists of dividers, phase frequency comparator(PFC), charge pump, voltage controlled oscillator(VCO), and loop filter. All components for PLL are integrated inside the chip.

The dividers provide a fixed multiplication ratio 40/3. When a reference clock, ranging from 15MHz to 20MHz and either coming from crystal or external system reference, provides to PLL, the clock outputs should fall in the range of 200-266.67MHz. Following examples shows the relationship between input and output frequencies:

Reference Frequency	Output Frequency
15MHz	200MHz
18.75MHz	250MHz
20MHz	266.67MHz

FREQUENCY REFERENCE

The internal reference oscillator includes all passive components required. A proper resonant crystal should be connected between XO and XI. To minimize the noise pick up, maintain short lead lengths between the crystal and the MX8335 by soldering the crystal to the ground plane. The lead length of the capacitor should be kept to minimum to reduce noise suscepibility. The reference clock can also be supplied by external clock signal. In this case, the reference clock should connected to XI and XO should be unconnected.

POWER SUPPLY CONDITIONING

Clock jittering is the undesirable variations in frequency and phase of a clock source. In PLL, there are many clock jitter sources, such as flicker and thermal noise in electronic element, electromagnetic coupling, power supply noise, signal reflection, ground bounce, physical vibration and variation in temperature and humidity.

Among these noise factors, the power supply noise and ground bounce are most crucial and should be given special care. To eliminate the supply noise, it is judicious to decouple the power noise as shown in Fig. 1, where C1=0.01uF, C2=0.1uF, and C3=47uF.

OUTPUT CIRCUITRY

The clock source output is an open drain NMOS transistor. The MX8335 enables and disables the NMOS transistor alternately to drive the output load. The biasing circuity for the MX8335 is shown in Fig. 1.

Output high voltage is determined by the Vt voltage. To set a value for output low voltage, we must determine the Rs and Rt values. Rt is determined by system operating conditions, which may be ranging from 25 Ohms to 50 Ohms. Rs can be acquired by following equation:

Rs=(Rt x Vt/Vs)-(Rt+Ro)

Ro=On resistor of NMOS transistor

Vs=Signal Swing

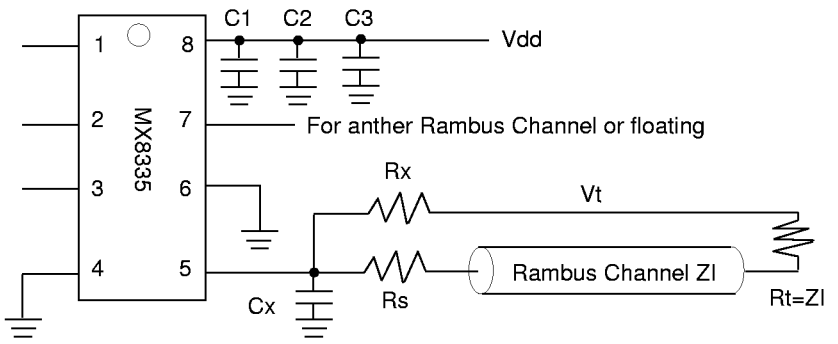
For a system with Vt=2.5V, Rt=25 Ohms, Vs=1.4V, and the MX8335's Ro=10 Ohms

Rs=(25 x 2.5/1.4)-(25+10)=9.6 Ohms

Cx capacitor can help equalize rising and falling rate. Rx resistor helps decrease the rising time. Both Rx and Cx depend on Rt+Rs and PCB layout. Typical values of Rx and Cx for 25 Ohms line impedance are ∞ Ohms and 4pF respectively. For 50 Ohms line impedance, Rx is about 100 Ohms, and Cx is about 2pF. Special care must be taken during physical design of the output bias circuits and the Rambus channel.

Rx, Cx, and Rs should be as close to the MX8335 as possible, and are prefered to use SMD devices. The signal path must be built using controlled impedence transmission line technique.

FIG. 1 INTERFACE CIRCUITRY



ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Storage Temperature	-85°C to 150°C
Applied Input Voltage	-0.5V to VDD + 0.5V
Applied Output Voltage	-0.5V to VDD + 0.5V
Supply Voltage	-0.5V to 5V
Operating Temperature	0 to 70°C
Power Dissipation	0.5Watts

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VDD = 3.0 V to 3.6 V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VIL	Input Low Voltage			0.8	V	
VIH	Input High Voltage	2.4			V	
IIL	Input Low Current			-5	uA	
IIH	Input High Current			5	uA	
IVDD	VDD Current	30	35	40	mA	
CI	Input Capacitance			10	pF	
ZL	Line Impedence	25		50	Ohm	Rambus Level
VLT	Line Termination Voltage	2.2		2.7	V	Rambus Level
IOH	Output High Current	-10		10	uA	CLKOUT
IOL	Output Low Current	40	50		mA	VOL=0.4V, CLKOUT
Ro	Output Resistance	5	10	15	Ohm	CLKOUT

AC CHARACTERISTICS TA = 0°C to 70°C, VDD = 3.0 V to 3.6 V, Note 1

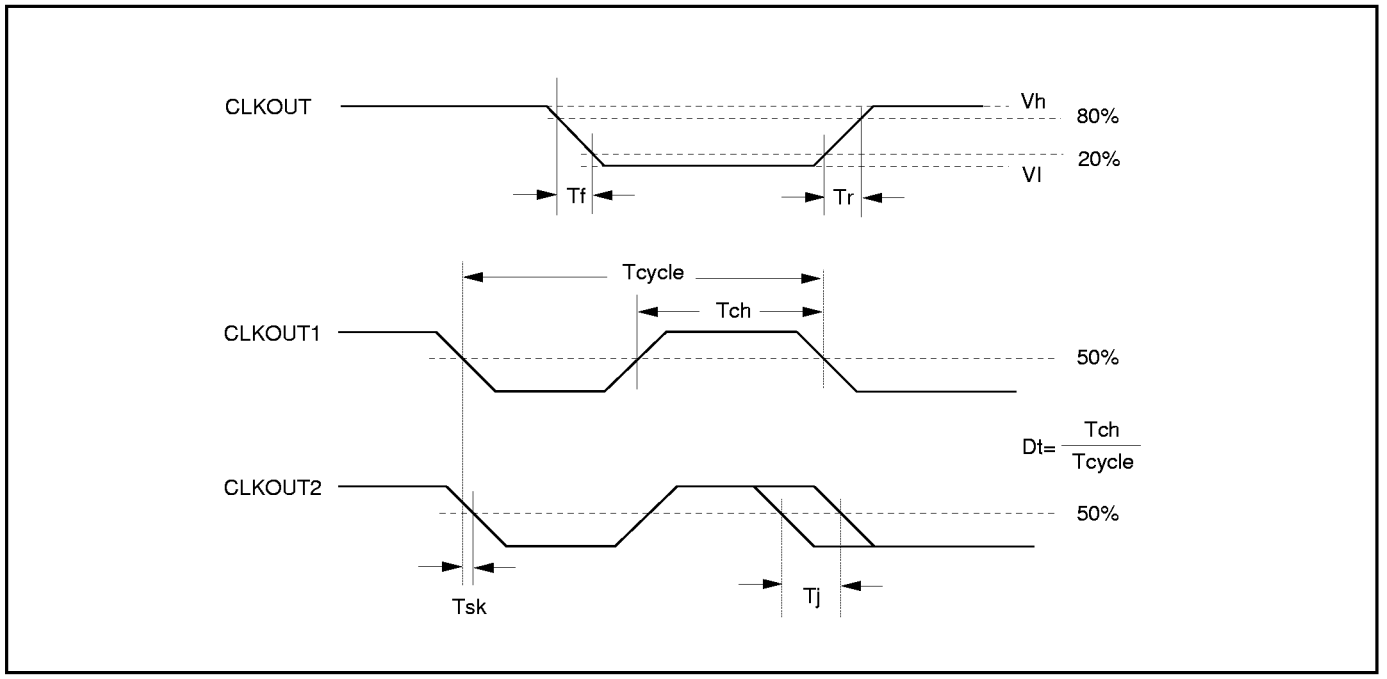
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Dt	Duty Cycle		50		%	CLKOUT
Tj	Jitter (peak to peak)			150	pS	CLKOUT, over 3 clock cycles
Tr/Tf	Rise/Fall Time	0.3		0.5	nS	CLKOUT
Tst	Clock stabilization		5		mS	1. After power is stable 2. Frequency from 0 to 266.67MHz
Aco	Ouput asymmetry		TBD			
Tsk	Output skew between two channels			50ps		Equal loading

Note1: The MX8335 parts are tested under 266.67MHz and triggered at falling edge.

ORDERING INFORMATION

PART NO.	PACKAGE
MX8335MC	8-PIN SOP

WAVE FROMS



PACKAGE INFORMATION

8-PIN PLASTIC SOP (150 mil)

ITEM	MILLIMETER	INCHES
A	4.95 MAX.	.195 MAX.
B	.53 [REF]	.021 [REF]
C	1.27 [TP]	.050 [TP]
D	.41 [TYP.]	.016 [TYP.]
E	.10 MIN.	.004 MIN.
F	1.73 MAX.	.068 MAX.
G	1.45 ± .13	.057 ± .005
H	5.99 ± .3	.236 ± .012
I	3.91 ± .13	.154 ± .005
J	1.02	.040
K	.20 [TYP.]	.008 [TYP.]
L	.76	.030

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.