

**Document Title**

**128Kx36 & 256Kx18 Synchronous Pipelined SRAM**

**Revision History**

<b><u>Rev.No.</u></b>	<b><u>History</u></b>	<b><u>Draft Date</u></b>	<b><u>Remark</u></b>
0.0	- Preliminary specification release	Mar. 1999	Preliminary
1.0	- Final specification release	Nov. 1999	Final

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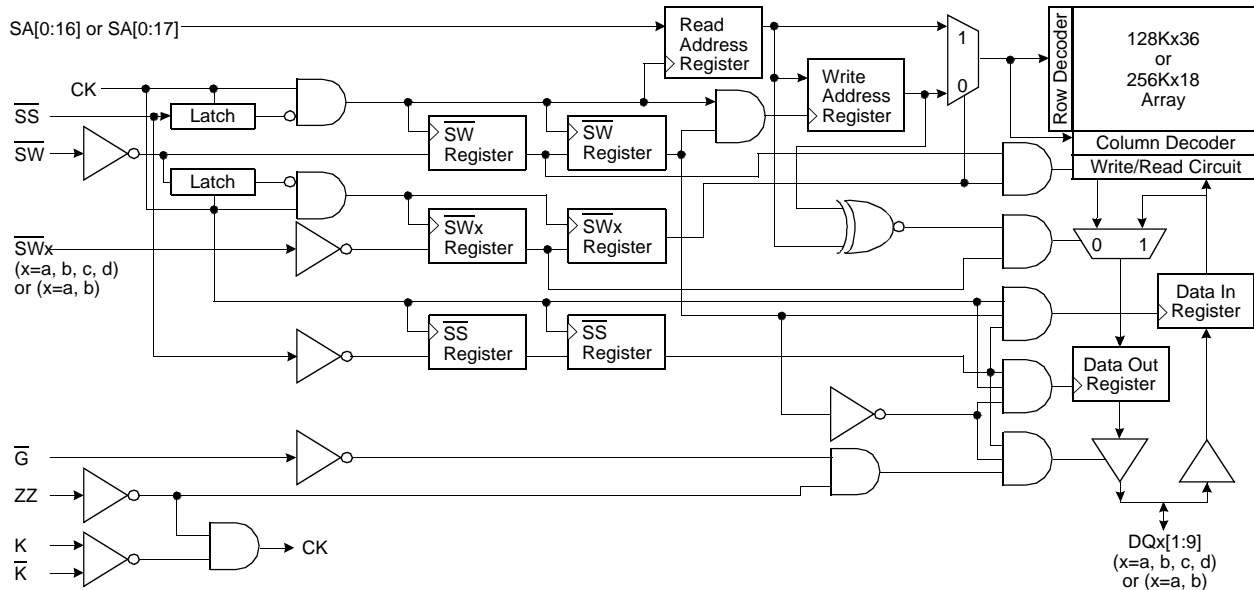
**128Kx36 & 256Kx18 Synchronous Pipelined SRAM**

**FEATURES**

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/1.5V Output Power Supply.
- HSTL Input and Output Levels.
- Differential, HSTL Clock Inputs K,  $\bar{K}$ .
- Synchronous Read and Write Operation
- Registered Input and Registered Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- Programmable Impedance Output Drivers.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17)Pin Ball Grid Array Package(14mmx22mm).

Organization	Part Number	Cycle Time	Access Time
128Kx36	K7P403611A-H30	3.3	1.8
	K7P403611A-H27	3.6	1.9
	K7P403611A-H25	4.0	2.0
256Kx18	K7P401811A-H30	3.3	1.8
	K7P401811A-H27	3.6	1.9
	K7P401811A-H25	4.0	2.0

**FUNCTIONAL BLOCK DIAGRAM**



**PIN DESCRIPTION**

Pin Name	Pin Description	Pin Name	Pin Description
K, $\bar{K}$	Differential Clocks	VREF	HSTL Input Reference Voltage
SAn	Synchronous Address Input	M1, M2	Read Protocol Mode Pins ( M1=Vss, M2=VDD )
DQn	Bi-directional Data Bus	$\bar{G}$	Asynchronous Output Enable
$\bar{SW}$	Synchronous Global Write Enable	$\bar{SS}$	Synchronous Select
$\bar{SWa}$	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
$\bar{SWb}$	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
$\bar{SWc}$	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
$\bar{SWd}$	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	ZQ	Output Driver Impedance Control
VDD	Core Power Supply	Vss	GND
VDDQ	Output Power Supply	NC	No Connection

**K7P403611A**  
**K7P401811A**

**128Kx36 & 256Kx18 SRAM**

**PACKAGE PIN CONFIGURATIONS(TOP VIEW)**

**K7P403611A(128Kx36)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	SA <sub>13</sub>	SA <sub>10</sub>	NC	SA <sub>7</sub>	SA <sub>4</sub>	V <sub>DDQ</sub>
<b>B</b>	NC	NC	SA <sub>9</sub>	NC	SA <sub>8</sub>	NC	NC
<b>C</b>	NC	SA <sub>12</sub>	SA <sub>11</sub>	V <sub>DD</sub>	SA <sub>6</sub>	SA <sub>5</sub>	NC
<b>D</b>	DQ <sub>c8</sub>	DQ <sub>c9</sub>	V <sub>SS</sub>	ZQ	V <sub>SS</sub>	DQ <sub>b9</sub>	DQ <sub>b8</sub>
<b>E</b>	DQ <sub>c6</sub>	DQ <sub>c7</sub>	V <sub>SS</sub>	$\overline{SS}$	V <sub>SS</sub>	DQ <sub>b7</sub>	DQ <sub>b6</sub>
<b>F</b>	V <sub>DDQ</sub>	DQ <sub>c5</sub>	V <sub>SS</sub>	$\overline{G}$	V <sub>SS</sub>	DQ <sub>b5</sub>	V <sub>DDQ</sub>
<b>G</b>	DQ <sub>c3</sub>	DQ <sub>c4</sub>	$\overline{SWc}$	NC	$\overline{SWb}$	DQ <sub>b4</sub>	DQ <sub>b3</sub>
<b>H</b>	DQ <sub>c1</sub>	DQ <sub>c2</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQ <sub>b2</sub>	DQ <sub>b1</sub>
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	DQ <sub>d1</sub>	DQ <sub>d2</sub>	V <sub>SS</sub>	K	V <sub>SS</sub>	DQ <sub>a2</sub>	DQ <sub>a1</sub>
<b>L</b>	DQ <sub>d3</sub>	DQ <sub>d4</sub>	$\overline{SWd}$	$\overline{K}$	$\overline{SWa}$	DQ <sub>a4</sub>	DQ <sub>a3</sub>
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>d5</sub>	V <sub>SS</sub>	$\overline{SW}$	V <sub>SS</sub>	DQ <sub>a5</sub>	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>d6</sub>	DQ <sub>d7</sub>	V <sub>SS</sub>	SA <sub>16</sub>	V <sub>SS</sub>	DQ <sub>a7</sub>	DQ <sub>a6</sub>
<b>P</b>	DQ <sub>d8</sub>	DQ <sub>d9</sub>	V <sub>SS</sub>	SA <sub>0</sub>	V <sub>SS</sub>	DQ <sub>a9</sub>	DQ <sub>a8</sub>
<b>R</b>	NC	SA <sub>15</sub>	M <sub>1</sub>	V <sub>DD</sub>	M <sub>2</sub>	SA <sub>2</sub>	NC
<b>T</b>	NC	NC	SA <sub>14</sub>	SA <sub>1</sub>	SA <sub>3</sub>	NC	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**K7P401811A(256Kx18)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	SA <sub>13</sub>	SA <sub>10</sub>	NC	SA <sub>7</sub>	SA <sub>4</sub>	V <sub>DDQ</sub>
<b>B</b>	NC	NC	SA <sub>9</sub>	NC	SA <sub>8</sub>	NC	NC
<b>C</b>	NC	SA <sub>12</sub>	SA <sub>11</sub>	V <sub>DD</sub>	SA <sub>6</sub>	SA <sub>5</sub>	NC
<b>D</b>	DQ <sub>b1</sub>	NC	V <sub>SS</sub>	ZQ	V <sub>SS</sub>	DQ <sub>a9</sub>	NC
<b>E</b>	NC	DQ <sub>b2</sub>	V <sub>SS</sub>	$\overline{SS}$	V <sub>SS</sub>	NC	DQ <sub>a8</sub>
<b>F</b>	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	$\overline{G}$	V <sub>SS</sub>	DQ <sub>a7</sub>	V <sub>DDQ</sub>
<b>G</b>	NC	DQ <sub>b3</sub>	$\overline{SWb}$	NC	NC	NC	DQ <sub>a6</sub>
<b>H</b>	DQ <sub>b4</sub>	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQ <sub>a5</sub>	NC
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	NC	DQ <sub>b5</sub>	V <sub>SS</sub>	K	V <sub>SS</sub>	NC	DQ <sub>a4</sub>
<b>L</b>	DQ <sub>b6</sub>	NC	NC	$\overline{K}$	$\overline{SWa}$	DQ <sub>a3</sub>	NC
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>b7</sub>	V <sub>SS</sub>	$\overline{SW}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>b8</sub>	NC	V <sub>SS</sub>	SA <sub>16</sub>	V <sub>SS</sub>	DQ <sub>a2</sub>	NC
<b>P</b>	NC	DQ <sub>b9</sub>	V <sub>SS</sub>	SA <sub>1</sub>	V <sub>SS</sub>	NC	DQ <sub>a1</sub>
<b>R</b>	NC	SA <sub>15</sub>	M <sub>1</sub>	V <sub>DD</sub>	M <sub>2</sub>	SA <sub>2</sub>	NC
<b>T</b>	NC	SA <sub>17</sub>	SA <sub>14</sub>	NC	SA <sub>3</sub>	SA <sub>0</sub>	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

## FUNCTION DESCRIPTION

The K7P403611A and K7P401811A are 4,718,592 bit Synchronous Pipeline Mode SRAM. It is organized as 131,072 words of 36 bits (or 262,144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.

Single differential HSTL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, All addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers edge of the next rising edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

### Read Operation

During reads, the address is registered during the first clock edge, the internal array is read between this first edge and the second edge, and data is captured in the output register and driven to the CPU during the second clock edge.  $\overline{SS}$  is driven low during this cycle, signaling that the SRAM should drive out the data.

During consecutive read cycles where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

### Write(Store) Operation

All addresses and  $\overline{SW}$  are sampled on the clock rising edge.  $\overline{SW}$  is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and  $\overline{SW}$  have been sampled by the SRAM.  $\overline{SS}$  will be driven low during the same cycle that the Address,  $\overline{SW}$  and  $SW[a:d]$  are valid to signal that a valid operation is on the Address and Control Input.

Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals  $SW[a:d]$  signal which 9-bit bytes will be written. Timing of  $SW[a:d]$  is the same as the  $\overline{SW}$  signal.

### Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

### Programmable Impedance Output Buffer Operation

This HSTL Late Write SRAM has been designed with programmable impedance output buffers. The SRAMs output buffer impedance can be adjusted to match the system data bus impedance, by connecting an external resistor (RQ) between the ZQ pin of the SRAM and Vss. The value of RQ must be five times the value of the intended line impedance driven by the SRAM. For example, a 250 $\Omega$  resistor will give an output buffer impedance of 50 $\Omega$ . The allowable range of RQ is from 175 $\Omega$  to 350 $\Omega$ . Internal circuits evaluate and periodically adjust the output buffer impedance, as the impedance is affected by drifts in supply voltage and temperature. One evaluation occurs every 32 clock cycles, with each evaluation moving the output buffer impedance level only one step at a time toward the optimum level. Impedance updates occur when the SRAM is in High-Z state, and thus are triggered by write and deselect operations. Updates will also be triggered with G HIGH initiated High-Z state, providing the specified G setup and hold times are met. Impedance match is not instantaneous upon power-up. In order to guarantee optimum output driver impedance, the SRAM requires a minimum number of non-read cycles (1,024) after power-up. The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to Vss or VDD.

### Mode Control

There are two mode control select pins (M1 and M2) used to set the proper read protocol. This SRAM supports single clock pipelined operating mode. For proper specified device operation, M1 must be connected to Vss and M2 must be connected to VDD. These mode pins must be set at power-up and must not change during device operation.

### Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: Vss, VDD, VDDQ, VREF, then VIN. VDD and VDDQ can be applied simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: VIN, VREF, VDDQ, VDD, Vss. VDD and VDDQ can be removed simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-down.

### Sleep Mode

Sleep mode is a low power mode initiated by bringing the asynchronous ZZ pin high. During sleep mode, all other inputs are ignored and outputs are brought to a High-Impedance state. Sleep mode current and output High-Z are guaranteed after the specified sleep mode enable time. During sleep mode the memory array data content is preserved. Sleep mode must not be initiated until after all pending operations have completed, as any pending operation is not guaranteed to properly complete after sleep mode is initiated. Normal operations can be resumed by bringing the ZZ pin low, but only after the specified sleep mode recovery time.

**TRUTH TABLE**

K	ZZ	$\overline{G}$	$\overline{SS}$	$\overline{SW}$	$\overline{SWa}$	$\overline{SWb}$	$\overline{SWc}$	$\overline{SWd}$	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled.
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	X	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	X	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	X	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	X	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	X	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	X	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all byte

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit	Note
Core Supply Voltage Relative to Vss	VDD	-0.5 to 3.9	V	
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to 3.9	V	
Voltage on any I/O pin Relative to Vss	VTERM	-0.5 to VDD+0.5	V	
Output Short-Circuit Current	IOUT	25	mA	
Operating Temperature	TOPR	0 to 70	°C	
Storage Temperature	TSTG	-55 to 125	°C	

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	VDD	3.15	3.3	3.45	V	
Output Power Supply Voltage	VDDQ	1.4	1.5	1.6	V	
Input High Level	VIH	VREF+0.1	-	VDDQ+0.3	V	
Input Low Level	VIL	-0.3	-	VREF-0.1	V	
Input Reference Voltage	VREF	0.6	VDDQ/2	2VDDQ/3	V	
Clock Input Signal Voltage	VIN-CLK	-0.3	-	VDDQ+0.3	V	
Clock Input Differential Voltage	VDIF-CLK	0.1	-	VDDQ+0.6	V	
Clock Input Common Mode Voltage	VCM-CLK	0.6	VDDQ/2	2VDDQ/3	V	

**PIN CAPACITANCE**

Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C <sub>IN</sub>	-	4	pF
Output Capacitance	C <sub>OUT</sub>	-	6	pF

**NOTE** : Periodically sampled and not 100% tested.(dV=0V, f=1MHz)

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , ZZ & SS=V <sub>IL</sub> )	I <sub>DD33</sub> I <sub>DD36</sub> I <sub>DD4</sub>	-	650 600 550	mA	1, 2
Average Power Supply Operating Current-x18 (V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , ZZ & SS=V <sub>IL</sub> )	I <sub>DD33</sub> I <sub>DD36</sub> I <sub>DD4</sub>	-	600 550 500	mA	1, 2
Power Supply Standby Current (V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , ZZ=V <sub>IH</sub> )	I <sub>SBZZ</sub>	-	60	mA	1
Active Standby Power Supply Current (V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , SS=V <sub>IH</sub> , ZZ=V <sub>IL</sub> )	I <sub>SBSS</sub>	-	200	mA	1
Input Leakage Current (V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DDQ</sub> )	I <sub>LI</sub>	-1	1	μA	
Output Leakage Current (V <sub>OUT</sub> =V <sub>SS</sub> or V <sub>DDQ</sub> , DQ in High-Z)	I <sub>LO</sub>	-1	1	μA	
Output High Voltage(Programmable Impedance Mode)	V <sub>OH1</sub>	V <sub>DDQ</sub> /2	V <sub>DDQ</sub>	V	3, 5
Output Low Voltage(Programmable Impedance Mode)	V <sub>OL1</sub>	V <sub>SS</sub>	V <sub>DDQ</sub> /2	V	4, 5
Output High Voltage(I <sub>OH</sub> =-0.1mA)	V <sub>OH2</sub>	V <sub>DDQ</sub> -0.2	V <sub>DDQ</sub>	V	6
Output Low Voltage(I <sub>OL</sub> =0.1mA)	V <sub>OL2</sub>	V <sub>SS</sub>	0.2	V	6
Output High Voltage(I <sub>OH</sub> =-6mA)	V <sub>OH3</sub>	V <sub>DDQ</sub> -0.4	V <sub>DDQ</sub>	V	6
Output Low Voltage(I <sub>OL</sub> =6mA)	V <sub>OL3</sub>	V <sub>SS</sub>	0.4	V	6

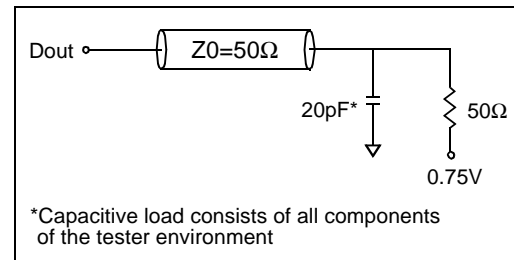
**NOTE** :1. Minimum cycle. I<sub>OUT</sub>=0mA.  
 2. 50% read cycles.  
 3. |I<sub>OH</sub>|=(V<sub>DDQ</sub>/2)/(R<sub>Q</sub>/5)±10% @V<sub>OH</sub>=V<sub>DDQ</sub>/2 for 175Ω ≤ R<sub>Q</sub> ≤ 350Ω.  
 4. |I<sub>OL</sub>|=(V<sub>DDQ</sub>/2)/(R<sub>Q</sub>/5)±10% @V<sub>OL</sub>=V<sub>DDQ</sub>/2 for 175Ω ≤ R<sub>Q</sub> ≤ 350Ω.  
 5. Programmable Impedance Output Buffer Mode. The ZQ pin is connected to V<sub>SS</sub> through R<sub>Q</sub>.  
 6. Minimum Impedance Output Buffer Mode. The ZQ pin is connected to V<sub>SS</sub> or V<sub>DD</sub>.

**AC TEST CONDITIONS**

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	V <sub>DD</sub>	3.15~3.45	V
Output Power Supply Voltage	V <sub>DDQ</sub>	1.4~1.6	V
Input High/Low Level	V <sub>IH</sub> /V <sub>IL</sub>	1.25/0.25	V
Input Reference Level	V <sub>REF</sub>	0.75	V
Input Rise/Fall Time	T <sub>R</sub> /T <sub>F</sub>	1.0/1.0	ns
Input and Out Timing Reference Level		0.75	V
Clock Input Timing Reference Level		Cross Point	V

**NOTE :** Parameters are tested with R<sub>Q</sub>=250Ω and V<sub>DDQ</sub>=1.5V.

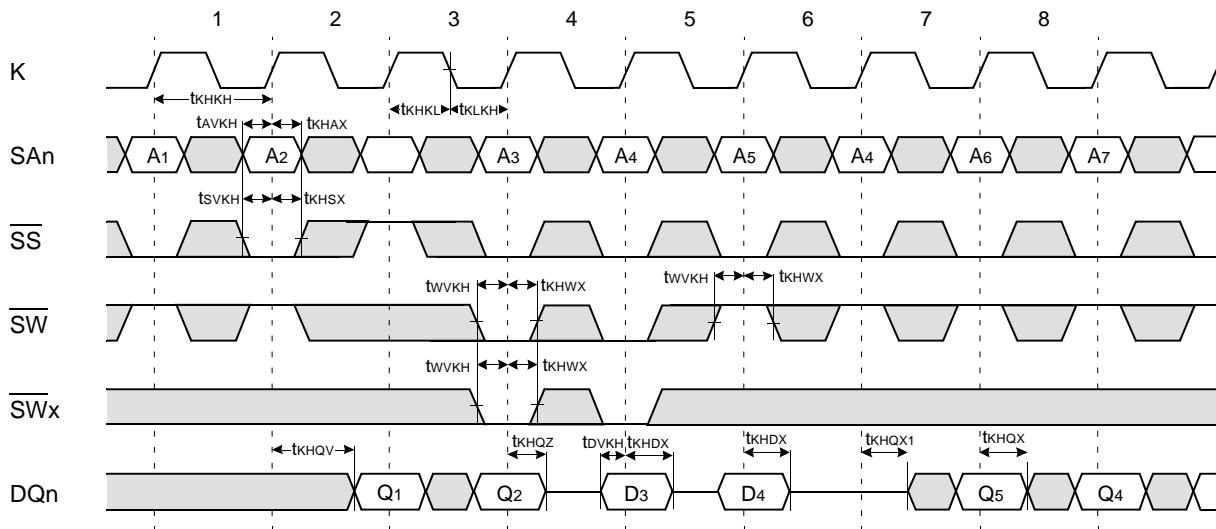
**AC TEST OUTPUT LOAD**



**AC CHARACTERISTICS**

Parameter	Symbol	-30		-27		-25		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t <sub>KHKH</sub>	3.3	-	3.6	-	4.0	-	ns	
Clock High Pulse Width	t <sub>KHKL</sub>	1.2	-	1.2	-	1.2	-	ns	
Clock Low Pulse Width	t <sub>KLKH</sub>	1.2	-	1.2	-	1.2	-	ns	
Clock High to Output Valid	t <sub>KHQV</sub>	-	1.8	-	1.9	-	2.0	ns	
Clock High to Output Hold	t <sub>KHQX</sub>	0.5	-	0.5	-	0.5	-	ns	
Address Setup Time	t <sub>AVKH</sub>	0.4	-	0.4	-	0.4	-	ns	
Address Hold Time	t <sub>KHAX</sub>	0.7	-	0.7	-	0.7	-	ns	
Write Data Setup Time	t <sub>DVKH</sub>	0.4	-	0.4	-	0.4	-	ns	
Write Data Hold Time	t <sub>KHDX</sub>	0.7	-	0.7	-	0.7	-	ns	
$\overline{SW}$ , $\overline{SW}[a:d]$ Setup Time	t <sub>WVKH</sub>	0.4	-	0.4	-	0.4	-	ns	
$\overline{SW}$ , $\overline{SW}[a:d]$ Hold Time	t <sub>KHWX</sub>	0.7	-	0.7	-	0.7	-	ns	
$\overline{SS}$ Setup Time	t <sub>SVKH</sub>	0.4	-	0.4	-	0.4	-	ns	
$\overline{SS}$ Hold Time	t <sub>KHSX</sub>	0.7	-	0.7	-	0.7	-	ns	
Clock High to Output Hi-Z	t <sub>KHQZ</sub>	-	2.0	-	2.0	-	2.0	ns	
Clock High to Output Low-Z	t <sub>KHQX1</sub>	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ High to Output High-Z	t <sub>GHQZ</sub>	-	2.0	-	2.0	-	2.0	ns	
$\overline{G}$ Low to Output Low-Z	t <sub>GLQX</sub>	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ Low to Output Valid	t <sub>GLQV</sub>	-	2.0	-	2.0	-	2.0	ns	
ZZ High to Power Down(Sleep Time)	t <sub>ZZE</sub>	-	6.6	-	7.2	-	8.0	ns	
ZZ Low to Recovery(Wake-up Time)	t <sub>ZZR</sub>	-	6.6	-	7.2	-	8.0	ns	

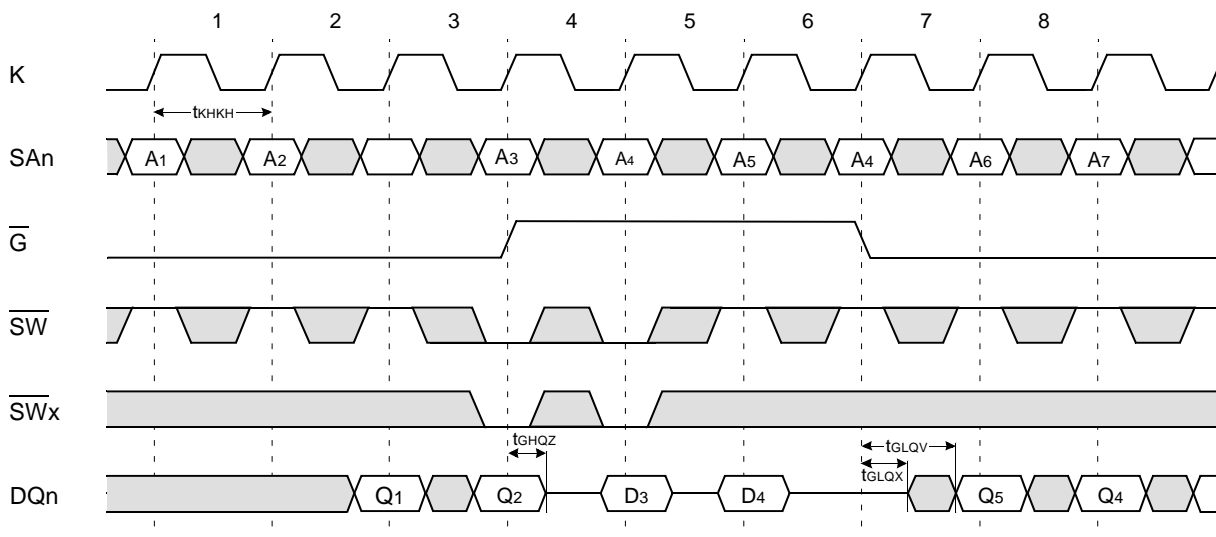
**TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES ( $\overline{SS}$  Controlled,  $\overline{G}=Low$ )**



**NOTE**

1.  $D3$  is the input data written in memory location  $A3$ .
2.  $Q4$  is the output data read from the write data buffer(not from the cell array), as a result of address  $A4$  being a match from the last write cycle address.

**TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES ( $\overline{G}$  Controlled,  $\overline{SS}=Low$ )**

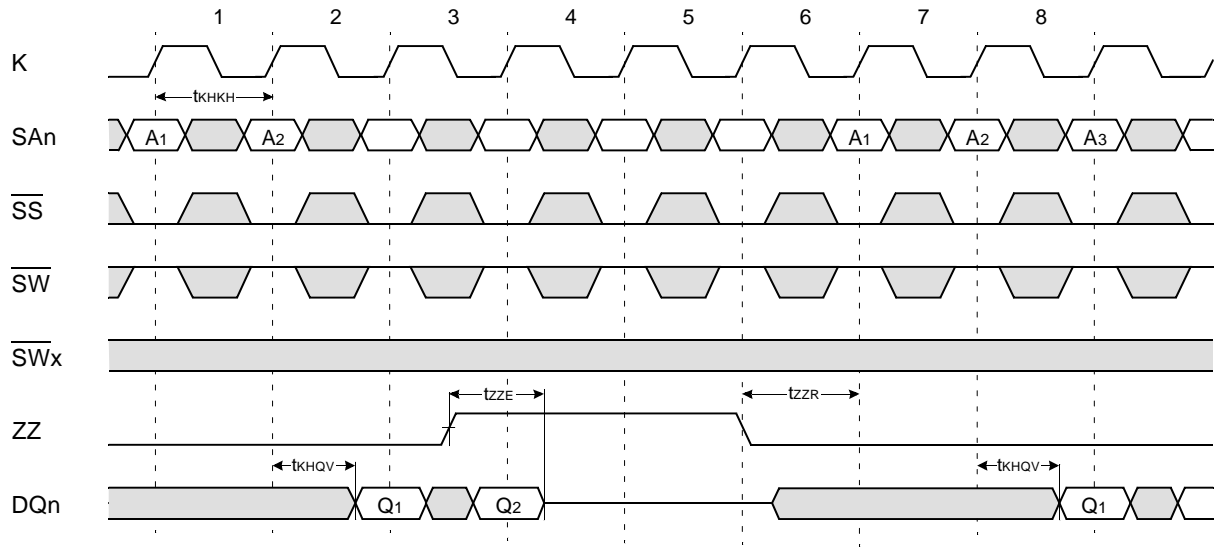


**NOTE**

1.  $D3$  is the input data written in memory location  $A3$ .
2.  $Q4$  is the output data read from the write data buffer(not from the cell array), as a result of address  $A4$  being a match from the last write cycle address.



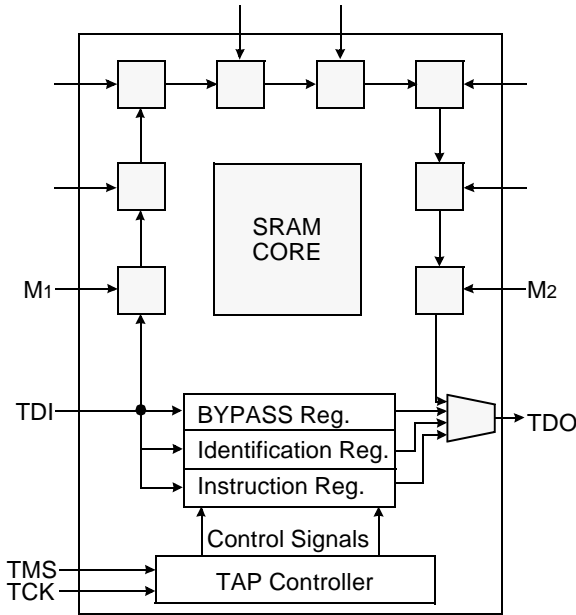
**TIMING WAVEFORMS OF STANDBY CYCLES**



**IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG**

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to Vdd through a resistor. TDO should be left unconnected.

**JTAG Block Diagram**



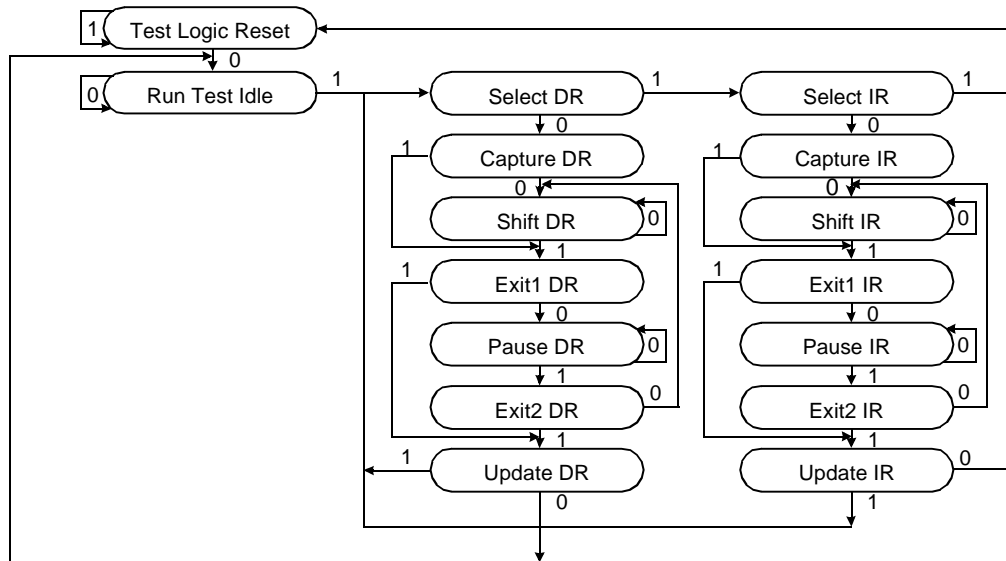
**JTAG Instruction Coding**

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

**NOTE :**

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not place DQs in Hi-Z.

**TAP Controller State Diagram**



**SCAN REGISTER DEFINITION**

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

**ID REGISTER DEFINITION**

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	XXXXXX	00001001110	1
256Kx18	0000	00110 00011	XXXXXX	00001001110	1

**BOUNDARY SCAN EXIT ORDER(x36)**

36	3B	SA <sub>9</sub>		SA <sub>8</sub>	5B	35
37	2B	NC		NC	6B	34
38	3A	SA <sub>10</sub>		SA <sub>7</sub>	5A	33
39	3C	SA <sub>11</sub>		SA <sub>6</sub>	5C	32
40	2C	SA <sub>12</sub>		SA <sub>5</sub>	6C	31
41	2A	SA <sub>13</sub>		SA <sub>4</sub>	6A	30
42	2D	DQc <sub>9</sub>		DQb <sub>9</sub>	6D	29
43	1D	DQc <sub>8</sub>		DQb <sub>8</sub>	7D	28
44	2E	DQc <sub>7</sub>		DQb <sub>7</sub>	6E	27
45	1E	DQc <sub>6</sub>		DQb <sub>6</sub>	7E	26
46	2F	DQc <sub>5</sub>		DQb <sub>5</sub>	6F	25
47	2G	DQc <sub>4</sub>		DQb <sub>4</sub>	6G	24
48	1G	DQc <sub>3</sub>		DQb <sub>3</sub>	7G	23
49	2H	DQc <sub>2</sub>		DQb <sub>2</sub>	6H	22
50	1H	DQc <sub>1</sub>		DQb <sub>1</sub>	7H	21
51	3G	$\overline{SWc}$		$\overline{SWb}$	5G	20
52	4D	ZQ		$\overline{G}$	4F	19
53	4E	$\overline{SS}$		K	4K	18
54	4G	NC		$\overline{K}$	4L	17
55	4H	NC		$\overline{SWa}$	5L	16
56	4M	$\overline{SW}$		DQa <sub>1</sub>	7K	15
57	3L	$\overline{SWd}$		DQa <sub>2</sub>	6K	14
58	1K	DQd <sub>1</sub>		DQa <sub>3</sub>	7L	13
59	2K	DQd <sub>2</sub>		DQa <sub>4</sub>	6L	12
60	1L	DQd <sub>3</sub>		DQa <sub>5</sub>	6M	11
61	2L	DQd <sub>4</sub>		DQa <sub>6</sub>	7N	10
62	2M	DQd <sub>5</sub>		DQa <sub>7</sub>	6N	9
63	1N	DQd <sub>6</sub>		DQa <sub>8</sub>	7P	8
64	2N	DQd <sub>7</sub>		DQa <sub>9</sub>	6P	7
65	1P	DQd <sub>8</sub>		ZZ	7T	6
66	2P	DQd <sub>9</sub>		SA <sub>3</sub>	5T	5
67	3T	SA <sub>14</sub>		SA <sub>2</sub>	6R	4
68	2R	SA <sub>15</sub>		SA <sub>1</sub>	4T	3
69	4N	SA <sub>16</sub>		SA <sub>0</sub>	4P	2
70	3R	M <sub>1</sub>		M <sub>2</sub>	5R	1

**BOUNDARY SCAN EXIT ORDER(x18)**

26	3B	SA <sub>9</sub>		SA <sub>8</sub>	5B	25
27	2B	NC		NC	6B	24
28	3A	SA <sub>10</sub>		SA <sub>7</sub>	5A	23
29	3C	SA <sub>11</sub>		SA <sub>6</sub>	5C	22
30	2C	SA <sub>12</sub>		SA <sub>5</sub>	6C	21
31	2A	SA <sub>13</sub>		SA <sub>4</sub>	6A	20
				DQa <sub>9</sub>	6D	19
32	1D	DQb <sub>1</sub>				
33	2E	DQb <sub>2</sub>				
				DQa <sub>8</sub>	7E	18
				DQa <sub>7</sub>	6F	17
34	2G	DQb <sub>3</sub>				
				DQa <sub>6</sub>	7G	16
				DQa <sub>5</sub>	6H	15
35	1H	DQb <sub>4</sub>				
36	3G	$\overline{SWb}$				
37	4D	ZQ		$\overline{G}$	4F	14
38	4E	$\overline{SS}$		K	4K	13
39	4G	NC		$\overline{K}$	4L	12
40	4H	NC		$\overline{SWa}$	5L	11
41	4M	$\overline{SW}$		DQa <sub>4</sub>	7K	10
42	2K	DQb <sub>5</sub>		DQa <sub>3</sub>	6L	9
43	1L	DQb <sub>6</sub>				
44	2M	DQb <sub>7</sub>		DQa <sub>2</sub>	6N	8
45	1N	DQb <sub>8</sub>		DQa <sub>1</sub>	7P	7
				ZZ	7T	6
46	2P	DQb <sub>9</sub>		SA <sub>3</sub>	5T	5
47	3T	SA <sub>14</sub>		SA <sub>2</sub>	6R	4
48	2R	SA <sub>15</sub>				
49	4N	SA <sub>16</sub>		SA <sub>1</sub>	4P	3
50	2T	SA <sub>17</sub>		SA <sub>0</sub>	6T	2
51	3R	M <sub>1</sub>		M <sub>2</sub>	5R	1

**NOTE :** 1. Pins 6B/2B are no connection pins to internal chip and place holders for 8M/16M parts. The scanned data are fixed to "0" for this 4M part.  
2. Pins 4G and 4H are no connection pin to internal chip. The scanned data are fixed to "0" and "1" respectively.

**JTAG DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	3.15	3.3	3.45	V	
Input High Level	V <sub>IH</sub>	1.7	-	V <sub>DD</sub> +0.3	V	
Input Low Level	V <sub>IL</sub>	-0.3	-	0.7	V	
Output High Voltage(I <sub>OH</sub> =-2mA)	V <sub>OH</sub>	2.0	-	V <sub>DD</sub>	V	
Output Low Voltage(I <sub>OL</sub> =2mA)	V <sub>OL</sub>	V <sub>SS</sub>	-	0.4	V	

**NOTE** : 1. The input level of SRAM pin is to follow the SRAM DC specification.

**JTAG AC TEST CONDITIONS**

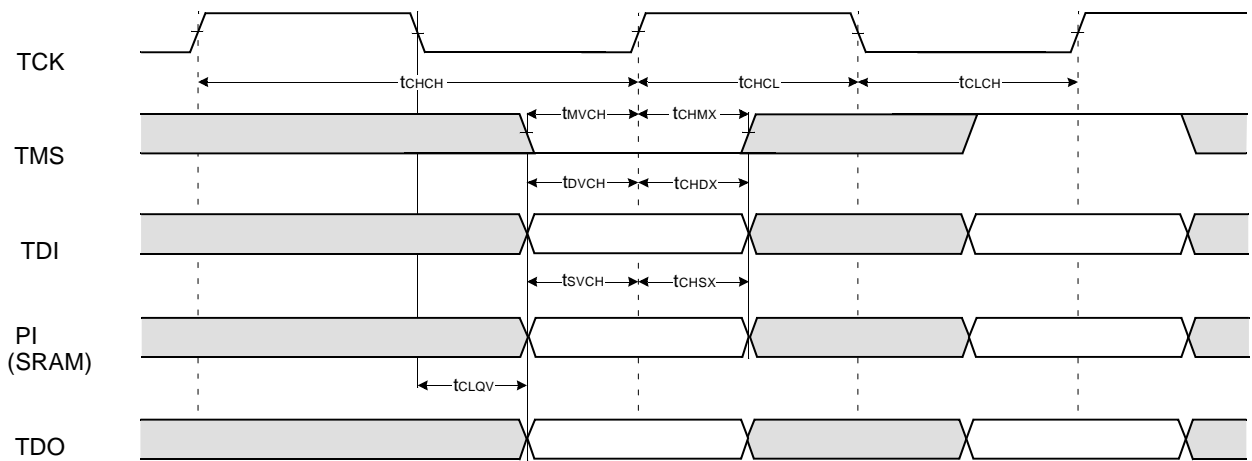
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V <sub>IH</sub> /V <sub>IL</sub>	2.5/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		1.25	V	1

**NOTE** : 1. See SRAM AC test output load on page 7.

**JTAG AC Characteristics**

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t <sub>CHCH</sub>	50	-	ns	
TCK High Pulse Width	t <sub>CHCL</sub>	20	-	ns	
TCK Low Pulse Width	t <sub>CLCH</sub>	20	-	ns	
TMS Input Setup Time	t <sub>MVCH</sub>	5	-	ns	
TMS Input Hold Time	t <sub>CHMX</sub>	5	-	ns	
TDI Input Setup Time	t <sub>DVCH</sub>	5	-	ns	
TDI Input Hold Time	t <sub>CHDX</sub>	5	-	ns	
SRAM Input Setup Time	t <sub>SVCH</sub>	5	-	ns	
SRAM Input Hold Time	t <sub>CHSX</sub>	5	-	ns	
Clock Low to Output Valid	t <sub>CLQV</sub>	0	10	ns	

**JTAG TIMING DIAGRAM**



**119 BGA PACKAGE DIMENSIONS**

