R1Q2A7236ABG
R1Q2A7218ABG
R1Q2A7209ABG

72-Mbit QDR™II SRAM
2-word Burst

R10DS0175EJ0011
Rev. 0.11
2013.01.15

Description

The R1Q2A7236 is a 2,097,152-word by 36-bit, the R1Q2A7218 is a 4,194,304-word by 18-bit, and the R1Q2A7209 is a 8,388,608-word by 9-bit synchronous quad data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell. It integrates unique synchronous peripheral circuitry and a burst counter. All input registers are controlled by an input clock pair (K and /K) and are latched on the positive edge of K and /K. These products are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration. These products are packaged in 165-pin plastic FBGA package.

Features

- Power Supply
  - 1.8 V for core (V_{DD}), 1.4 V to V_{DD} for I/O (V_{DDQ})
- Clock
  - Fast clock cycle time for high bandwidth
  - Two input clocks (K and /K) for precise DDR timing at clock rising edges only
  - Two input clocks for output data (C and /C) to minimize clock skew and flight time mismatches
  - Two output echo clocks (CQ and /CQ) simplify data capture in high-speed systems
  - Clock-stop capability with µs restart
- I/O
  - Separate independent read and write data ports with concurrent transactions
  - 100% bus utilization DDR read and write operation
  - HSTL I/O
  - User programmable output impedance
  - DLL/PLL circuitry for wide output data valid window and future frequency scaling
- Function
  - Two-tick burst for low DDR transaction size
  - Internally self-timed write control
  - Simple control logic for easy depth expansion
  - JTAG 1149.1 compatible test access port
- Package
  - 165 FBGA package (15 x 17 x 1.4 mm)

Notes: 1. QDR RAMs and Quad Data Rate RAMs comprise a new family of products developed by Cypress Semiconductor, IDT, Samsung, and Renesas Electronics Corp. (QDR Co-Development Team)
2. The specifications of this device are subject to change without notice. Please contact your nearest Renesas Electronics Sales Office regarding specifications.
3. Refer to "http://www.renesas.com/products/memory/fast_sram/qdr_sram/index.jsp" for the latest and detailed information.

Part Number Definition

Column No.	0	1	2	3	4	5	6	7	8	9	10	11	-	12	13	14	15	16
Example	R	1	Q	2	A	7	2	1	8	A	B	G	-	4	0	R	B	0
	The above part number is just example for 72M QDRII B2 x18 250MHz, 15x17mm PKG, Pb-free part.																	

No.	-	Comments
0-1	R1	Renesas Memory Prefix
2-3	Q2	QDR II B2[*1] (L15)[*2]
	Q3	QDR II B4 (L15)
	Q4	DDR II B2 (L15)
	Q5	DDR II B4 (L15)
	Q6	DDR II B2 SIO[*3] (L15)
	QA	QDR II+ B4 L25[*2]
	QB	DDR II+ B2 L25
	QC	DDR II+ B4 L25
	QD	QDR II+ B4 L25 w/ODT[*4]
	QE	DDR II+ B2 L25 w/ODT
	QF	DDR II+ B4 L25 w/ODT
	QG	QDR II+ B4 L20
	QH	DDR II+ B2 L20
	QJ	DDR II+ B4 L20
	QK	QDR II+ B4 L20 w/ODT
	QL	DDR II+ B2 L20 w/ODT
	QM	DDR II+ B4 L20 w/ODT
	QN	QDR II+ B2 L20
	QP	QDR II+ B2 L20 w/ODT
	-	-

No.	-	Comments
4	A	Vdd = 1.8 V
5-6	36	Density = 36Mb
	72	Density = 72Mb
	44	Density = 144Mb
	88	Density = 288Mb
7-8	09	Data width = 9bit
	18	Data width = 18bit
	36	Data width = 36bit
9	R	1st Generation
	A	2nd Generation
	B	3rd Generation
	C	4th Generation
	D	5th Generation
	E	6th Generation
	F	7th Generation
10-11	BG	PKG= BGA 15x17 mm
	BB	PKG= BGA 13x15 mm
-	-	-

No.	-	Comments
12-13	60	Frequency = 167MHz
	50	Frequency = 200MHz
	40	Frequency = 250MHz
	36	Frequency = 275MHz
	33	Frequency = 300MHz
	30	Frequency = 333MHz
	27	Frequency = 375MHz
	25	Frequency = 400MHz
	22	Frequency = 450MHz
	20	Frequency = 500MHz
	19	Frequency = 533MHz
	18	Frequency = 550MHz
14	R	Commercial temp. Ta range = 0℃ to 70℃
	I	Industrial temp. Ta range = -40℃ to 85℃
15	A	Pb and Tray
	B	Pb-free and Tray
	T	Pb and Tape&Reel
	S	Pb-free and Tape&Reel
16	0 to 9, A to Z or None	Renesas internal use

Note1:
[*1] B=Burst length (B2: Burst length=2, B4: Burst length=4)
[*2] L=Read Latency (L15: Read Latency = 1.5 cycle, L20: 2.0 cycle, L25: 2.5 cycle)
[*3] SIO=Separate I/O
[*4] ODT=On die termination

Note2:
Package Marking Name
Pb parts: Marking Name = Part Number(0-14)
Pb-free parts: Marking Name = Part Number(0-14) + "PB-F"
(Example) R1QAA4436RBG-20R ----- Pb parts
R1QAA4436RBG-20R PB-F ----- Pb-free parts

Note3:
Pb : RoHS Compliance Level = 5/6
Pb-free: RoHS Compliance Level = 6/6

Note4:
R1Q*A series support both "Commercial" and "Industrial" temperatures by "Industrial" temperature parts.

72M QDR/DDR SRAM (R1Q*A72 Series) Lineup

- Renesas supports or plans to support the parts listed below.

No	Product Type	Burst Length	Latency (Cycle)	ODT	Organi-zation		QDR II+ / DDR II+						QDR II / DDR II			
						Frequency (max) (MHz)	533	500	450	400	375	333	333	300	250	200
						Cycle Time (min) (ns)	1.875	2.00	2.22	2.50	2.66	3.00	3.00	3.30	4.00	5.00
						Part Number ↓ yy →	-19	-20	-22	-25	-27	-30	-30	-33	-40	-50
1	QDRII	B2	1.5	No	x 9	R1Q 2 A72 09 A Bv-yy									-40	-50
2					x18	R1Q 2 A72 18 A Bv-yy									-40	-50
3					x36	R1Q 2 A72 36 A Bv-yy										
5		B4			x18	R1Q 3 A72 18 A Bv-yy							-30	-33	-40	
6					x36	R1Q 3 A72 36 A Bv-yy										
8	DDRII	B2			x18	R1Q 4 A72 18 A Bv-yy							-30	-33	-40	
9					x36	R1Q 4 A72 36 A Bv-yy										
11		B4			x18	R1Q 5 A72 18 A Bv-yy							-30	-33	-40	
12					x36	R1Q 5 A72 36 A Bv-yy										
14	DDRII SIO	B2			x18	R1Q 6 A72 18 A Bv-yy							-30	-33	-40	
15					x36	R1Q 6 A72 36 A Bv-yy										
17	QDRII+	B4	2.5	No	x18	R1Q A A72 18 A Bv-yy	-19	-20	-22							
18					x36	R1Q A A72 36 A Bv-yy										
20	DDRII+	B2			x18	R1Q B A72 18 A Bv-yy	-19	-20	-22							
21					x36	R1Q B A72 36 A Bv-yy										
23		B4			x18	R1Q C A72 18 A Bv-yy	-19	-20	-22							
24					x36	R1Q C A72 36 A Bv-yy										
26	QDRII+	B4	2.5	Yes	x18	R1Q D A72 18 A Bv-yy	-19	-20	-22							
27					x36	R1Q D A72 36 A Bv-yy										
29	DDRII+	B2			x18	R1Q E A72 18 A Bv-yy	-19	-20	-22							
30					x36	R1Q E A72 36 A Bv-yy										
32		B4			x18	R1Q F A72 18 A Bv-yy	-19	-20	-22							
33					x36	R1Q F A72 36 A Bv-yy										
35	QDRII+	B4	2.0	No	x18	R1Q G A72 18 A Bv-yy				-25						
36					x36	R1Q G A72 36 A Bv-yy										
38	DDRII+	B2			x18	R1Q H A72 18 A Bv-yy				-25						
39					x36	R1Q H A72 36 A Bv-yy										
41		B4			x18	R1Q J A72 18 A Bv-yy				-25						
42					x36	R1Q J A72 36 A Bv-yy										
44	QDRII+	B4	2.0	Yes	x18	R1Q K A72 18 A Bv-yy				-25						
45					x36	R1Q K A72 36 A Bv-yy										
47	DDRII+	B2			x18	R1Q L A72 18 A Bv-yy				-25						
48					x36	R1Q L A72 36 A Bv-yy										
50		B4			x18	R1Q M A72 18 A Bv-yy				-25						
51					x36	R1Q M A72 36 A Bv-yy										

Notes:
1. "v" represents the package size. If "v" = "G" then size is 15 x 17 mm, and if "v" = "B" then 13 x 15 mm.
2. "yy" represents the speed bin. "R1QAA7236ABG-20" can operate at 500 MHz(max) of frequency, for example.
3. The part which is not listed above is not supported, as of the day when this datasheet was issued,
in spite of the existence of the part number or datasheet.

Pin Arrangement

R1Q2A7236 series

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	NC	SA	/W	/BW2	/K	/BW1	/R	SA	NC	CQ
B	Q27	Q18	D18	SA	/BW3	K	/BW0	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	SA	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	/DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	/C	SA	SA	SA	TMS	TDI

(Top View)

Notes: 1. Address expansion order for future higher density SRAMs: 10A → 2A → 7A → 5B.
2. NC pins can be left floating or connected to 0V ~ V_{DDQ}.

R1Q2A7218 series

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	NC	SA	/W	/BW1	/K	NC	/R	SA	SA	CQ
B	NC	Q9	D9	SA	NC	K	/BW0	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	SA	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	/DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	/C	SA	SA	SA	TMS	TDI

(Top View)

Notes: 1. Address expansion order for future higher density SRAMs: 10A → 2A → 7A → 5B.
2. NC pins can be left floating or connected to 0V ~ V_{DDQ}.

Pin Arrangement

R1Q2A7209 series

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	SA	SA	/W	NC	/K	NC	/R	SA	SA	CQ
B	NC	NC	NC	SA	NC	K	/BW	SA	NC	NC	Q4
C	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D4
D	NC	D5	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D3	Q3
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	D6	Q6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	/DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q2	D2
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	Q7	D7	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D1
N	NC	D8	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	Q8	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	/C	SA	SA	SA	TMS	TDI

(Top View)

Notes: 1. Address expansion order for future higher density SRAMs: 10A → 2A → 7A → 5B.

2. NC pins can be left floating or connected to 0V ~ V_{DDQ}.

Pin Descriptions

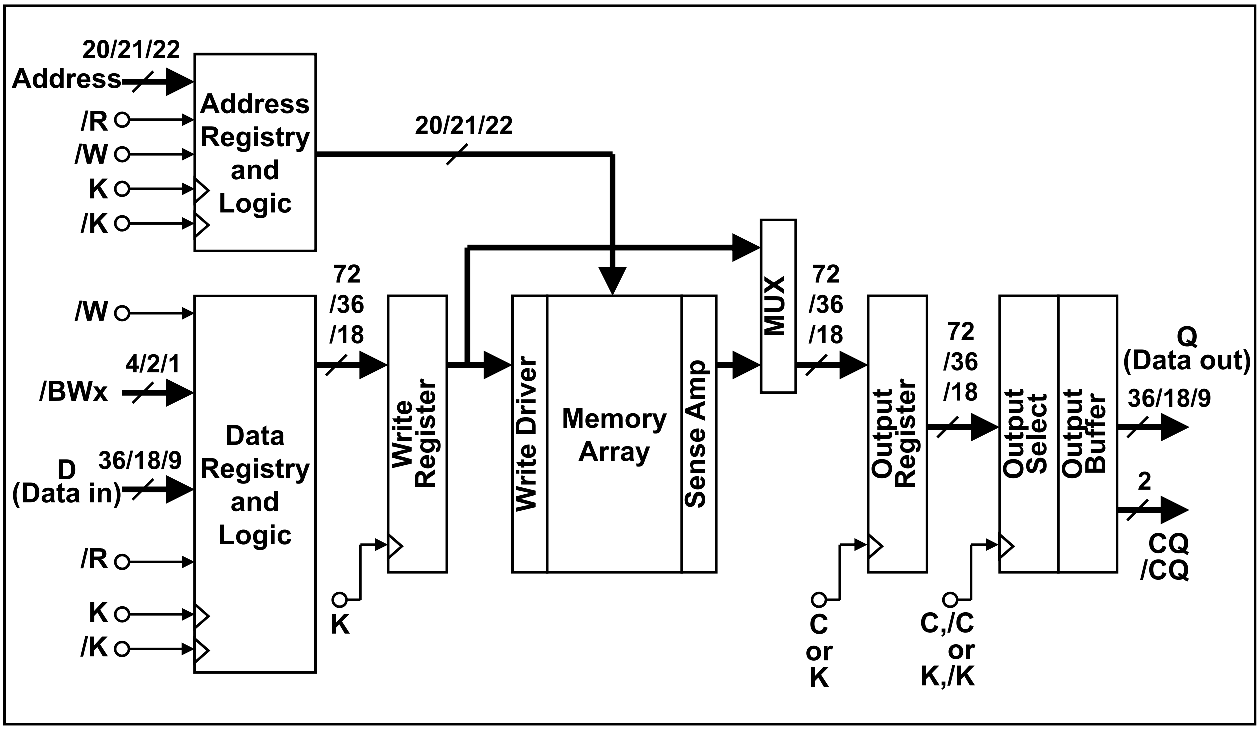
Name	I/O type	Descriptions	Notes
SA	Input	Synchronous address inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. All transactions operate on a burst-of-four words (two clock periods of bus activity). These inputs are ignored when device is deselected.	
/R	Input	Synchronous read: When low, this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K, and is ignored on the subsequent rising edge of K.	
/W	Input	Synchronous write: When low, this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K, and is ignored on the subsequent rising edge of K.	
$/BW_x$	Input	Synchronous byte writes: When low, these inputs cause their respective byte to be registered and written during WRITE cycles. These signals are sampled on the same edge as the corresponding data and must meet setup and hold times around the rising edges of K and /K for each of the two rising edges comprising the WRITE cycle. See Byte Write Truth Table for signal to data relationship.	
K, /K	Input	Input clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of /K. /K is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. These balls cannot remain V_{REF} level.	
C, /C **(II only)**	Input	Output clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of /C is used as the output timing reference for the first and third output data. The rising edge of C is used as the output timing reference for second and fourth output data. Ideally, /C is 180 degrees out of phase with C. C and /C may be tied high to force the use of K and /K as the output reference clocks instead of having to provide C and /C clocks. If tied high, C and /C must remain high and not to be toggled during device operation. These balls cannot remain V_{REF} level.	1
/DOFF	Input	DLL/PLL disable: When low, this input causes the DLL/PLL to be bypassed for stable, low frequency operation.	
TMS TDI	Input	IEEE1149.1 test inputs: 1.8 V I/O levels. These balls may be left not connected if the JTAG function is not used in the circuit.	
TCK	Input	IEEE1149.1 clock input: 1.8 V I/O levels. This ball must be tied to V_{SS} if the JTAG function is not used in the circuit.	

Notes:
1. R1Q2, R1Q3, R1Q4, R1Q5, R1Q6 series have C and /C pins. R1QA, R1QB, R1QC, R1QD, R1QE, R1QF, R1QG, R1QH, R1QJ, R1QK, R1QL, R1QM, R1QN, R1QP series do not have C, /C pins. In the series, K and /K are used as the output reference clocks instead of C and /C. Therefore, hereafter, C and /C represent K and /K in this document.

Name	I/O type	Descriptions	Notes
ZQ	Input	Output impedance matching input: This input is used to tune the device outputs to the system data bus impedance. Q and CQ output impedance are set to 0.2 × RQ, where RQ is a resistor from this ball to ground. This ball can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This ball cannot be connected directly to V_{SS} or left unconnected. In ODT (On Die Termination) enable devices, the ODT termination values tracks the value of RQ. The ODT range is selected by ODT control input.	
ODT **(II+ only)**	Input	ODT control: **When low**; [Option 1] Low range mode is selected. The impedance range is between 52 Ω and 105 Ω (Thevenin equivalent), which follows 0.3 × RQ for 175 Ω ≤ RQ ≤ 350 Ω. [Option 2] ODT is disabled. **When high**; High range mode is selected. The impedance range is between 105 Ω and 150 Ω (Thevenin equivalent), which follows 0.6 × RQ for 175 Ω ≤ RQ ≤ 250 Ω. **When floating**; [Option 1] High range mode is selected. [Option 2] ODT is disabled.	1
D_0 to D_n	Input	Synchronous data inputs: Input data must meet setup and hold times around the rising edges of K and /K during WRITE operations. See Pin Arrangement figures for ball site location of individual signals. The ×9 device uses D0~D8. D9~D35 should be treated as NC pin. The ×18 device uses D0~D17. D18~D35 should be treated as NC pin. The ×36 device uses D0~D35.	
CQ, /CQ	Output	Synchronous echo clock outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tri-states.	
TDO	Output	IEEE 1149.1 test output: 1.8 V I/O level.	
Q_0 to Q_n	Output	Synchronous data outputs: Output data is synchronized to the respective C and /C, or to the respective K and /K if C and /C are tied high. This bus operates in response to /R commands. See Pin Arrangement figures for ball site location of individual signals. The ×9 device uses Q0~Q8. Q9~Q35 should be treated as NC pin. The ×18 device uses Q0~Q17. Q18~Q35 should be treated as NC pin. The ×36 device uses Q0~Q35.	
QVLD **(II+ only)**	Output	Valid output indicator: The Q Valid indicates valid output data. QVLD is edge aligned with CQ and /CQ.	
V_{DD}	Supply	Power supply: 1.8 V nominal. See DC Characteristics and Operating Conditions for range.	2
V_{DDQ}	Supply	Power supply: Isolated output buffer supply. Nominally 1.5 V. See DC Characteristics and Operating Conditions for range.	2
V_{SS}	Supply	Power supply: Ground.	2
V_{REF}	—	HSTL input reference voltage: Nominally $V_{DDQ}/2$, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffers.	
NC	—	No connect: These pins can be left floating or connected to 0V ~ V_{DDQ}.	

Notes:
1. Renesas status: Option 1 = Available, Option 2 = Possible.
2. All power supply and ground balls must be connected for proper operation of the device.

Block Diagram (R1Q2A7236 / R1Q2A7218 / R1Q2A7209 series)



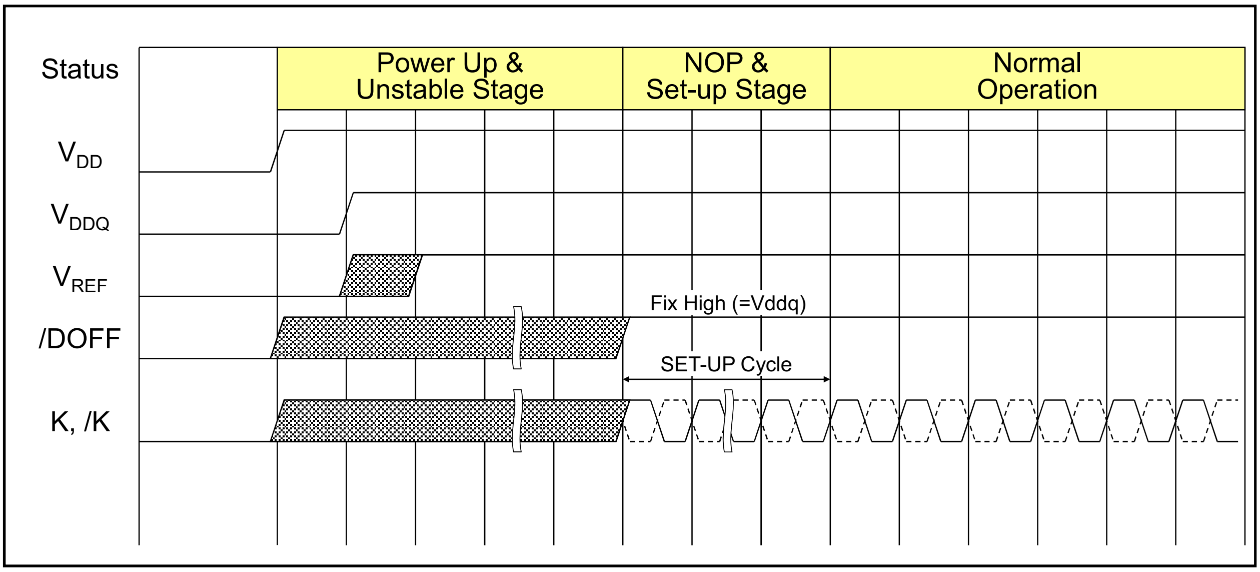
Notes
1. C and /C pins do not exist in II+ series parts.

General Description

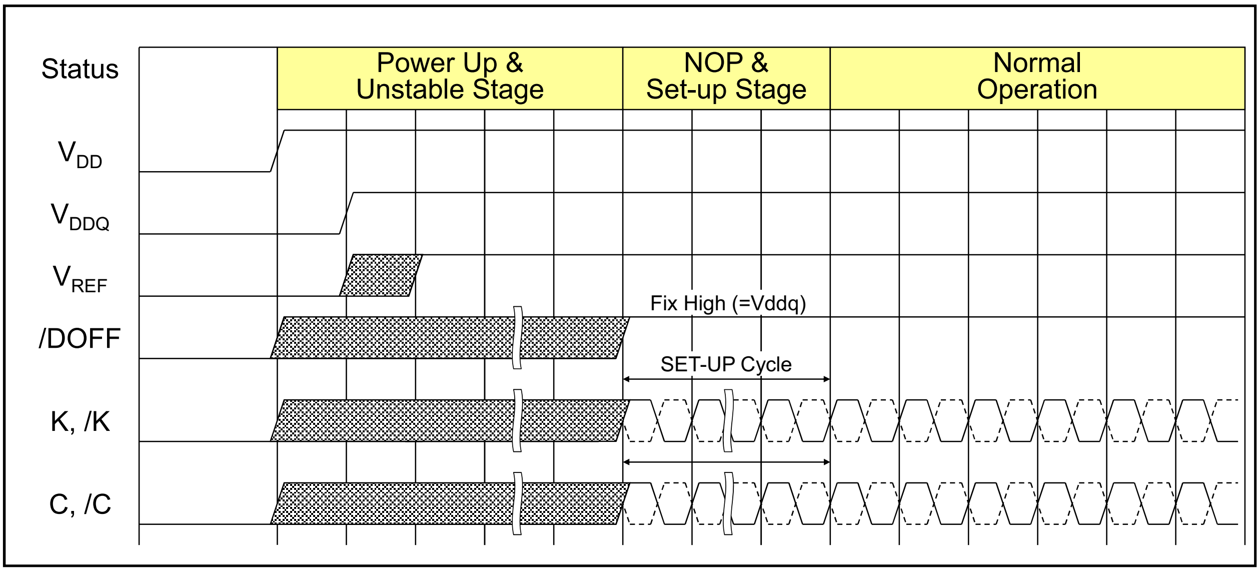
Power-up and Initialization Sequence

- V_{DD} must be stable before K, /K clocks are applied.
- Recommended voltage application sequence : $V_{SS} \rightarrow V_{DD} \rightarrow V_{DDQ}$ & $V_{REF} \rightarrow V_{IN}$. (0 V to V_{DD}, V_{DDQ} < 200 ms)
- Apply V_{REF} after V_{DDQ} or at the same time as V_{DDQ}.
- Then execute either one of the following three sequences.

1. Single Clock Mode (C and /C tied high)
   - Drive /DOFF high (/DOFF can be tied high from the start).
   - Then provide stable clocks (K, /K) for at least 1024 cycles (II series) or 20 us (II+ series).
     These meet the QDR common specification of 20 us.
     When the operating frequency is less than 180 MHz, 2048 cycles are required (II series).



2. Double Clock Mode (C and /C control outputs) (II series only)
   - Drive /DOFF high (/DOFF can be tied high from the start)
   - Then provide stable clocks (K, /K , C, /C) for at least 1024 cycles (II series).
     This meets the QDR common specification of 20 us.
     When the operating frequency is less than 180 MHz, 2048 cycles are required (II series).



3. DLL/PLL Off Mode (/DOFF tied low)
   - In the "NOP and setup stage", provide stable clocks (K, /K) for at least 1024 cycles (II series) or 20 us (II+ series). These meet the QDR common specification of 20 us.

DLL/PLL Constraints

1. DLL/PLL uses K clock as its synchronizing input. The input should have low phase jitter which is specified as tKC var.

2. The lower end of the frequency at which the DLL/PLL can operate is 120 MHz. (Please refer to AC Characteristics table for detail.)

3. When the operating frequency is changed or /DOFF level is changed, setup cycles are required again.

Programmable Output Impedance

1. Output buffer impedance can be programmed by terminating the ZQ ball to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is 250 Ω typical. The total external capacitance of ZQ ball must be less than 7.5 pF.

K Truth Table

<table>
<tr><th>Operation</th><th>K</th><th>/R</th><th>/W</th><th colspan="4">D or Q</th></tr>
<tr><td rowspan="3">Write Cycle:
Load address, input write data on consecutive K and /K rising edges</td><td rowspan="3">↑</td><td rowspan="3">×</td><td rowspan="3">L</td><td colspan="4">Data in</td></tr>
<tr><td colspan="2">Input data</td><td>D(A+0)</td><td>D(A+1)</td></tr>
<tr><td colspan="2">Input clock</td><td>K(t)↑</td><td>/K(t)↑</td></tr>
<tr><td rowspan="5">Read Cycle:
Load address, output read data on consecutive C and /C rising edges</td><td rowspan="5">↑</td><td rowspan="5">L</td><td rowspan="5">×</td><td colspan="4">Data out</td></tr>
<tr><td colspan="2">Output data</td><td>Q(A+0)</td><td>Q(A+1)</td></tr>
<tr><td rowspan="3">Input clock for Q</td><td>RL*7=1.5</td><td>/C(t+1)↑</td><td>C(t+2)↑</td></tr>
<tr><td>RL=2.0</td><td>C(t+2)↑</td><td>/C(t+2)↑</td></tr>
<tr><td>RL=2.5</td><td>/C(t+2)↑</td><td>C(t+3)↑</td></tr>
<tr><td>NOP (No operation)</td><td>↑</td><td>H</td><td>H</td><td colspan="4">D = × or Q = High-Z</td></tr>
<tr><td>Standby (Clock stopped)</td><td>Stopped</td><td>×</td><td>×</td><td colspan="4">Previous state</td></tr>
</table>

Notes:

1. H: high level, L: low level, ×: don't care, ↑: rising edge.
2. Data inputs are registered at K and /K rising edges. Data outputs are delivered at C and /C rising edges, except if C and /C are high, then data outputs are delivered at K and /K rising edges.
3. /R and /W must meet setup/hold times around the rising edges (low to high) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in high-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. When clocks are stopped, the following cases are recommended; the case of K = low, /K = high, C = low and /C = high, or the case of K = high, /K = low, C = high and /C = low. This condition is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. RL = Read Latency (unit = cycle).

Byte Write Truth Table (x 36)

Operation	K	/K	/BW0	/BW1	/BW2	/BW3
Write D0 to D35	↑	-	L	L	L	L
	-	↑	L	L	L	L
Write D0 to D8	↑	-	L	H	H	H
	-	↑	L	H	H	H
Write D9 to D17	↑	-	H	L	H	H
	-	↑	H	L	H	H
Write D18 to D26	↑	-	H	H	L	H
	-	↑	H	H	L	H
Write D27 to D35	↑	-	H	H	H	L
	-	↑	H	H	H	L
Write nothing	↑	-	H	H	H	H
	-	↑	H	H	H	H

Notes:
1. H: high level, L: low level, ↑: rising edge.
2. Assumes a WRITE cycle was initiated. /BWx can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Byte Write Truth Table (x 18)

Operation	K	/K	/BW0	/BW1
Write D0 to D17	↑	-	L	L
	-	↑	L	L
Write D0 to D8	↑	-	L	H
	-	↑	L	H
Write D9 to D17	↑	-	H	L
	-	↑	H	L
Write nothing	↑	-	H	H
	-	↑	H	H

Notes:
1. H: high level, L: low level, ↑: rising edge.
2. Assumes a WRITE cycle was initiated. /BWx can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

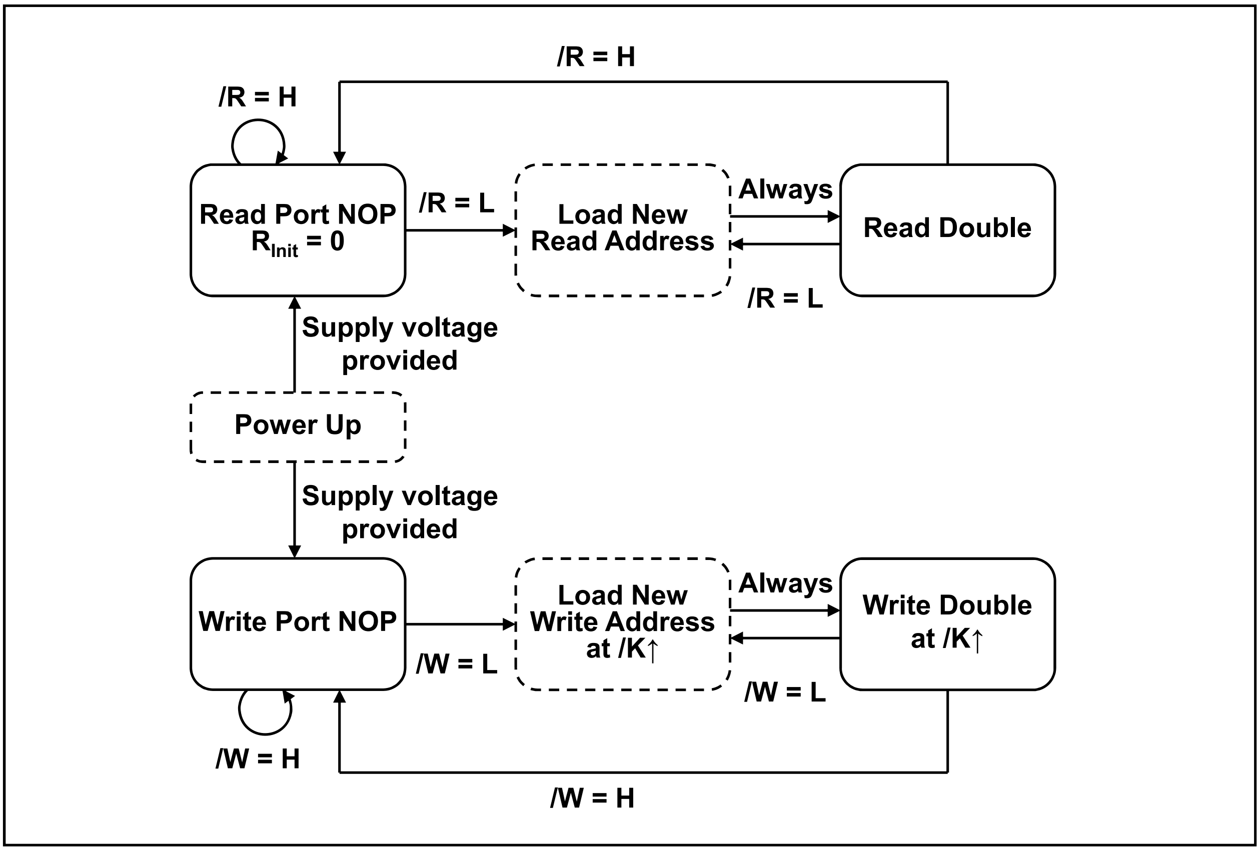
Byte Write Truth Table (x 9)

Just Reference except R1Q2A**09 series

Operation	K	/K	/BW
Write D0 to D8	↑	-	L
	-	↑	L
Write nothing	↑	-	H
	-	↑	H

Notes:
1. H: high level, L: low level, ↑: rising edge.
2. Assumes a WRITE cycle was initiated. /BWx can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



Notes:

1. The address is concatenated with one additional internal LSB to facilitate burst operation. The address order is always fixed as: xxx…xxx+0, xxx…xxx+1.
   Bus cycle is terminated at the end of this sequence (burst count = 2).
2. Read and write state machines can be active simultaneously.
3. State machine control timing sequence is controlled by K.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Input voltage on any ball	V_{IN}	–0.5 to V_{DD} + 0.5 (2.5 V max.)	V	1, 4
Input/output voltage	$V_{I/O}$	–0.5 to V_{DDQ} + 0.5 (2.5 V max.)	V	1, 4
Core supply voltage	V_{DD}	–0.5 to 2.5	V	1, 4
Output supply voltage	V_{DDQ}	–0.5 to V_{DD}	V	1, 4
Junction temperature	Tj	+125 (max)	°C	5
Storage temperature	T_{STG}	–55 to +125	°C	

Notes:
1. All voltage is referenced to V_{SS}.
2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
4. The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF} then V_{IN}. Remember, according to the Absolute Maximum Ratings table, V_{DDQ} is not to exceed 2.5 V, whatever the instantaneous value of V_{DDQ}.
5. Some method of cooling or airflow should be considered in the system. (Especially for high frequency or ODT parts)

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage -- core	V_{DD}	1.7	1.8	1.9	V	1
Power supply voltage -- I/O	V_{DDQ}	1.4	1.5	V_{DD}	V	1, 2
Input reference voltage -- I/O	V_{REF}	0.68	0.75	0.95	V	3
Input high voltage	$V_{IH\ (DC)}$	V_{REF} + 0.1	—	V_{DDQ} + 0.3	V	1, 4, 5
Input low voltage	$V_{IL\ (DC)}$	–0.3	—	V_{REF} – 0.1	V	1, 4, 5

Notes:
1. At power-up, V_{DD} and V_{DDQ} are assumed to be a linear ramp from 0V to V_{DD}(min.) or V_{DDQ}(min.) within 200ms. During this time $V_{DDQ} < V_{DD}$ and $V_{IH} < V_{DDQ}$.
   During normal operation, V_{DDQ} must not exceed V_{DD}.
2. Please pay attention to Tj not to exceed the temperature shown in the absolute maximum ratings table due to current from V_{DDQ}.
3. Peak to peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.
4. These are DC test criteria. The AC V_{IH} / V_{IL} levels are defined separately to measure timing parameters.
5. Overshoot: $V_{IH\ (AC)} \leq V_{DDQ} + 0.5$ V for $t \leq t_{KHKH}/2$
   Undershoot: $V_{IL\ (AC)} \geq -0.5$ V for $t \leq t_{KHKH}/2$
   During normal operation, $V_{IH(DC)}$ must not exceed V_{DDQ} and $V_{IL(DC)}$ must not be lower than V_{SS}.

DC Characteristics

(Ta = 0 ~ +70°C @ R1Q*A*****BG-**R** series, Ta = -40 ~ +85°C @ R1Q*A*****BG-**I** series)
(V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.5V, V_{REF} = 0.75V)

Operating Supply Current (Write / Read)

Symbol = I_{DD}. Unit = mA. See Notes 1, 2 and 3 in the page after next.

							QDR II+ / DDR II+						QDR II / DDR II			
No	Product Type	Burst Length	Latency (Cycle)	ODT	Organi-zation	Frequency (max) (MHz)	533	500	450	400	375	333	333	300	250	200
						Cycle Time (min) (ns)	1.875	2.00	2.22	2.50	2.66	3.00	3.00	3.30	4.00	5.00
						Part Number ↓ yy →	-19	-20	-22	-25	-27	-30	-30	-33	-40	-50
1	QDRII	B2	1.5	No	x 9	R1Q2A7209ABv-yy									760	670
2					x18	R1Q2A7218ABv-yy									890	780
3					x36	R1Q2A7236ABv-yy									950	830
5		B4			x18	R1Q3A7218ABv-yy							880	820	730	
6					x36	R1Q3A7236ABv-yy							910	850	750	
8	DDRII	B2			x18	R1Q4A7218ABv-yy							750	700	630	
9					x36	R1Q4A7236ABv-yy							810	760	680	
11		B4			x18	R1Q5A7218ABv-yy							660	630	590	
12					x36	R1Q5A7236ABv-yy							700	670	630	
14	DDRII SIO	B2			x18	R1Q6A7218ABv-yy							750	700	630	
15					x36	R1Q6A7236ABv-yy							810	760	680	
17	QDRII+	B4	2.5	No	x18	R1QAA7218ABv-yy	1220	1160	1070							
18					x36	R1QAA7236ABv-yy	1280	1220	1130							
20	DDRII+	B2			x18	R1QBA7218ABv-yy	1030	990	920							
21					x36	R1QBA7236ABv-yy	1110	1060	990							
23		B4			x18	R1QCA7218ABv-yy	820	790	750							
24					x36	R1QCA7236ABv-yy	880	850	800							
26	QDRII+	B4	2.5	Yes	x18	R1QDA7218ABv-yy	1220	1160	1070							
27					x36	R1QDA7236ABv-yy	1280	1220	1130							
29	DDRII+	B2			x18	R1QEA7218ABv-yy	1030	990	920							
30					x36	R1QEA7236ABv-yy	1110	1060	990							
32		B4			x18	R1QFA7218ABv-yy	820	790	750							
33					x36	R1QFA7236ABv-yy	880	850	800							
35	QDRII+	B4	2.0	No	x18	R1QGA7218ABv-yy				980						
36					x36	R1QGA7236ABv-yy				1060						
38	DDRII+	B2			x18	R1QHA7218ABv-yy				850						
39					x36	R1QHA7236ABv-yy				910						
41		B4			x18	R1QJA7218ABv-yy				710						
42					x36	R1QJA7236ABv-yy				760						
44	QDRII+	B4	2.0	Yes	x18	R1QKA7218ABv-yy				980						
45					x36	R1QKA7236ABv-yy				1060						
47	DDRII+	B2			x18	R1QLA7218ABv-yy				850						
48					x36	R1QLA7236ABv-yy				910						
50		B4			x18	R1QMA7218ABv-yy				710						
51					x36	R1QMA7236ABv-yy				760						

Notes:
1. "v" represents the package size. If "v" = "G" then size is 15 x 17 mm, and if "v" = "B" then 13 x 15 mm.
2. "yy" represents the speed bin. "R1QAA7236ABG-20" can operate at 500 MHz(max) of frequency, for example.

Standby Supply Current (NOP)

Symbol = I_{SB1}. Unit = mA. See Notes 2, 4 and 5 in the next page.

No	Product Type	Burst Length	Latency (Cycle)	ODT	Organi-zation	Frequency (max) (MHz) / Cycle Time (min) (ns) / Part Number	QDR II+ / DDR II+						QDR II / DDR II			
						Frequency (max) (MHz)	533	500	450	400	375	333	333	300	250	200
						Cycle Time (min) (ns)	1.875	2.00	2.22	2.50	2.66	3.00	3.00	3.30	4.00	5.00
						Part Number ↓ yy →	-19	-20	-22	-25	-27	-30	-30	-33	-40	-50
1	QDRII	B2	1.5	No	x 9	R1Q 2 A72 09 A Bv-yy									570	510
2					x18	R1Q 2 A72 18 A Bv-yy									670	600
3					x36	R1Q 2 A72 36 A Bv-yy									710	630
5		B4			x18	R1Q 3 A72 18 A Bv-yy							630	590	520	
6					x36	R1Q 3 A72 36 A Bv-yy							650	610	540	
8	DDRII	B2			x18	R1Q 4 A72 18 A Bv-yy							650	610	560	
9					x36	R1Q 4 A72 36 A Bv-yy							710	670	610	
11		B4			x18	R1Q 5 A72 18 A Bv-yy							540	510	480	
12					x36	R1Q 5 A72 36 A Bv-yy							570	540	500	
14	DDRII SIO	B2			x18	R1Q 6 A72 18 A Bv-yy							650	610	560	
15					x36	R1Q 6 A72 36 A Bv-yy							710	670	610	
17	QDRII+	B4	2.5	No	x18	R1Q A A72 18 A Bv-yy	870	830	780							
18					x36	R1Q A A72 36 A Bv-yy	910	870	810							
20	DDRII+	B2			x18	R1Q B A72 18 A Bv-yy	870	840	780							
21					x36	R1Q B A72 36 A Bv-yy	960	920	860							
23		B4			x18	R1Q C A72 18 A Bv-yy	690	660	630							
24					x36	R1Q C A72 36 A Bv-yy	730	710	670							
26	QDRII+	B4	2.5	Yes	x18	R1Q D A72 18 A Bv-yy	870	830	780							
27					x36	R1Q D A72 36 A Bv-yy	910	870	810							
29	DDRII+	B2			x18	R1Q E A72 18 A Bv-yy	870	840	780							
30					x36	R1Q E A72 36 A Bv-yy	960	920	860							
32		B4			x18	R1Q F A72 18 A Bv-yy	690	660	630							
33					x36	R1Q F A72 36 A Bv-yy	730	710	670							
35	QDRII+	B4	2.0	No	x18	R1Q G A72 18 A Bv-yy				720						
36					x36	R1Q G A72 36 A Bv-yy				770						
38	DDRII+	B2			x18	R1Q H A72 18 A Bv-yy				720						
39					x36	R1Q H A72 36 A Bv-yy				790						
41		B4			x18	R1Q J A72 18 A Bv-yy				590						
42					x36	R1Q J A72 36 A Bv-yy				630						
44	QDRII+	B4	2.0	Yes	x18	R1Q K A72 18 A Bv-yy				720						
45					x36	R1Q K A72 36 A Bv-yy				770						
47	DDRII+	B2			x18	R1Q L A72 18 A Bv-yy				720						
48					x36	R1Q L A72 36 A Bv-yy				790						
50		B4			x18	R1Q M A72 18 A Bv-yy				590						
51					x36	R1Q M A72 36 A Bv-yy				630						

Notes:

1. "v" represents the package size. If "v" = "G" then size is 15 x 17 mm, and if "v" = "B" then 13 x 15 mm.
2. "yy" represents the speed bin. "R1QAA7236ABG-20" can operate at 500 MHz(max) of frequency, for example.

Leakage Currents & Output Voltage

Parameter	Symbol	Min	Max	Unit	Test condition	Notes
Input leakage current	I_{LI}	–2	2	μA		10
Output leakage current	I_{LO}	–5	5	μA		11
Output high voltage	V_{OH} (Low)	$V_{DDQ} - 0.2$	V_{DDQ}	V	$\lvert I_{OH} \rvert \leq 0.1$ mA	8, 9
	V_{OH}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	Note 6	8, 9
Output low voltage	V_{OL} (Low)	V_{SS}	0.2	V	$I_{OL} \leq 0.1$ mA	8, 9
	V_{OL}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	Note 7	8, 9

Notes:

1. All inputs (except ZQ, V_{REF}) are held at either V_{IH} or V_{IL}.
2. I_{OUT} = 0 mA. $V_{DD} = V_{DD}$ max, $t_{KHKH} = t_{KHKH}$ min.
3. Operating supply currents (I_{DD}) are measured at 100% bus utilization. I_{DD} of QDR family is current of device with 100% write and 100% read cycle. I_{DD} of DDR family is current of device with 100% write cycle (if I_{DD}(Write) > I_{DD}(Read)) or 100% read cycle (if I_{DD}(Write) < I_{DD}(Read)).
4. All address / data inputs are static at either $V_{IN} > V_{IH}$ or $V_{IN} < V_{IL}$.
5. Reference value. (Condition = NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.)
6. Outputs are impedance-controlled. $\lvert I_{OH} \rvert = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
7. Outputs are impedance-controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
8. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
9. HSTL outputs meet JEDEC HSTL Class I and Class II standards.
10. $0 \leq V_{IN} \leq V_{DDQ}$ for all input balls (except V_{REF}, ZQ, TCK, TMS, TDI ball).
    If R1QD, R1QE, R1QF, R1QK, R1QL, R1QM, R1QP series, balls with ODT do not follow this spec.
11. $0 \leq V_{OUT} \leq V_{DDQ}$ (except TDO ball), output disabled.

Thermal Resistance

Parameter	Symbol	Airflow	Typ	Unit	Test condition	Notes
Junction to Ambient	θ_{JA}	1 m/s	11.0	°C/W	EIA/JEDEC JESD51	1
Junction to Case	θ_{JC}	-	4.4			

Notes:

1. These parameters are calculated under the condition. These are reference values.
2. $Tj = Ta + \theta_{JA} \times Pd$

   $Tj = Tc + \theta_{JC} \times Pd$

   where

   Tj : junction temperature when the device has achieved a steady-state after application of Pd (°C)

   Ta : ambient temperature (°C)

   Tc : temperature of external surface of the package or case (°C)

   θ_{JA} : thermal resistance from junction-to-ambient (°C/W)

   θ_{JC} : thermal resistance from junction-to-case (package) (°C/W)

   Pd : power dissipation that produced change in junction temperature (W) (cf.JESD51-2A)

Capacitance

(Ta = +25°C, Frequency = 1.0MHz, V_{DD} = 1.8V, V_{DDQ} = 1.5V)

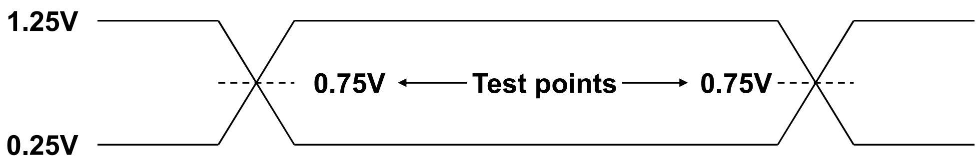
Parameter	Symbol	Min	Typ	Max	Unit	Test condition	Notes
Input capacitance (SA, /R, /W, /BW, D(separate))	C_{IN}	—	4	5	pF	V_{IN} = 0 V	1, 2
Clock input capacitance (K, /K, C, /C)	C_{CLK}	—	4	5	pF	V_{CLK} = 0 V	1, 2
Output capacitance (Q(separate), DQ(common), CQ, /CQ)	$C_{I/O}$	—	5	6	pF	$V_{I/O}$ = 0 V	1, 2

Notes:

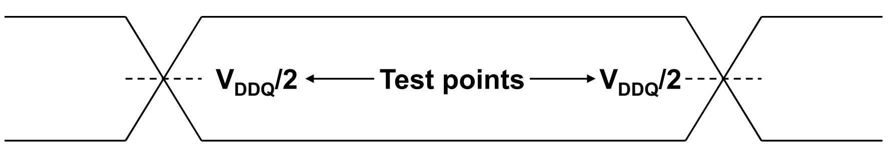
1. These parameters are sampled and not 100% tested.
2. Except JTAG (TCK, TMS, TDI, TDO) pins.

AC Test Conditions

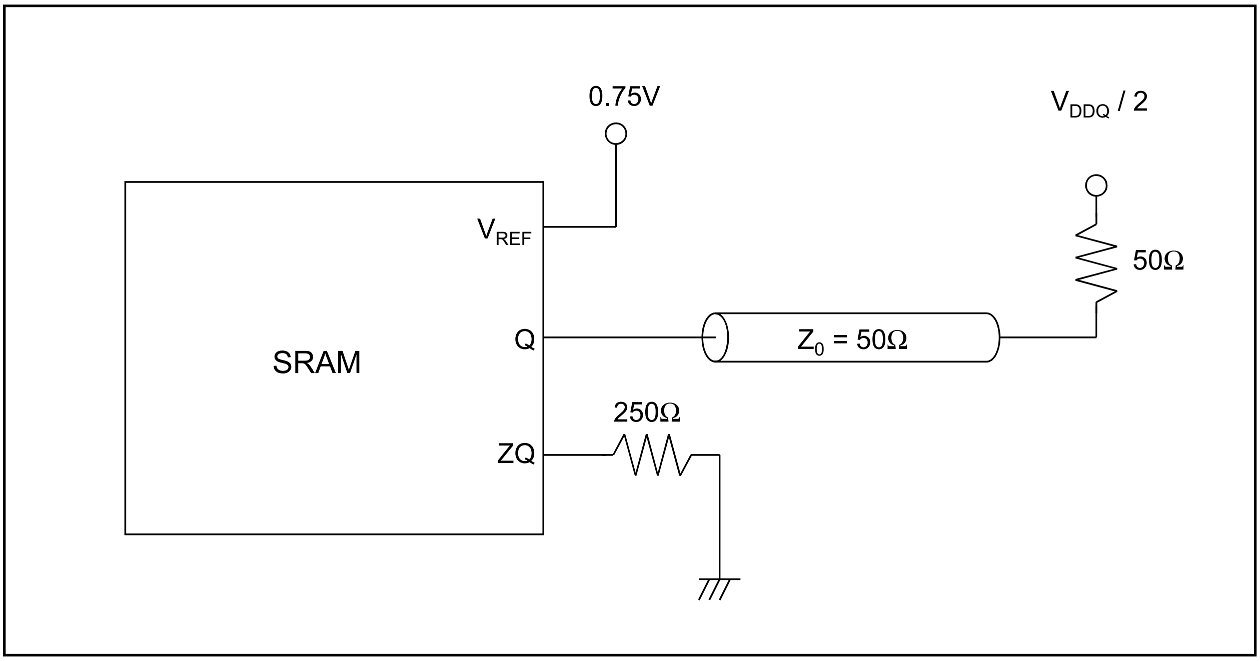
Input waveform (Rise/fall time ≤ 0.3 ns)



Output waveform



Output load conditions



AC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	$V_{IH\,(AC)}$	V_{REF} + 0.2	—	—	V	1, 2, 3, 4
Input low voltage	$V_{IL\,(AC)}$	—	—	V_{REF} – 0.2	V	1, 2, 3, 4

Notes:

1. All voltages referenced to V_{SS} (GND).
   During normal operation, V_{DDQ} must not exceed V_{DD}.
2. These conditions are for AC functions only, not for AC parameter test.
3. Overshoot: $V_{IH\,(AC)} \le V_{DDQ} + 0.5$ V for $t \le t_{KHKH}/2$
   Undershoot: $V_{IL\,(AC)} \ge -0.5$ V for $t \le t_{KHKH}/2$
   Control input signals may not have pulse widths less than t_{KHKL} (min) or operate at cycle rates less than t_{KHKH} (min).
4. To maintain a valid level, the transitioning edge of the input must:
   a. Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL\,(AC)}$ or $V_{IH\,(AC)}$.
   b. Reach at least the target AC level.
   c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL\,(DC)}$ or $V_{IH\,(DC)}$.

AC Characteristics (QDR-II, DDR-II series)

(Ta = 0 ~ +70°C @ R1Q*A*****BG-**R** series)
(Ta = -40 ~ +85°C @ R1Q*A*****BG-**I** series)
(V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.5V, V_{REF} = 0.75V)

Parameter	Symbol	-30		-33		-40		-50		—		—		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock															
Average clock cycle time (K, /K, C, /C)	t_{KHKH}	3.00	8.40	3.30	8.40	4.00	8.40	5.00	8.40	—	—	—	—	ns	8
Clock high time (K, /K, C, /C)	t_{KHKL}	1.20	—	1.32	—	1.60	—	2.00	—	—	—	—	—	ns	
Clock low time (K, /K, C, /C)	t_{KLKH}	1.20	—	1.32	—	1.60	—	2.00	—	—	—	—	—	ns	
Clock to /clock (K to /K, C to /C)	$t_{KH/KH}$	1.35	—	1.49	—	1.80	—	2.20	—	—	—	—	—	ns	
/Clock to clock (/K to K, /C to C)	$t_{/KHKH}$	1.35	—	1.49	—	1.80	—	2.20	—	—	—	—	—	ns	
Clock to data clock (K to C, /K to /C)	t_{KHCH}	0	1.35	0	1.49	0	1.80	0	2.20	—	—	—	—	ns	
DLL/PLL Timing															
Clock phase jitter (K, /K, C, /C)	t_{KC} var	—	0.20	—	0.20	—	0.20	—	0.20	—	—	—	—	ns	3
Lock time (K, C)	t_{KC} lock	1024	—	1024	—	1024	—	1024	—	—	—	—	—	Cy-cle	2
K static to DLL/PLL reset	t_{KC} reset	30	—	30	—	30	—	30	—	—	—	—	—	ns	7
Output Times															
C, /C high to output valid	t_{CHQV}	—	0.45	—	0.45	—	0.45	—	0.45	—	—	—	—	ns	9
C, /C high to output hold	t_{CHQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	—	—	—	—	ns	9
C, /C high to echo clock valid	t_{CHCQV}	—	0.45	—	0.45	—	0.45	—	0.45	—	—	—	—	ns	9
C, /C high to echo clock hold	t_{CHCQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	—	—	—	—	ns	9
CQ, /CQ high to output valid	t_{CQHQV}	—	0.25	—	0.27	—	0.30	—	0.35	—	—	—	—	ns	4, 7
CQ, /CQ high to output hold	t_{CQHQX}	–0.25	—	–0.27	—	–0.30	—	–0.35	—	—	—	—	—	ns	4, 7
C, /C high to output high-Z	t_{CHQZ}	—	0.45	—	0.45	—	0.45	—	0.45	—	—	—	—	ns	5, 6, 9
C, /C high to output low-Z	t_{CHQX1}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	—	—	—	—	ns	5, 9
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Parameter	Symbol	-30		-33		-40		-50		—		—		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Setup Times															
Address valid to K rising edge	t_{AVKH} for R1Q2	—	—	—	—	0.35	—	0.40	—	—	—	—	—	ns	1
	t_{AVKH} for R1Q3/4/5/6	0.40	—	0.40	—	0.50	—	0.60	—	—	—	—	—		
Control inputs valid to K rising edge	t_{IVKH} for R1Q2	—	—	—	—	0.35	—	0.40	—	—	—	—	—	ns	1
	t_{IVKH} for R1Q3/4/5/6	0.40	—	0.40	—	0.50	—	0.60	—	—	—	—	—		
Data-in valid to K, /K rising edge	t_{DVKH}	0.28	—	0.30	—	0.35	—	0.40	—	—	—	—	—	ns	1
Hold Times															
K rising edge to address hold	t_{KHAX} for R1Q2	—	—	—	—	0.35	—	0.40	—	—	—	—	—	ns	1
	t_{KHAX} for R1Q3/4/5/6	0.40	—	0.40	—	0.50	—	0.60	—	—	—	—	—		
K rising edge to control inputs hold	t_{KHIX} for R1Q2	—	—	—	—	0.35	—	0.40	—	—	—	—	—	ns	1
	t_{KHIX} for R1Q3/4/5/6	0.40	—	0.40	—	0.50	—	0.60	—	—	—	—	—		
K, /K rising edge to data-in hold	t_{KHDX}	0.28	—	0.30	—	0.35	—	0.40	—	—	—	—	—	ns	1

Notes:

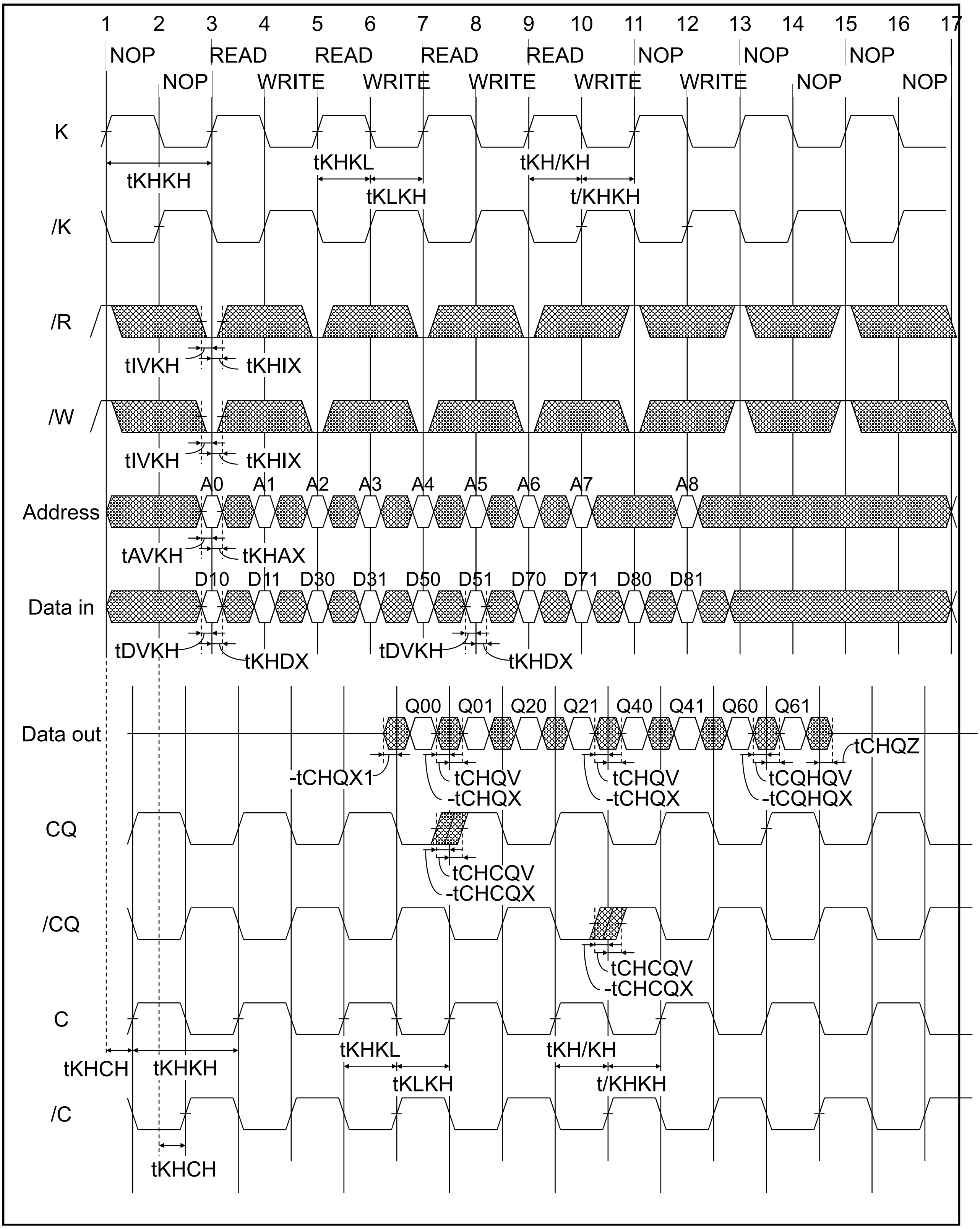
1. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.
2. V_{DD} and V_{DDQ} slew rate must be less than 0.1 V DC per 50 ns for DLL/PLL lock retention. DLL/PLL lock time begins once V_{DD} , V_{DDQ} and input clock are stable.
   It is recommended that the device is kept inactive during these cycles.
   This specification meets the QDR common spec. of 20 us.
3. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
4. Echo clock is very tightly controlled to data valid / data hold. By design, there is a ±0.1 ns variation from echo clock to data. The datasheet parameters reflect tester guardbands and test setup variations.
5. Transitions are measured ±100 mV from steady-state voltage.
6. At any given voltage and temperature t_{CHQZ} is less than t_{CHQX1} and t_{CHQV}.
7. These parameters are sampled.
8. When x18 and x36 configuration except QDRII-B2 are operated at less than 180MHz, DLL/PLL should be disabled (/DOFF=L). Please contact Renesas if these devices are always used at less than 180MHz with DLL/PLL operation.
9. t_{CHQV}, t_{CHQX}, t_{CHCQV}, t_{CHCQX}, t_{CHQZ}, t_{CHQX1} spec of R1Q3A and R1Q4A series is determined by the actual frequency regardless of Part Number (Marking Name). The following is the spec for the actual frequency.
   t_{CHQV}, t_{CHCQV}, t_{CHQZ} = 0.45 ns for $\geq$ 200 MHz and 0.50 ns for < 200 MHz
   t_{CHQX}, t_{CHCQX}, t_{CHQX1} = -0.45 ns for $\geq$ 200 MHz and -0.50 ns for < 200 MHz

Remarks:

1. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.
2. Control input signals may not be operated with pulse widths less than t_{KHKL} (min).
3. If C, /C are tied high, K, /K become the references for C, /C timing parameters.
4. V_{DDQ} is +1.5 V DC. V_{REF} is +0.75 V DC.
5. Control signals are /R, /W (QDR series), /LD, R-/W (DDR series), /BW, /BW0, /BW1, /BW2 and /BW3. Setup and hold times of /BWx signals must be the same as those of Data-in signals.

Timing Waveforms

Read and Write Timing (QDRII, B2, Read Latency = 1.5 cycle)



Notes:

1. Q00 refers to output from address A0+0. Q01 refers to output from the next internal burst address following A0, i.e., A0+1.
2. Outputs are disabled (high-Z) N clock cycle after the last read cycle. Here, N = Read Latency + Burst Length × 0.5.
3. In this example, if address A0 = A1, then data Q00 = D10, Q01 = D11. Write data is forwarded immediately as read results.
4. To control read and write operations, /BW signals must operate at the same timing as Data-in signals.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs.
TDI and TMS are internally pulled up and may be unconnected, or may be connected to VDD through a pull up resistor.
TDO should be left unconnected.

Test Access Port (TAP) Pins

Symbol I/O	Pin assignments	Description	Notes
TCK	2R	Test clock input. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.	
TMS	10R	Test mode select. This is the command input for the TAP controller state machine.	
TDI	11R	Test data input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.	
TDO	1R	Test data output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.	

Notes:
The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on SRAM POWER-UP.

TAP DC Operating Characteristics

(Ta = 0 ~ +70°C @ R1Q*A*****BG-**R** series)
(Ta = -40 ~ +85°C @ R1Q*A*****BG-**I** series)
(V_{DD} = 1.8V ±0.1V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	+1.3	—	V_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	+0.5	V	
Input leakage current	I_{LI}	–5.0	—	+5.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
Output leakage current	I_{LO}	–5.0	—	+5.0	µA	0 V ≤ V_{IN} ≤ V_{DD}, output disabled
Output low voltage	V_{OL1}	—	—	0.2	V	I_{OLC} = 100 µA
	V_{OL2}	—	—	0.4	V	I_{OLT} = 2 mA
Output high voltage	V_{OH1}	1.6	—	—	V	$\lvert I_{OHC}\rvert$ = 100 µA
	V_{OH2}	1.4	—	—	V	$\lvert I_{OHT}\rvert$ = 2 mA

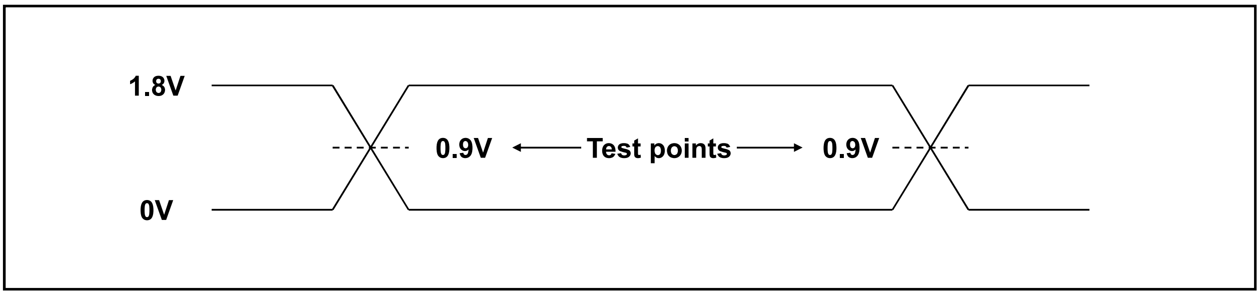
Notes:

1. All voltages referenced to V_{SS} (GND).
2. At power-up, V_{DD} and V_{DDQ} are assumed to be a linear ramp from 0V to V_{DD}(min.) or V_{DDQ}(min.) within 200ms. During this time V_{DDQ} < V_{DD} and V_{IH} < V_{DDQ}.
   During normal operation, V_{DDQ} must not exceed V_{DD}.

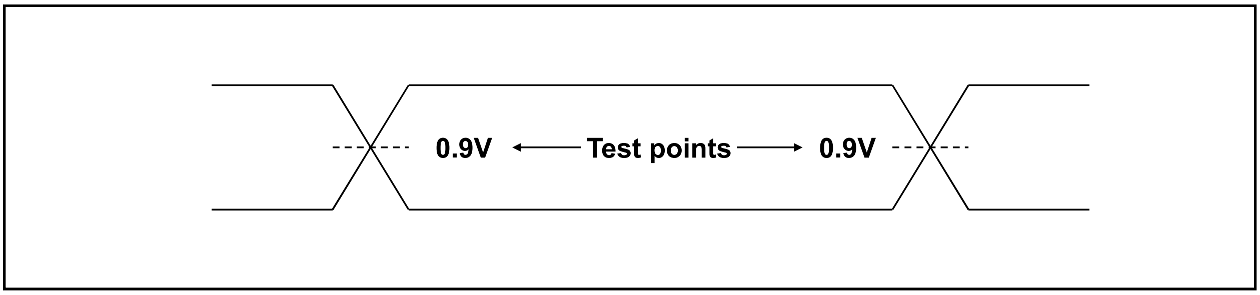
TAP AC Test Conditions

Parameter	Symbol	Conditions	Unit	Notes
Input timing measurement reference levels	V_{REF}	0.9	V	
Input pulse levels	V_{IL}, V_{IH}	0 to 1.8	V	
Input rise/fall time	tr, tf	≤ 1.0	ns	
Output timing measurement reference levels		0.9	V	
Test load termination supply voltage (V_{TT})		0.9	V	
Output load		See figures		

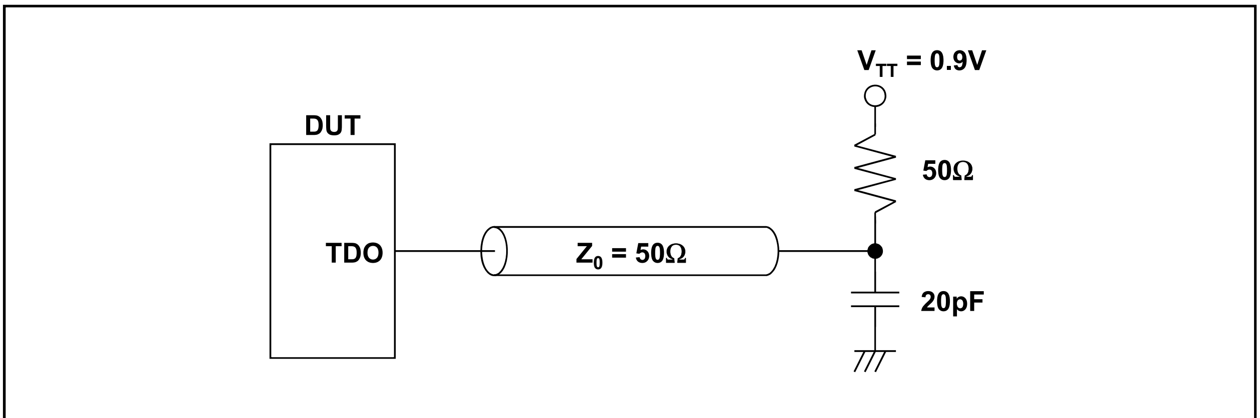
Input waveform



Output waveform



Output load condition



External Load at Test

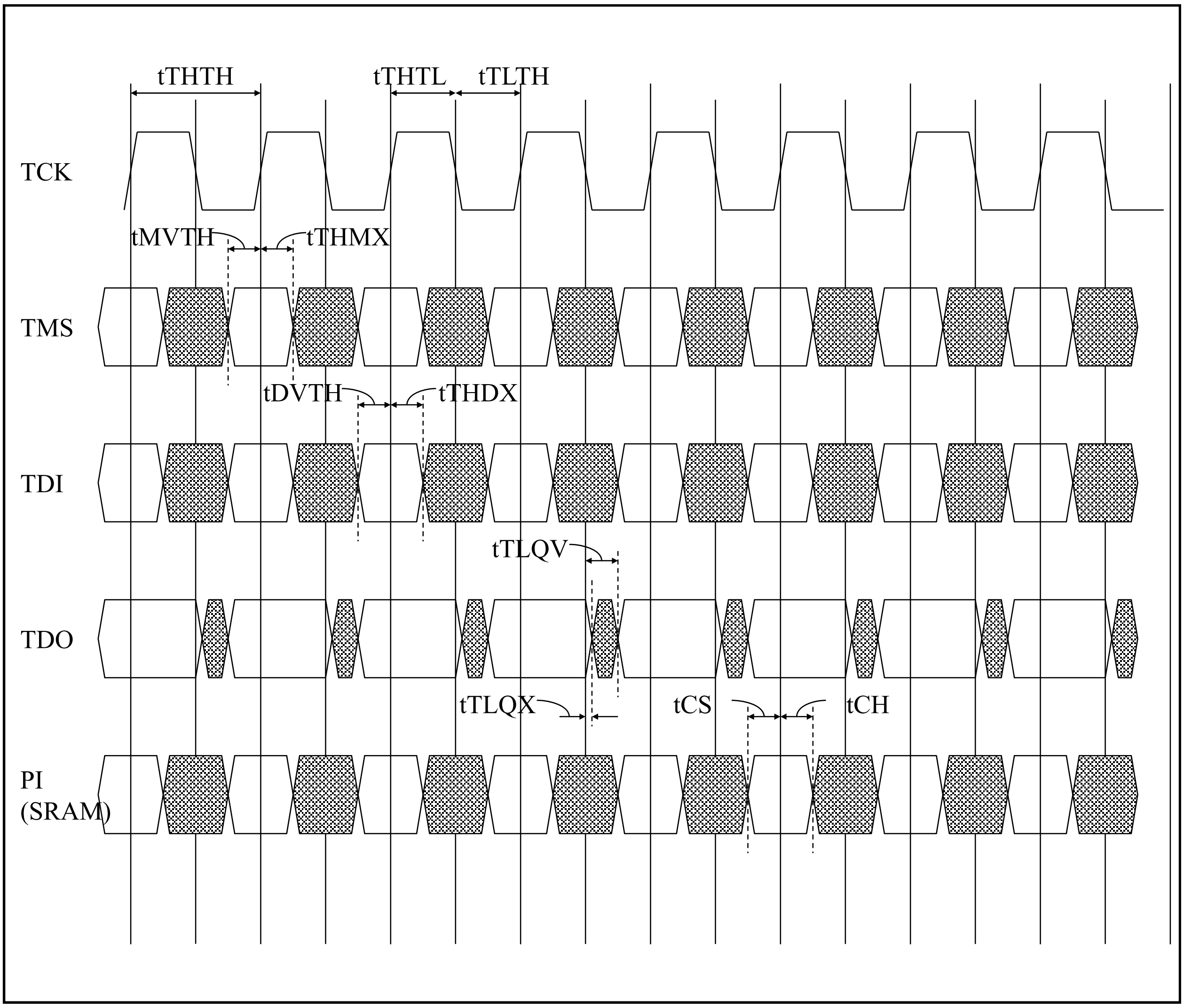
TAP AC Operating Characteristics

(Ta = 0 ~ +70°C @ R1Q*A*****BG-**R** series)
(Ta = -40 ~ +85°C @ R1Q*A*****BG-**I** series)
(V_{DD} = 1.8V ±0.1V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Test clock (TCK) cycle time	t_{THTH}	50	—	—	ns	
TCK high pulse width	t_{THTL}	20	—	—	ns	
TCK low pulse width	t_{TLTH}	20	—	—	ns	
Test mode select (TMS) setup	t_{MVTH}	5	—	—	ns	
TMS hold	t_{THMX}	5	—	—	ns	
Capture setup	t_{CS}	5	—	—	ns	1
Capture hold	t_{CH}	5	—	—	ns	1
TDI valid to TCK high	t_{DVTH}	5	—	—	ns	
TCK high to TDI invalid	t_{THDX}	5	—	—	ns	
TCK low to TDO unknown	t_{TLQX}	0	—	—	ns	
TCK low to TDO valid	t_{TLQV}	—	—	10	ns	

Notes:
1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

TAP Controller Timing Diagram



Test Access Port Registers

Register name	Length	Symbol	Notes
Instruction register	3 bits	IR [2:0]	
Bypass register	1 bit	BP	
ID register	32 bits	ID [31:0]	
Boundary scan register	109 bits	BS [109:1]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Description	Notes
0	0	0	EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary scan register cells at output balls are used to apply test vectors, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output driver is turned on and the PRELOAD data is driven onto the output balls.	1, 2, 3, 5
0	0	1	IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO balls in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.	
0	1	0	SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the RAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.	3, 4, 5
0	1	1	RESERVED	The RESERVED instructions are not implemented but are reserved for future use. Do not use these instructions.	
1	0	0	SAMPLE (/PRELOAD)	When the SAMPLE instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to SAMPLE metastable input will not harm the device, repeatable results cannot be expected. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO balls.	3, 5
1	0	1	RESERVED	-	
1	1	0	RESERVED	-	
1	1	1	BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.	

Notes:

1. Data in output register is not guaranteed if EXTEST instruction is loaded.
2. After performing EXTEST, power-up conditions are required in order to return part to normal operation.
3. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.
4. Clock recovery initialization cycles are required after boundary scan.
5. For R1QD, R1QE, R1QF, R1QK, R1QL, R1QM, R1QP series, ODT is disabled in EXTEST, SAMPLE-Z or SAMPLE mode.

Boundary Scan Order

Bit #	Ball ID	Signal names			Bit #	Ball ID	Signal names		
		x9	x18	x36			x9	x18	x36
1	6R	/C	/C	/C	36	10E	D3	D6	D6
2	6P	C	C	C	37	10D	NC	NC	D15
3	6N	SA	SA	SA	38	9E	NC	NC	Q15
4	7P	SA	SA	SA	39	10C	NC	Q7	Q7
5	7N	SA	SA	SA	40	11D	NC	D7	D7
6	7R	SA	SA	SA	41	9C	NC	NC	D16
7	8R	SA	SA	SA	42	9D	NC	NC	Q16
8	8P	SA	SA	SA	43	11B	Q4	Q8	Q8
9	9R	SA	SA	SA	44	11C	D4	D8	D8
10	11P	Q0	Q0	Q0	45	9B	NC	NC	D17
11	10P	D0	D0	D0	46	10B	NC	NC	Q17
12	10N	NC	NC	D9	47	11A	CQ	CQ	CQ
13	9P	NC	NC	Q9	48	10A	SA	SA	NC
14	10M	NC	Q1	Q1	49	9A	SA	SA	SA
15	11N	NC	D1	D1	50	8B	SA	SA	SA
16	9M	NC	NC	D10	51	7C	SA	SA	SA
17	9N	NC	NC	Q10	52	6C	SA	SA	SA
18	11L	Q1	Q2	Q2	53	8A	/R	/R	/R
19	11M	D1	D2	D2	54	7A	NC	NC	/BW1
20	9L	NC	NC	D11	55	7B	/BW	/BW0	/BW0
21	10L	NC	NC	Q11	56	6B	K	K	K
22	11K	NC	Q3	Q3	57	6A	/K	/K	/K
23	10K	NC	D3	D3	58	5B	NC	NC	/BW3
24	9J	NC	NC	D12	59	5A	NC	/BW1	/BW2
25	9K	NC	NC	Q12	60	4A	/W	/W	/W
26	10J	Q2	Q4	Q4	61	5C	SA	SA	SA
27	11J	D2	D4	D4	62	4B	SA	SA	SA
28	11H	ZQ	ZQ	ZQ	63	3A	SA	SA	SA
29	10G	NC	NC	D13	64	2A	SA	NC	NC
30	9G	NC	NC	Q13	65	1A	/CQ	/CQ	/CQ
31	11F	NC	Q5	Q5	66	2B	NC	Q9	Q18
32	11G	NC	D5	D5	67	3B	NC	D9	D18
33	9F	NC	NC	D14	68	1C	NC	NC	D27
34	10F	NC	NC	Q14	69	1B	NC	NC	Q27
35	11E	Q3	Q6	Q6	70	3D	NC	Q10	Q19

Boundary Scan Order

Bit #	Ball ID	Signal names			Bit #	Ball ID	Signal names		
		x9	x18	x36			x9	x18	x36
71	3C	NC	D10	D19	91	2L	Q7	Q15	Q24
72	1D	NC	NC	D28	92	3L	D7	D15	D24
73	2C	NC	NC	Q28	93	1M	NC	NC	D33
74	3E	Q5	Q11	Q20	94	1L	NC	NC	Q33
75	2D	D5	D11	D20	95	3N	NC	Q16	Q25
76	2E	NC	NC	D29	96	3M	NC	D16	D25
77	1E	NC	NC	Q29	97	1N	NC	NC	D34
78	2F	NC	Q12	Q21	98	2M	NC	NC	Q34
79	3F	NC	D12	D21	99	3P	Q8	Q17	Q26
80	1G	NC	NC	D30	100	2N	D8	D17	D26
81	1F	NC	NC	Q30	101	2P	NC	NC	D35
82	3G	Q6	Q13	Q22	102	1P	NC	NC	Q35
83	2G	D6	D13	D22	103	3R	SA	SA	SA
84	1H	/DOFF	/DOFF	/DOFF	104	4R	SA	SA	SA
85	1J	NC	NC	D31	105	4P	SA	SA	SA
86	2J	NC	NC	Q31	106	5P	SA	SA	SA
87	3K	NC	Q14	Q23	107	5N	SA	SA	SA
88	3J	NC	D14	D23	108	5R	SA	SA	SA
89	2K	NC	NC	D32	109	—	INTER-NAL	INTER-NAL	INTER-NAL
90	1K	NC	NC	Q32	—	—	—	—	—

Notes:

In boundary scan mode,

1. Clock balls (K, /K, C, /C) are referenced to each other and must be at opposite logic levels for reliable operation.
2. CQ and /CQ data are synchronized to the respective C and /C (except EXTEST, SAMPLE-Z).
3. If C and /C tied high, CQ is generated with respect to K and /CQ is generated with respect to /K (except EXTEST, SAMPLE-Z).

ID Register

-	Revision number (31 :29)			Type number (28 : 12)																	Vendor JEDEC code (11 : 1)											Start bit (0)
#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	R	R	R	0	C	M	M	M	A	W	W	0	1	Q	Q	Q	B	O	S	0	0	1	0	0	0	1	0	0	0	1	1	1

R	R	R	
0	0	0	Revison 0
0	0	1	Revison 1
0	1	0	Revison 2
0	1	1	Revison 3
:			:

C	
0	36M&72M w/o ODT, 144M,288M
1	36M&72M w/ ODT

M	M	M	
0	1	0	Density = 36Mb
0	1	1	Density = 72Mb
1	0	1	Density = 144Mb
1	1	0	Density = 288Mb

A	
0	144M&288M w/o ODT, 36M,72M
1	144M&288M w/ ODT

W	W	
0	0	x9
1	0	x18
1	1	x36

Q	
0	II (QDR-II, DDR-II)
1	II+ (QDR-II+, DDR-II+)

Q	
0	DDR
1	QDR

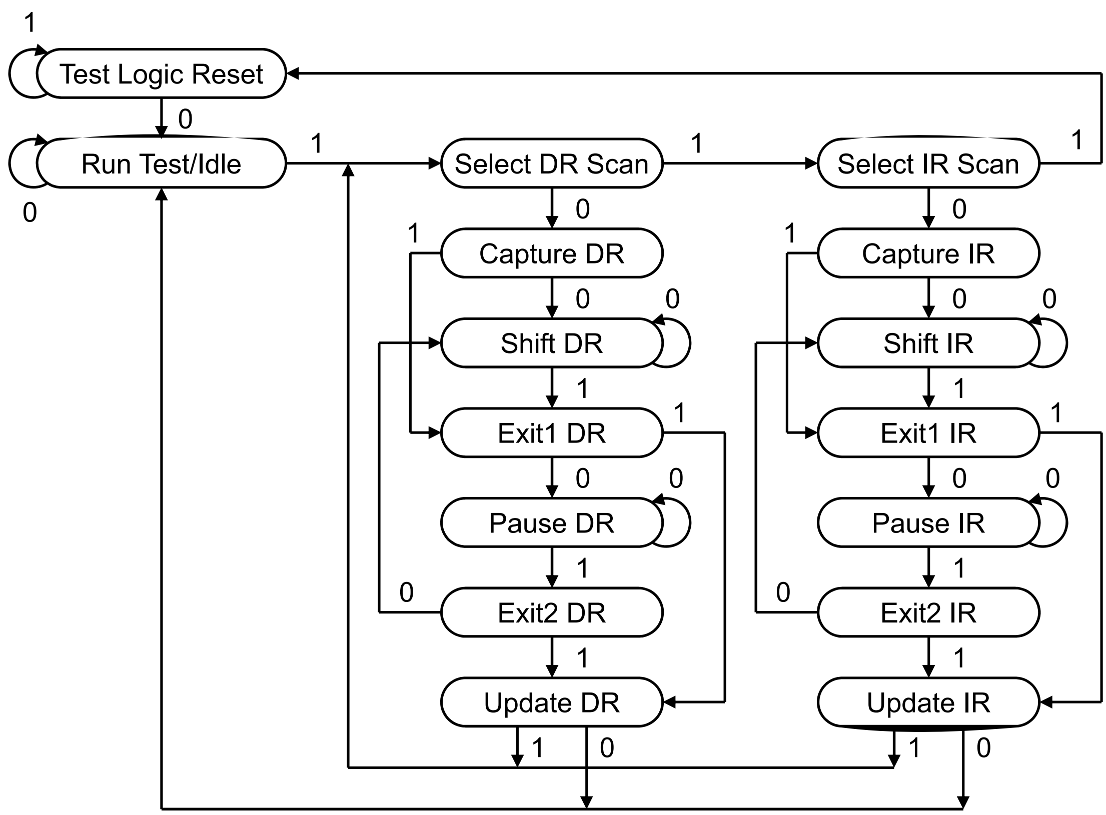
Q	
0	Latency=1.5 (@II), Latency=2.0 (@II+)
1	Latency=2.5 (@II+)

B	
0	Burst Length = 2 word burst
1	Burst Length = 4 word burst

O	
0	without ODT
1	with ODT

S	
0	Common I/O
1	Separate I/O

TAP Controller State Diagram



Notes:

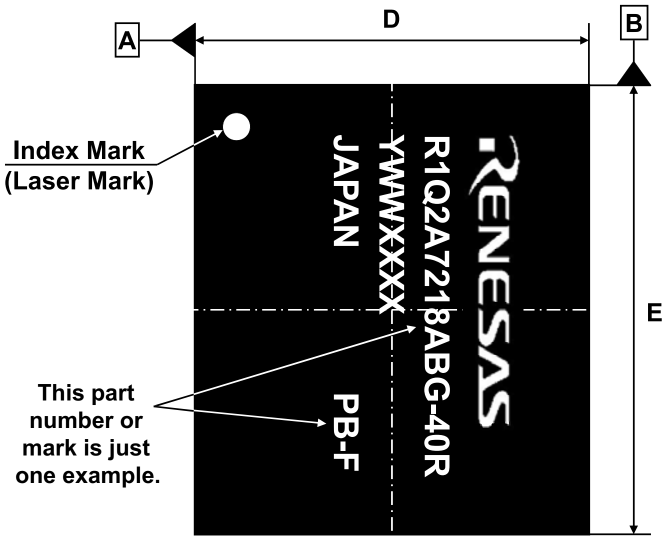
The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Dimensions and Marking Information

Both Pb parts and Pb-free parts are available.

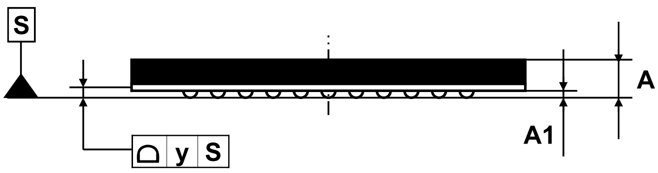
JEITA Package Code	Renesas Code	Previous Code	Mass (typ.)
P-LBGA165-15x17-1.00	PLBG0165FD-A	165FHE	0.6 g



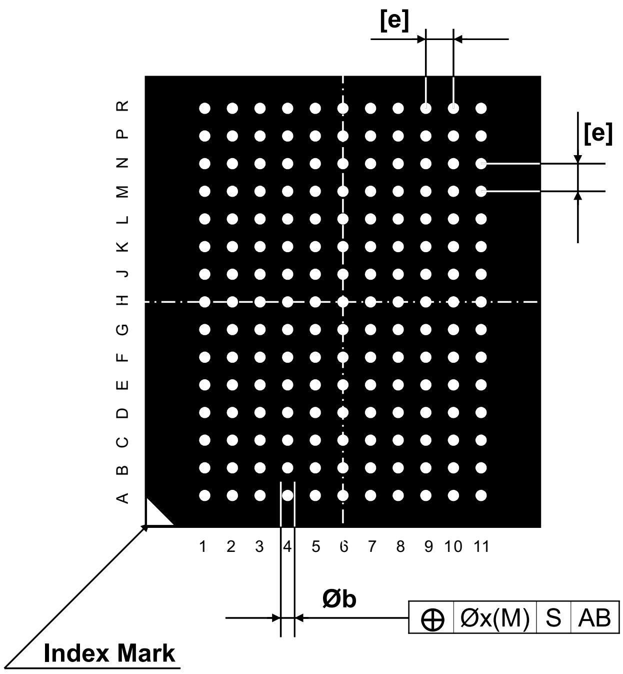
Top View

Marking Information

1st row : Vender name (RENESAS)
2nd row: Part number
3rd row : Y : Year code
WW : Week code
XXXX : Renesas internal use
4th row : Country name (JAPAN)
+ "None" --- Pb parts
+ "PB-F" --- Pb-free parts



Side View



Bottom View

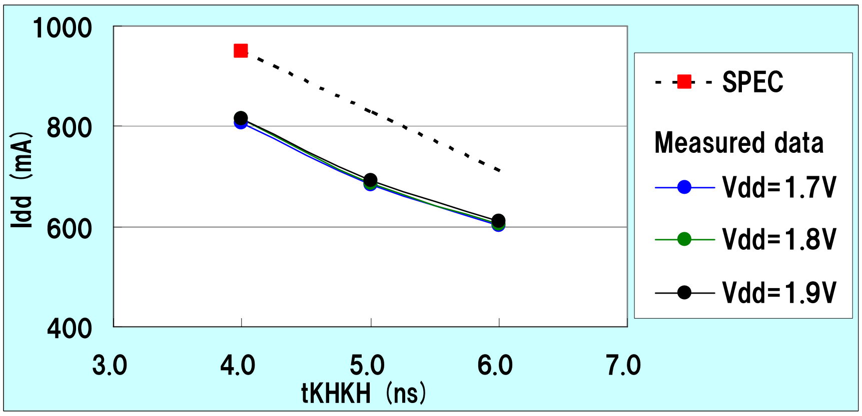
Reference Symbol	Dimension in mm		
	Min	Nom	Max
D	14.9	15.0	15.1
E	16.9	17.0	17.1
A	-	-	1.4
A1	0.27	0.32	0.37
[e]	-	1.0	-
b	0.45	0.5	0.55
x	-	-	0.2
y	-	-	0.15

Appendix

Example of DC/AC characteristics data

Parts Number : R1Q2A7236RBG-40R

IDD (Operating supply current) - tKHKH (Ta=70 degC)



tKHKH (Clock cycle time) Shmoo (Ta=70 degC)

```
        TIME
        1NS       2NS       3NS       4NS       5NS       6NS
Voltage +----+----+----+----+----+----+----+----+----+----+
2.00V   ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP
1.95V   ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP      P : Pass
1.90V   ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP        : SPEC
1.85V   ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP
1.80V   ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP
1.75V   ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP
1.70V   ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP
1.65V   ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP
1.60V   ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP
        +----+----+----+----+----+----+----+----+----+----+
        1NS       2NS       3NS       4NS       5NS       6NS
```

Vdd

tKHKH

tCHQV (C, /C high to output valid) Shmoo (Ta=70 degC)

```
        TIME
        0PS       100PS     200PS     300PS     400PS     500PS
Voltage +----+----+----+----+----+----+----+----+----+----+
2.00V   ....................... PPPPPPPPPPPPPPPPPPPPPPPPPPP
1.95V   .......................PPPPPPPPPPPPPPPPPPPPPPPPPPPP      P : Pass
1.90V   .......................PPPPPPPPPPPPPPPPPPPPPPPPPPPP        : SPEC
1.85V   ....................... PPPPPPPPPPPPPPPPPPPPPPPPPPP
1.80V   ....................... PPPPPPPPPPPPPPPPPPPPPPPPPPP
1.75V   .......................PPPPPPPPPPPPPPPPPPPPPPPPPPPP
1.70V   .......................PPPPPPPPPPPPPPPPPPPPPPPPPPPP
1.65V   ....................... PPPPPPPPPPPPPPPPPPPPPPPPPPP
1.60V   ....................... PPPPPPPPPPPPPPPPPPPPPPPPPPP
        +----+----+----+----+----+----+----+----+----+----+
        0PS       100PS     200PS     300PS     400PS     500PS
```

Vdd

tCHQV

Revision History (1)

Rev.	Date	#	Comment
Rev. 0.00a	'08.10.08	1	Initial issue.
Rev. 0.00b	'08.10.09	1	Corrected typos in "DC Characteristics": VOH/VOL= VDDQ/2±1.12 → ±0.12.
Rev. 0.00c	'08.11.19	1	Added "Speed Bin Table". Added "ODT timing chart" to QDRII+ and DDRII+ series.
Rev. 0.00d	'08.11.28	1	Corrected typos in "General Description": ODT pin = Q0～Qn → D0～Dn.
		2	Updated "Recommended DC Operating Conditions": Vref =0.68～0.95V → 0.7～0.8V (II+ series).
		3	Added comment to "Thermal Resistance" section: These are reference values.
Rev. 0.00e	'08.12.07	1	Added "Generation Number Table".
Rev. 0.00 f -1	'09.02.09	1	Changed Marking Name in "Part Number Definition Table".
		2	Added marking information to "Package Dimension Information" section.
		3	Corrected ODT On/Off timing in "ODT pin" table.
		4	Updated minimum frequency of QDRII+ and DDRII+ series.
		5	Changed pin name in "Pin Arrangement" of DDRII+ series: SA0/SA1 → NC.
		6	Added the row to "K Truth Table": RL=2.0 and RL=2.5.
Rev. 0.00g -1	'09.02.24	1	Updated SET-UP cycles: II+ series DLL lock time = 20us → 2048 cycle.
		2	Added comment to "ODT on/off Timing Chart" section: ODT on/off switching timings are edge aligned with CQ or /CQ.
		3	Updated "Thermal Resistance".
Rev. 0.00h	'09.03.04	1	Added "-50" speed bin to QDR II B2 x18/x36 series.
Rev. 0.00i	'09.06.15	1	Updated "Package Dimensions": Mass=0.7→0.6g, A(max)=1.46→1.4mm.
		2	Updated "Operating/Standby Supply Currents".
Rev. 0.01a	'09.10.25	1	Added comment to "Power-up and Initialization Sequence" section: Apply Vref after Vddq or at the same time as Vddq.
		2	Updated "Speed Bin Table".
Rev. 0.02a	'10.02.01	1	Added "Renesas QDR SRAM Homepage URL" to notes of front page.
		2	Updated "Power-up and Initialization Sequence".
		3	Updated "DLL Constraints".
		4	Updated "Operating Supply Current" and "Standby Supply Current"
		5	Updated "Thermal Resistance".
		6	Changed remarks of "AC Characteristics" on "Control signals".
Rev. 0.03a	'10.04.01	1	Changed company name, RENESAS logo and base color from those of Renesas Technology to Renesas Electronics.
		2	Changed vender name marking in "Package Dimensions and Marking Information" section.
		3	Added "A" generation to 72M series.
Rev. 0.04a	'10.06.10	1	Changed the pin description for NC pin.
		2	Changed note 4 of "TAP Controller Instruction Set": "Clock recovery initialization cycles are required after boundary scan"
Rev. 0.05a	'10.06.25	1	Changed Vddq range of II+ series: Vddq=1.5±0.1V → 1.4V ～ Vdd.
		2	Added Note.8 and Note.9 to AC Characteristics table for II+ series.
		3	Updated Speed Bin Table for 144M.
Rev. 0.05b	'10.07.02	1	Added Note.2 to Generation Number Table.
		2	Updated Speed Bin Table for 36M and 72M.
Rev. 0.05c	'10.07.24	1	Updated Operating Supply Current and Standby Supply Current Table for 36M and 72M.
Rev. 0.06a	'10.09.20	1	Changed Initialization Sequence: Initial cycle of II+ series = 2048cycles → 20us.
Rev. 0.07a	'10.10.06	1	Added Note.9 to AC Characteristics table for II series.
Rev. 0.07b	'10.10.30	1	Updated AC Characteristics for the series of RL=2.0.
		2	Updated Speed Bin Table for 72M/36M/144M.
		3	Added R1QNA, R1QPA series to 144M QDR lineup.
		4	Changed JTAG/ID Register(ID Code): #27="0": 36M&72M w/o ODT, 144M,288M "1": 36M&72M w/ ODT #23="0": 144M&288M w/o ODT, 36M,72M "1": 144M&288M w/ ODT #(26,25,24)="100"→"101"(144M), "101"→"110"(288M).

Revision History (2)

Rev.	Data	#	Comment
Rev.0.08a	11.05.23	1	Added Note.7 to tQVLD in AC Characteristics table for II+ series.
		2	Changed description of tQVLD in AC Characteristics table for RL=2 series: CQ high to QVLD valid → /CQ high to QVLD valid.
		3	Updated Remarks 4 of AC Characteristics table.
		4	Updated tKHKH(max) in AC Characteristics table for QDRII+ B2 series.
		5	Added 13 x15 mm package lineup to 36M II+ & 72M II/II+ series.
Rev.0.08b	11.07.17	1	Updated "Package Dimensions" for 13 x15 mm package.
		2	Updated "Thermal Resistance" for 13 x15 mm package.
		3	Changed Title: "Ordering Informaion" → "Part Number Definition"、"Speed Bin Table" → "Renesas **M QDR/DDR SRAM Lineup"
Rev.0.09a	11.09.14	1	Updated Specification for ODT Option 2.
Rev.0.10a	11.12.09	1	Updated Part Number Definition table.(Added Note.4)
Rev.0.10b	12.03.12	1	Updated Part Number Definition table.(Added definition to No.10-11)
Rev.0.10c	12.06.05	1	Updated URL for Renesas QDR SRAM Homepage.
Rev.0.11	13.01.15	1	Updated "Part Number Definition" for 13 x 15 mm Package

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