CYPRESS

# CY7C419/21/25/29/33

## 256/512 /1K /2K/4K x 9 Asynchronous FIFO

### Features

- **Asynchronous first-in first-out (FIFO) buffer memories**
- **256 x 9 (CY7C419)**
- **512 x 9 (CY7C421)**
- **1K x 9 (CY7C425)**
- **2K x 9 (CY7C429)**
- **4K x 9 (CY7C433)**
- **Dual-ported RAM cell**
- **High-speed 50.0-MHz read/write independent of depth/width**
- **Low operating power: $I_{CC}$ = 35 mA**
- **Empty and Full flags (Half Full flag in standalone)**
- **TTL compatible**
- **Retransmit in standalone**
- **Expandable in width**
- **PLCC, 7x7 TQFP, SOJ, 300-mil and 600-mil DIP**
- **Pin compatible and functionally equivalent to IDT7200, IDT7201, IDT7202, IDT7203, IDT7204, AM7200, AM7201, AM7202, AM7203, and AM7204**

### Functional Description

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, and CY7C432/3 are first-in first-out (FIFO) memories offered in 600-mil wide and 300-mil wide packages. They are, respectively, 256, 512, 1,024, 2,048, and 4,096 words by 9-bits wide.

Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

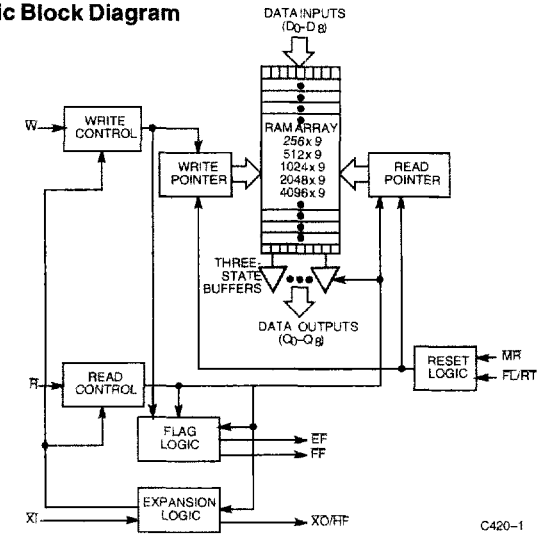
The read and write operations may be asynchronous; each can occur at a rate of 50.0 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

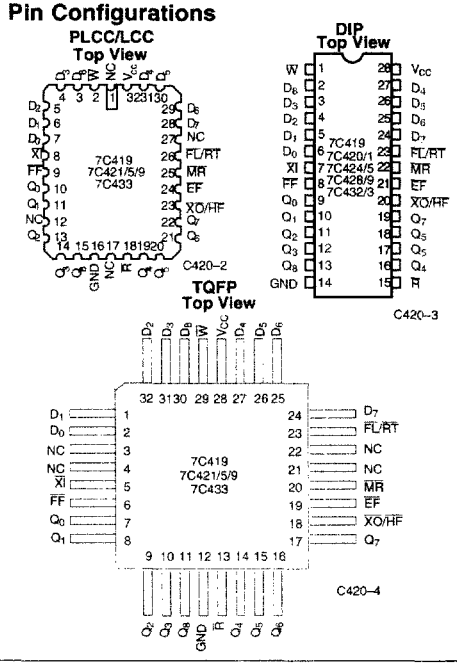
In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during retransmit, and then $\overline{R}$ is used to access the data.

The CY7C419, CY7C420, CY7C421, CY7C424, CY7C425, CY7C428, CY7C429, CY7C432, and CY7C433 are fabricated using an advanced 0.65-micron P-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout and guard rings.

## Logic Block Diagram




## Pin Configurations




## Selection Guide

| 256 x 9 | **7C419–10** | **7C419–15** | | | **7C419–30** | **7C419–40** | |
|---|---|---|---|---|---|---|---|
| 512 x 9 (600-mil only) | | | **7C420–20** | **7C420–25** | | **7C420–40** | **7C420–65** |
| 512 x 9 | **7C421–10** | **7C421–15** | **7C421–20** | **7C421–25** | **7C421–30** | **7C421–40** | **7C421–65** |
| 1K x 9 (600-mil only) | | | **7C424–20** | **7C424–25** | **7C424–30** | **7C424–40** | **7C424–65** |
| 1K x 9 | **7C425–10** | **7C425–15** | **7C425–20** | **7C425–25** | **7C425–30** | **7C425–40** | **7C425–65** |
| 2K x 9 (600-mil only) | | | **7C428–20** | | | | **7C428–65** |
| 2K x 9 | **7C429–10** | **7C429–15** | **7C429–20** | **7C429–25** | **7C429–30** | **7C429–40** | **7C429–65** |
| 4K x 9 (600-mil only) | | | | **7C432–25** | | **7C432–40** | |
| 4K x 9 | **7C433–10** | **7C433–15** | **7C433–20** | **7C433–25** | **7C433–30** | **7C433–40** | **7C433–65** |
| Frequency (MHz) | 50 | 40 | 33.3 | 28.5 | 25 | 20 | 12.5 |
| Maximum Access Time (ns) | 10 | 15 | 20 | 25 | 30 | 40 | 65 |
| $I_{CC1}$ (mA) | 35 | 35 | 35 | 35 | 35 | 35 | 35 |

## Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

Power Dissipation ..... 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2000V (per MIL–STD–883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature[1] | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to + 70°C | 5V ± 10% |
| Industrial | –40°C to +85°C | 5V ± 10% |
| Military | –55°C to +125°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range[2]

| Parameter | Description | Test Conditions | | 7C419–10, 15, 30, 40<br>7C420/1–10, 15, 20, 25, 30, 40, 65<br>7C424/5–10, 15, 20, 25, 30, 40, 65<br>7C428/9–10, 15, 20, 25, 30, 40, 65<br>7C432/3–10, 15, 20, 25, 30, 40, 65 | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –2.0 mA | | 2..4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | Com'l | 2.0 | $V_{CC}$ | V |
| | | | Mil/Ind | 2.2 | $V_{CC}$ | |
| $V_{IL}$ | Input LOW Voltage | | | Note 3 | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –10 | +10 | µA |
| $I_{OZ}$ | Output Leakage Current | $\overline{R}$ ≥ $V_{IH}$, GND ≤ $V_O$ ≤ $V_{CC}$ | | –10 | +10 | µA |
| $I_{OS}$ | Output Short Circuit Current[4] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | | –90 | mA |

## Electrical Characteristics Over the Operating Range[2] (continued)

| Parameter | Description | Test Conditions | | 7C419–10<br>7C421–10<br>7C425–10<br>7C429–10<br>7C433–10 | | 7C419–15<br>7C421–15<br>7C425–15<br>7C429–15<br>7C433–15 | | 7C420–20<br>7C421–20<br>7C424–20<br>7C425–20<br>7C428–20<br>7C429–20<br>7C433–20 | | 7C420–25<br>7C421–25<br>7C424–25<br>7C425–25<br>7C429–25<br>7C432–25<br>7C433–25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $I_{CC}$ | Operating Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA f = $f_{MAX}$ | Com'l | | 85 | | 65 | | 55 | | 50 | mA |
| | | | Mil/Ind | | | | 100 | | 90 | | 80 | |
| $I_{CC1}$ | Operating Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA F = 20 MHz | Com'l | | 35 | | 35 | | 35 | | 35 | mA |
| $I_{SB1}$ | Standby Current | All Inputs = $V_{IH}$ Min. | Com'l | | 10 | | 10 | | 10 | | 10 | mA |
| | | | Mil/Ind | | | | 15 | | 15 | | 15 | |
| $I_{SB2}$ | Power-Down Current | All Inputs ≥ $V_{CC}$ –0.2V | Com'l | | 5 | | 5 | | 5 | | 5 | mA |
| | | | Mil/Ind | | | | 8 | | 8 | | 8 | |

**Notes:**
1. $T_A$ is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. $V_{IL}$ (Min.) = –2.0V for pulse durations of less than 20 ns.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

## Electrical Characteristics Over the Operating Range[2] (continued)

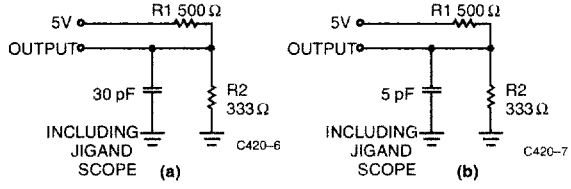
| Parameter | Description | Test Conditions | | 7C419–30 7C421–30 7C424–30 7C425–30 7C429–30 7C433–30 Min. | Max. | 7C419–40 7C420–40 7C421–40 7C424–40 7C425–40 7C429–40 7C432–40 7C433–40 Min. | Max. | 7C420–65 7C421–65 7C424–65 7C425–65 7C428–65 7C429–65 7C433–65 Min. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Operating Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA $f = f_{MAX}$ | Com'l | | 40 | | 35 | | 35 | mA |
| | | | Mil/Ind | | 75 | | 70 | | 65 | |
| $I_{CC1}$ | Operating Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA F = 20 MHz | Com'l | | 35 | | 35 | | 35 | mA |
| $I_{SB1}$ | Standby Current | All Inputs = $V_{IH}$ Min. | Com'l | | 10 | | 10 | | 10 | mA |
| | | | Mil | | 15 | | 15 | | 15 | |
| $I_{SB2}$ | Power-Down Current | All Inputs ≥ $V_{CC}$ −0.2V | Com'l | | 5 | | 5 | | 5 | mA |
| | | | Mil | | 8 | | 8 | | 8 | |

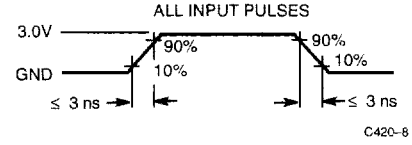
## Capacitance[5]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 4.5V | 6 | pF |
| $C_{OUT}$ | Output Capacitance | | 6 | pF |

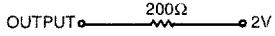
**Note:**
5. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms




Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over the Operating Range[6, 7]

| Parameter | Description | 7C419–10 7C421–10 7C425–10 7C429–10 7C433–10 | | 7C419–15 7C421–15 7C425–15 7C429–15 7C433–15 | | 7C420–20 7C421–20 7C424–20 7C425–20 7C428–20 7C429–20 7C433–20 | | 7C420–25 7C421–25 7C424–25 7C425–25 7C429–25 7C432–25 7C433–25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 20 | | 25 | | 30 | | 35 | | ns |
| $t_A$ | Access Time | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{RR}$ | Read Recovery Time | 10 | | 10 | | 10 | | 10 | | ns |
| $t_{PR}$ | Read Pulse Width | 10 | | 15 | | 20 | | 25 | | ns |
| $t_{LZR}$[5,8] | Read LOW to Low Z | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{DVR}$[8,9] | Data Valid After Read HIGH | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{HZR}$[5,8,9] | Read HIGH to High Z | | 15 | | 15 | | 15 | | 18 | ns |
| $t_{WC}$ | Write Cycle Time | 20 | | 25 | | 30 | | 35 | | ns |
| $t_{PW}$ | Write Pulse Width | 10 | | 15 | | 20 | | 25 | | ns |
| $t_{HWZ}$[5,8] | Write HIGH to Low Z | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{WR}$ | Write Recovery Time | 10 | | 10 | | 10 | | 10 | | ns |
| $t_{SD}$ | Data Set-Up Time | 6 | | 8 | | 12 | | 15 | | ns |
| $t_{HD}$ | Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{MRSC}$ | $\overline{MR}$ Cycle Time | 20 | | 25 | | 30 | | 35 | | ns |
| $t_{PMR}$ | $\overline{MR}$ Pulse Width | 10 | | 15 | | 20 | | 25 | | ns |
| $t_{RMR}$ | $\overline{MR}$ Recovery Time | 10 | | 10 | | 10 | | 10 | | ns |
| $t_{RPW}$ | Read HIGH to $\overline{MR}$ HIGH | 10 | | 15 | | 20 | | 25 | | ns |
| $t_{WPW}$ | Write HIGH to $\overline{MR}$ HIGH | 10 | | 15 | | 20 | | 25 | | ns |
| $t_{RTC}$ | Retransmit Cycle Time | 20 | | 25 | | 30 | | 35 | | ns |
| $t_{PRT}$ | Retransmit Pulse Width | 10 | | 15 | | 20 | | 25 | | ns |
| $t_{RTR}$ | Retransmit Recovery Time | 10 | | 10 | | 10 | | 10 | | ns |

**Notes:**

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V and output loading of the specified $I_{OL}/I_{OH}$ and 30 pF load capacitance, as in part (a) of AC Test Load and Waveforms. unless otherwise specified.
7. See the last page of this specification for Group A subgroup testing information.
8. $t_{HZR}$ transition is measured at +200 mV from $V_{OL}$ and −200 mV from $V_{OH}$. $t_{DVR}$ transition is measured at the 1.5V level. $t_{HWZ}$ and $t_{LZR}$ transition is measurec at ±100 mV from the steady state.
9. $t_{HZR}$ and $t_{DVR}$ use capacitance loading as in part (b) of AC Test Load and Waveforms.

**Switching Characteristics** Over the Operating Range[6, 7] (continued)

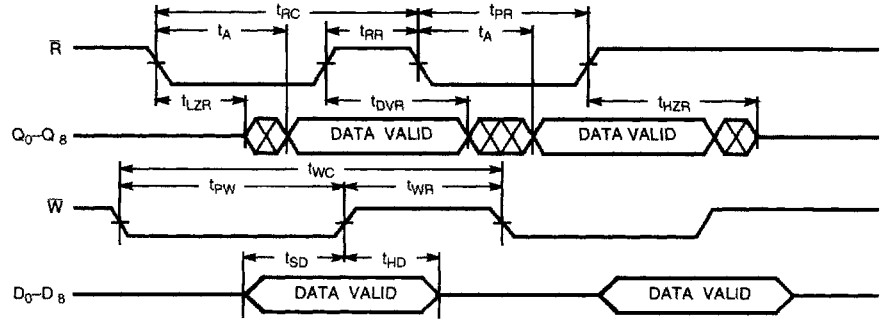
| Parameter | Description | 7C419–10<br>7C421–10<br>7C425–10<br>7C429–10<br>7C433–10 | | 7C419–15<br>7C421–15<br>7C425–15<br>7C429–15<br>7C433–15 | | 7C420–20<br>7C421–20<br>7C424–20<br>7C425–20<br>7C428–20<br>7C429–20<br>7C433–20 | | 7C420–25<br>7C421–25<br>7C424–25<br>7C425–25<br>7C429–25<br>7C432–25<br>7C433–25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{EFL}$ | $\overline{MR}$ to $\overline{EF}$ LOW | | 20 | | 25 | | 30 | | 35 | ns |
| $t_{HFH}$ | $\overline{MR}$ to $\overline{HF}$ HIGH | | 20 | | 25 | | 30 | | 35 | ns |
| $t_{FFH}$ | $\overline{MR}$ to $\overline{FF}$ HIGH | | 20 | | 25 | | 30 | | 35 | ns |
| $t_{REF}$ | Read LOW to $\overline{EF}$ LOW | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{RFF}$ | Read HIGH to $\overline{FF}$ HIGH | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{WEF}$ | Write HIGH to $\overline{EF}$ HIGH | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{WFF}$ | Write LOW to $\overline{FF}$ LOW | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{WHF}$ | Write LOW to $\overline{HF}$ LOW | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{RHF}$ | Read HIGH to $\overline{HF}$ HIGH | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{RAE}$ | Effective Read from Write HIGH | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{RPE}$ | Effective Read Pulse Width After $\overline{EF}$ HIGH | 10 | | 15 | | 20 | | 25 | | ns |
| $t_{WAF}$ | Effective Write from Read HIGH | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{WPF}$ | Effective Write Pulse Width After $\overline{FF}$ HIGH | 10 | | 15 | | 20 | | 25 | | ns |
| $t_{XOL}$ | Expansion Out LOW Delay from Clock | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{XOH}$ | Expansion Out HIGH Delay from Clock | | 10 | | 15 | | 20 | | 25 | ns |

**Switching Characteristics** Over the Operating Range[6, 7] (continued)

| Parameter | Description | 7C419–30 7C421–30 7C424–30 7C425–30 7C429–30 7C433–30 | | 7C419–40 7C420–40 7C421–40 7C424–40 7C425–40 7C429–40 7C432–40 7C433–40 | | 7C420–65 7C421–65 7C424–65 7C425–65 7C428–65 7C429–65 7C433–65 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 40 | | 50 | | 80 | | ns |
| $t_A$ | Access Time | | 30 | | 40 | | 65 | ns |
| $t_{RR}$ | Read Recovery Time | 10 | | 10 | | 15 | | ns |
| $t_{PR}$ | Read Pulse Width | 30 | | 40 | | 65 | | ns |
| $t_{LZR}$[5,8] | Read LOW to Low Z | 3 | | 3 | | 3 | | ns |
| $t_{DVR}$[8,9] | Data Valid After Read HIGH | 5 | | 5 | | 5 | | ns |
| $t_{HZR}$[5,8,9] | Read HIGH to High Z | | 20 | | 20 | | 20 | ns |
| $t_{WC}$ | Write Cycle Time | 40 | | 50 | | 80 | | ns |
| $t_{PW}$ | Write Pulse Width | 30 | | 40 | | 65 | | ns |
| $t_{HWZ}$[5,8] | Write HIGH to Low Z | 5 | | 5 | | 5 | | ns |
| $t_{WR}$ | Write Recovery Time | 10 | | 10 | | 15 | | ns |
| $t_{SD}$ | Data Set-Up Time | 18 | | 20 | | 30 | | ns |
| $t_{HD}$ | Data Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{MRSC}$ | $\overline{MR}$ Cycle Time | 40 | | 50 | | 80 | | ns |
| $t_{PMR}$ | $\overline{MR}$ Pulse Width | 30 | | 40 | | 65 | | ns |
| $t_{RMR}$ | $\overline{MR}$ Recovery Time | 10 | | 10 | | 15 | | ns |
| $t_{RPW}$ | Read HIGH to $\overline{MR}$ HIGH | 30 | | 40 | | 65 | | ns |
| $t_{WPW}$ | Write HIGH to $\overline{MR}$ HIGH | 30 | | 40 | | 65 | | ns |
| $t_{RTC}$ | Retransmit Cycle Time | 40 | | 50 | | 80 | | ns |
| $t_{PRT}$ | Retransmit Pulse Width | 30 | | 40 | | 65 | | ns |
| $t_{RTR}$ | Retransmit Recovery Time | 10 | | 10 | | 15 | | ns |
| $t_{EFL}$ | $\overline{MR}$ to $\overline{EF}$ LOW | | 40 | | 50 | | 80 | ns |
| $t_{HFH}$ | $\overline{MR}$ to $\overline{HF}$ HIGH | | 40 | | 50 | | 80 | ns |
| $t_{FFH}$ | $\overline{MR}$ to $\overline{FF}$ HIGH | | 40 | | 50 | | 80 | ns |
| $t_{REF}$ | Read LOW to $\overline{EF}$ LOW | | 30 | | 35 | | 60 | ns |
| $t_{RFF}$ | Read HIGH to $\overline{FF}$ HIGH | | 30 | | 35 | | 60 | ns |
| $t_{WEF}$ | Write HIGH to $\overline{EF}$ HIGH | | 30 | | 35 | | 60 | ns |
| $t_{WFF}$ | Write LOW to $\overline{FF}$ LOW | | 30 | | 35 | | 60 | ns |
| $t_{WHF}$ | Write LOW to $\overline{HF}$ LOW | | 30 | | 35 | | 60 | ns |
| $t_{RHF}$ | Read HIGH to $\overline{HF}$ HIGH | | 30 | | 35 | | 60 | ns |
| $t_{RAE}$ | Effective Read from Write HIGH | | 30 | | 35 | | 60 | ns |
| $t_{RPE}$ | Effective Read Pulse Width After $\overline{EF}$ HIGH | 30 | | 40 | | 65 | | ns |
| $t_{WAF}$ | Effective Write from Read HIGH | | 30 | | 35 | | 60 | ns |
| $t_{WPF}$ | Effective Write Pulse Width After $\overline{FF}$ HIGH | 30 | | 40 | | 65 | | ns |
| $t_{XOL}$ | Expansion Out LOW Delay from Clock | | 30 | | 40 | | 65 | ns |
| $t_{XOH}$ | Expansion Out HIGH Delay from Clock | | 30 | | 40 | | 65 | ns |

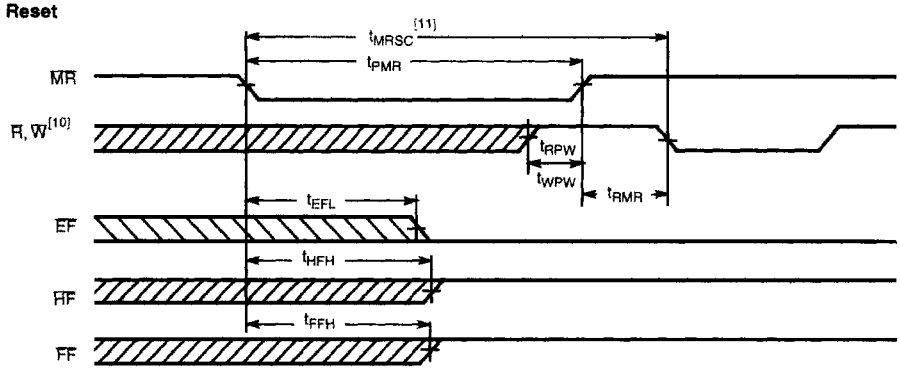
## Switching Waveforms

### Asynchronous Read and Write



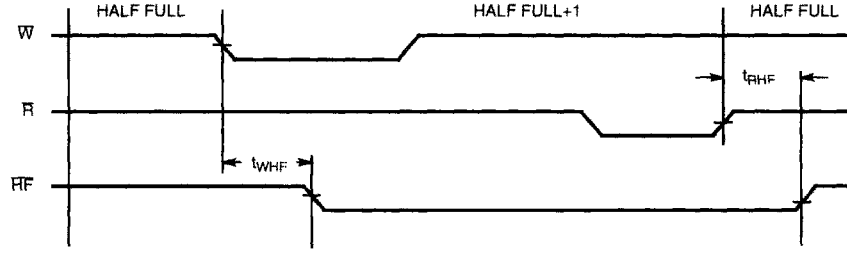

C420-9

### Master Reset




C420-10

### Half-Full Flag

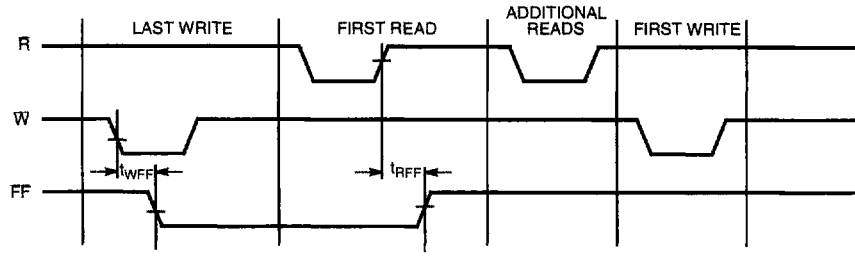



C420-11

**Notes:**
10. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$.
11. $t_{MRSC} = t_{PMR} + t_{RMR}$.

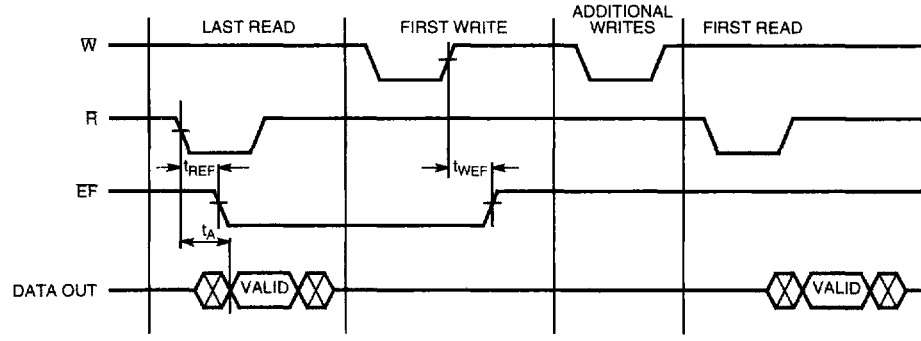
## Switching Waveforms (continued)

### Last Write to First Read Full Flag



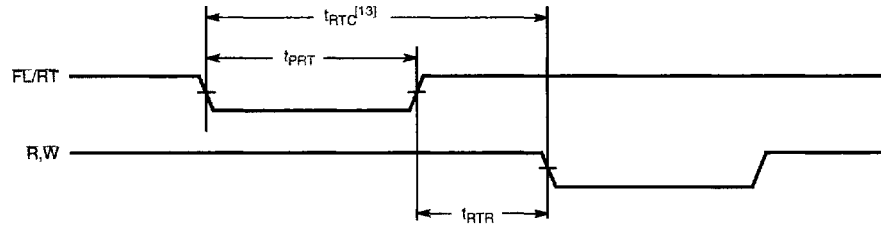

C420-12

### Last Read to First Write Empty Flag




C420-13

### Retransmit[12]

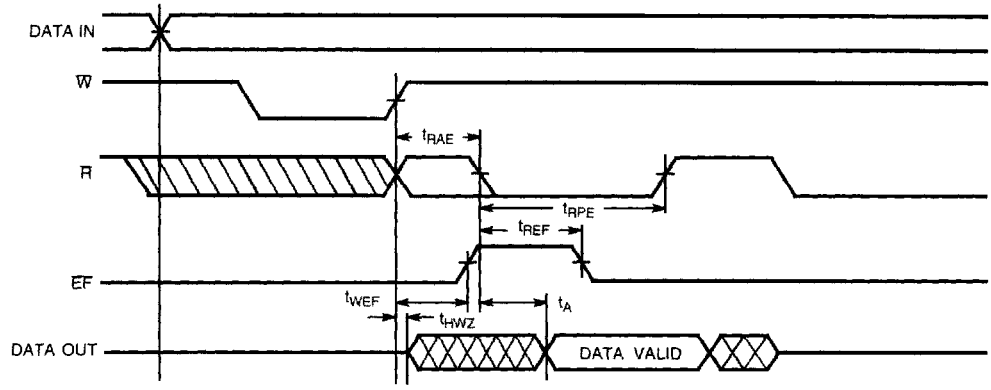



C420-14

**Notes:**
12. EF, HF and FF may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at $t_{RTC}$.
13. $t_{RTC} = t_{PRT} + t_{RTR}$.

## Switching Waveforms (continued)

### Empty Flag and Read Data Flow-Through Mode

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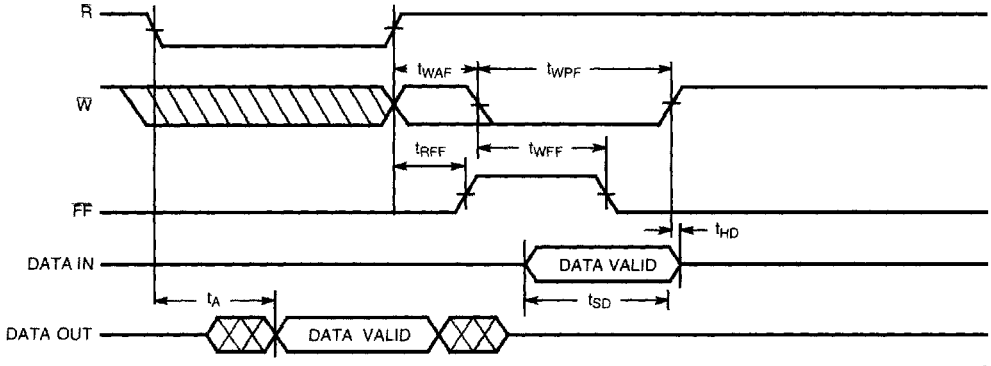
### Full Flag and Write Data Flow-Through Mode

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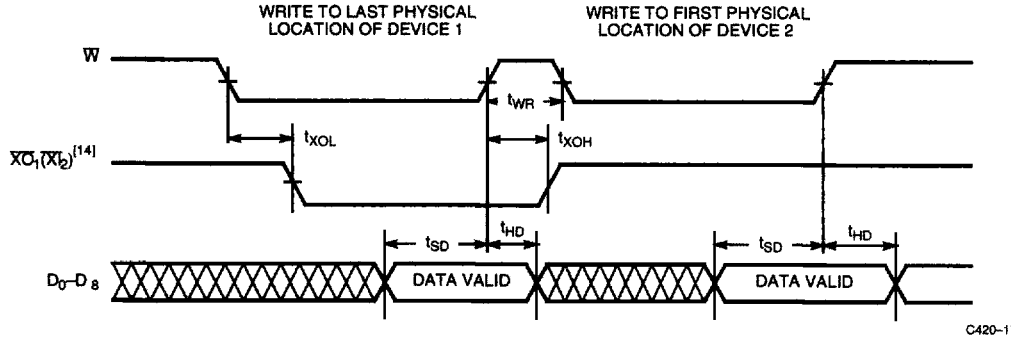
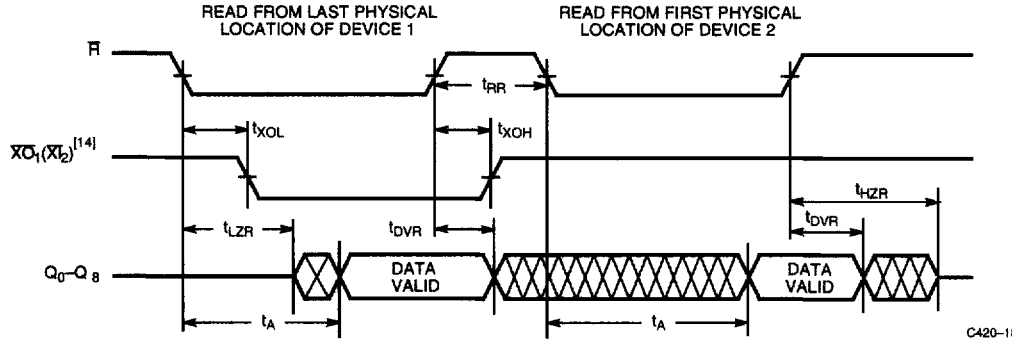
## Switching Waveforms (continued)

### Expansion Timing Diagrams




**Note:**
14. Expansion Out of device 1 ($\overline{XO}_1$) is connected to Expansion In of device 2 ($\overline{XI}_2$).

## Architecture

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, CY7C432/3 FIFOs consist of an array of 256, 512, 1024, 2048, 4096 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

### Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data propagation through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

### Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH $t_{RPW}$/$t_{WPW}$ before and $t_{RMR}$ after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

**Writing Data to the FIFO**

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs ($D_0$–$D_8$) $t_{SD}$ before and $t_{HD}$ after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs $t_{WEF}$ after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW $t_{WHF}$ after the falling edge of $\overline{W}$ following the FIFO actually being Half Full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs $t_{RHF}$ after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW $t_{WFF}$ after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH tRFF after a read from a full FIFO.

**Reading Data from the FIFO**

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs ($Q_0$–$Q_8$) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. The rising edge of $\overline{R}$ causes the data outputs to go to the high-impedance state and remain such until a write is performed. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read $t_{WEF}$ after a valid write.

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and $t_{RTR}$ after retransmit is LOW. With every read cycle after retransmit, previously accessed data as well as not previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

Up to the full depth of the FIFO can be repeatedly retransmitted.

**Standalone/Width Expansion Modes**

Standalone and width expansion modes are set by grounding Expansion In ($\overline{XI}$) and tying First Load ($\overline{FL}$) to $V_{CC}$. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

**Depth Expansion Mode** (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

**Use of the Empty and Full Flags**

In order to achieve the maximum frequency, the flags must be valid at the beginning of the next cycle. However, because they can be updated by either edge of the read of write signal, they must be valid by one-half of a cycle. Cypress FIFOs meet this requirement; some competitors' FIFOs do not.

The reason why the flags are required to be valid by the next cycle is fairly complex. It has to do with the "effective pulse width violation" phenomenon, which can occur at the full and empty boundary conditions, if the flags are not properly used. The empty flag must be used to prevent reading from an empty FIFO and the full flag must be used to prevent writing into a full FIFO.

For example, consider an empty FIFO that is receiving read pulses. Because the FIFO is empty, the read pulses are ignored by the FIFO, and nothing happens. Next, a single word is written into the FIFO, with a signal that is asynchronous to the read signal. The (internal) state machine in the FIFO goes from empty to empty+1. However, it does this asynchronously with respect to the read signal, so that it cannot be determined what the effective pulse width of the read signal is, because the state machine does not look at the read signal until it goes to the empty+1 state. In a similar manner, the minimum write pulse width may be violated by attempting to write into a full FIFO, and asynchronously performing a read. The empty and full flags are used to avoid these effective pulse width violations, but in order to do this and operate at the maximum frequency, the flag must be valid at the beginning of the next cycle.

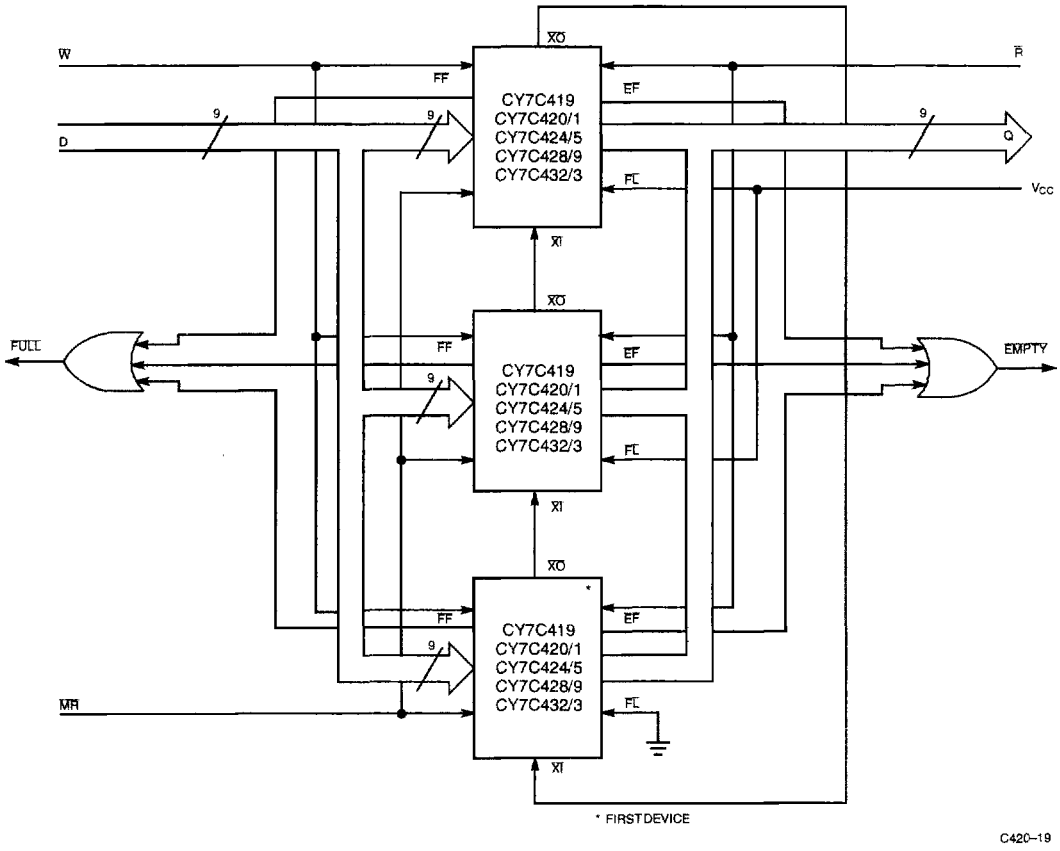



**Figure 1. Depth Expansion**

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 10 | CY7C419–10AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C419–10JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C419–10PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C419–10VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| 15 | CY7C419–15AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C419–15JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C419–15VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C419–15JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| 30 | CY7C419–30JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| 40 | CY7C419–40AC | A32 | 32-Pin Thin Plastic Quad Flatpack | |
| | CY7C419–40JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 25 | CY7C420–25PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |
| 40 | CY7C420–40PC | P15 | 28-Lead (600-Mil) Molded DIP | |
| 65 | CY7C420–65PC | P15 | 28-Lead (600-Mil) Molded DIP | |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 10 | CY7C421–10AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C421–10JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C421–10PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C421–10VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| 15 | CY7C421–15AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C421–15JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C421–15JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C421–15VI | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C421–15DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C421–15LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 20 | CY7C421–20JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C421–20PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C421–20VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C421–20JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| 25 | CY7C421–25JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C421–25PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C421–25VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C421–25JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C421–25PI | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C421–25DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| 30 | CY7C421–30JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C421–30PC | P21 | 28-Lead (300-Mil) Molded DIP | |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 30 | CY7C421–30JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C421–30DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C421–30LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 40 | CY7C421–40JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C421–40PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C421–40VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C421–40JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| 65 | CY7C421–65JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C421–65PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C421–65VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C421–65JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C421–65DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 40 | CY7C424–40PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |
| 65 | CY7C424–65PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 10 | CY7C425–10AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C425–10JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C425–10PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C425–10VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| 15 | CY7C425–15JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C425–15PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C425–15DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C425–15LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 20 | CY7C425–20JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C425–20PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C425–20VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| 25 | CY7C425–25JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C425–25PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C425–25JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C425–25VI | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C425–25DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C425–25LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 30 | CY7C425–30JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C425–30PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C425–30VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C425–30VI | V21 | 28-Lead (300-Mil) Molded SOJ | Industrial |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 40 | CY7C425–40JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C425–40PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C425–40VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C425–40JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| 65 | CY7C425–65JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C425–65PC | P21 | 28-Lead (300-Mil) Molded DIP | |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 20 | CY7C428–20PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |
| 25 | CY7C428–25DMB | D16 | 28-Lead (600-Mil) CerDIP | Military |
| 65 | CY7C428–65PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |

2

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 10 | CY7C429–10AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C429–10JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C429–10PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| 15 | CY7C429–15JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C429–15JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C429–15DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C429–15LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 20 | CY7C429–20JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C429–20PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C429–20VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C429–20DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| 25 | CY7C429–25JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C429–25PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C429–25VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C429–25JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C429–25DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C429–25LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 30 | CY7C429–30JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C429–30PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C429–30VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C429–30DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| 40 | CY7C429–40AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C429–40JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C429–40PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| 65 | CY7C429–65JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C429–65PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C429–65JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 25 | CY7C432–25PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |
| 40 | CY7C432–40PC | P15 | 28-Lead (600-Mil) Molded DIP | Commercial |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 10 | CY7C433–10AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C433–10JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C433–10PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C433–10VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| 15 | CY7C433–15AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C433–15JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C433–15JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C433–15PI | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C433–15DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C433–15LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 20 | CY7C433–20AC | A32 | 32-Pin Thin Plastic Quad Flatpack | Commercial |
| | CY7C433–20JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C433–20PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| 25 | CY7C433–25JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C433–25PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C433–25VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C433–25JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| 30 | CY7C433–30JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C433–30PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C433–30JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C433–30PI | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C433–30DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C433–30LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 40 | CY7C433–40JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C433–40PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C433–40VC | V21 | 28-Lead (300-Mil) Molded SOJ | |
| | CY7C433–40JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| 65 | CY7C433–65JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C433–65PC | P21 | 28-Lead (300-Mil) Molded DIP | |

## MILITARY SPECIFICATIONS
## Group A Subgroup Testing

### DC Characteristics

| Parameters | Subgroups |
|---|---|
| $V_{OH}$ | 1, 2, 3 |
| $V_{OL}$ | 1, 2, 3 |
| $V_{IH}$ | 1, 2, 3 |
| $V_{IL}$ Max. | 1, 2, 3 |
| $I_{IX}$ | 1, 2, 3 |
| $I_{CC}$ | 1, 2, 3 |
| $I_{CC1}$ | 1, 2, 3 |
| $I_{SB1}$ | 1, 2, 3 |
| $I_{SB2}$ | 1, 2, 3 |
| $I_{OS}$ | 1, 2, 3 |

### Switching Characteristics

| Parameters | Subgroups |
|---|---|
| $t_{RC}$ | 9, 10, 11 |
| $t_{A}$ | 9, 10, 11 |
| $t_{RR}$ | 9, 10, 11 |
| $t_{PR}$ | 9, 10, 11 |
| $t_{DVR}$ | 9, 10, 11 |
| $t_{WC}$ | 9, 10, 11 |
| $t_{PW}$ | 9, 10, 11 |
| $t_{WR}$ | 9, 10, 11 |
| $t_{SD}$ | 9, 10, 11 |
| $t_{HD}$ | 9, 10, 11 |
| $t_{MRSC}$ | 9, 10, 11 |
| $t_{PMR}$ | 9, 10, 11 |
| $t_{RMR}$ | 9, 10, 11 |
| $t_{RPW}$ | 9, 10, 11 |
| $t_{WPW}$ | 9, 10, 11 |
| $t_{RTC}$ | 9, 10, 11 |
| $t_{PRT}$ | 9, 10, 11 |
| $t_{RTR}$ | 9, 10, 11 |
| $t_{EFL}$ | 9, 10, 11 |
| $t_{HFH}$ | 9, 10, 11 |
| $t_{FFH}$ | 9, 10, 11 |
| $t_{REF}$ | 9, 10, 11 |
| $t_{RFF}$ | 9, 10, 11 |
| $t_{WEF}$ | 9, 10, 11 |
| $t_{WFF}$ | 9, 10, 11 |
| $t_{WHF}$ | 9, 10, 11 |
| $t_{RHF}$ | 9, 10, 11 |
| $t_{RAE}$ | 9, 10, 11 |
| $t_{RPE}$ | 9, 10, 11 |
| $t_{WAF}$ | 9, 10, 11 |
| $t_{WPF}$ | 9, 10, 11 |
| $t_{XOL}$ | 9, 10, 11 |
| $t_{XOH}$ | 9, 10, 11 |

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