National Semiconductor

September 1998

54ACTQ16646
16-Bit Transceiver/Register with TRI-STATE® Outputs

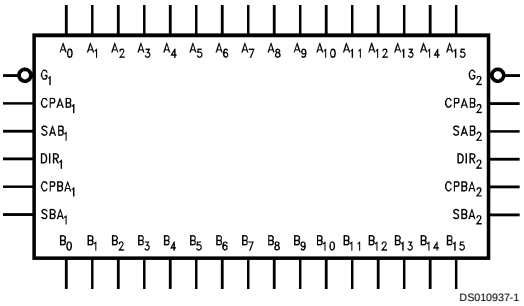
General Description

The 'ACTQ16646 contains sixteen non-inverting bidirectional registered bus transceivers providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition. The 'ACTQ16646 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series® features GTO® output control and undershoot corrector for superior performance.

Features

- Utilizes NSC FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- Separate control logic for each byte
- 16-bit version of the 'ACTQ646
- Outputs source/sink 24 mA
- Standard Microcircuit Drawing (SMD) 5962-9581601

Logic Symbol



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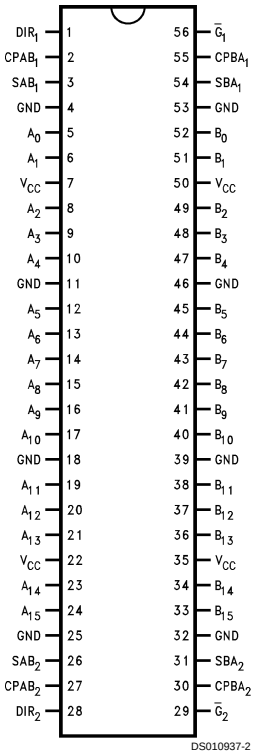
Connection Diagram

Pin Assignment for CERPAK



Real Time Transfer A-Bus to B-Bus

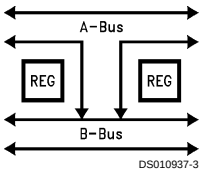


FIGURE 1.

Real Time Transfer B-Bus to A-Bus

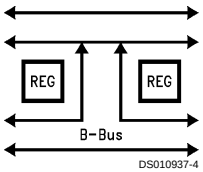


FIGURE 2.

Storage from Bus to Register

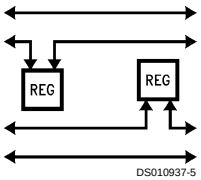


FIGURE 3.

Transfer from Register to Bus

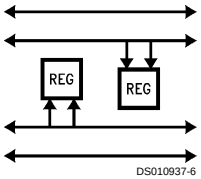


FIGURE 4.

Function Table

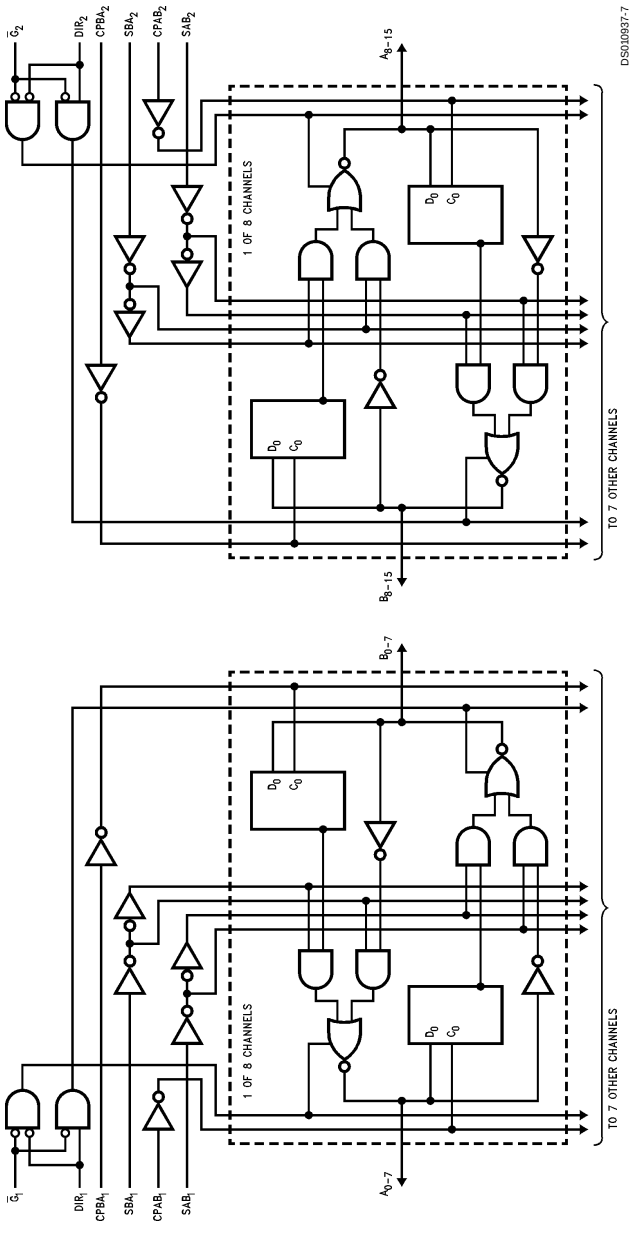
Inputs						Data I/O (Note 1)		Output Operation Mode
G_1	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X			Isolation
H	X	N	X	X	X	Input	Input	Clock An Data into A Register
H	X	X	N	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X			An to Bn — Real Time (Transparent Mode)
L	H	N	X	L	X	Input	Output	Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	N	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L			Bn to An — Real Time (Transparent Mode)
L	L	X	N	X	L	Output	Input	Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	N	X	H			Clock Bn into B Register and Output to An

H = HIGH Voltage Level X = Immaterial

L = LOW Voltage Level N = LOW-to-HIGH Transition.

Note 1: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

Logic Diagram



Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
Junction Temperature	
CDIP	+175˚C
Storage Temperature	−65˚C to +150˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A):	
54ACTQ	−55˚C to +125˚C
Minimum Input Edge Rate (dV/dt)	
'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Output Voltage	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
					V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
					V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{OZT}	Maximum I/O Leakage Current	5.5	±10.0	µA	V_{IN} = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V
I_{CC}	Max Quiescent Supply Current	5.5	160.0	µA	V_{IN} = V_{CC} or GND
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 4)		50	mA	V_{OHD} = 3.85V Min
V_{OLP}	Quick Output Maximum Dynamic V_{OL}	5.0	1.1	V	(Notes 5, 6)
V_{OLV}	Quick Output Minimum Dynamic V_{OL}	5.0	-0.8	V	(Notes 5, 6)

Note 3: All outputs loaded; thresholds associated with output under test.

Note 4: Maximum test duration 2.0 ms; one output loaded at a time.

Note 5: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Note 6: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 7)	54ACTQ $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units
			Min	Max	
t_{PHL}	Propagation Delay	5.0	2.9	10.2	ns
t_{PLH}	Clock to Bus		3.2	10.2	
t_{PHL}	Propagation Delay	5.0	3.6	11.5	ns
t_{PLH}	Bus to Bus		3.3	10.8	
t_{PHL}	Propagation Delay	5.0	3.1	11.3	ns
t_{PLH}	Select to Bus (w/An or Bn HIGH or LOW)		3.2	11.5	
t_{PZL}	Enable Time	5.0	3.8	12.9	ns
t_{PZH}	G to An/Bn		3.3	11.9	
t_{PLZ}	Disable Time	5.0	2.3	9.8	ns
t_{PHZ}	G to An/Bn		2.6	9.5	
t_{PZL}	Enable Time	5.0	4.3	14.0	ns
t_{PZH}	DIR to An/Bn		3.7	12.8	
t_{PLZ}	Disable Time	5.0	2.0	10.8	ns
t_{PHZ}	DIR to An/Bn		2.5	11.0	

Note 7: Voltage Range 5.0 is 5.0V ±0.5V.

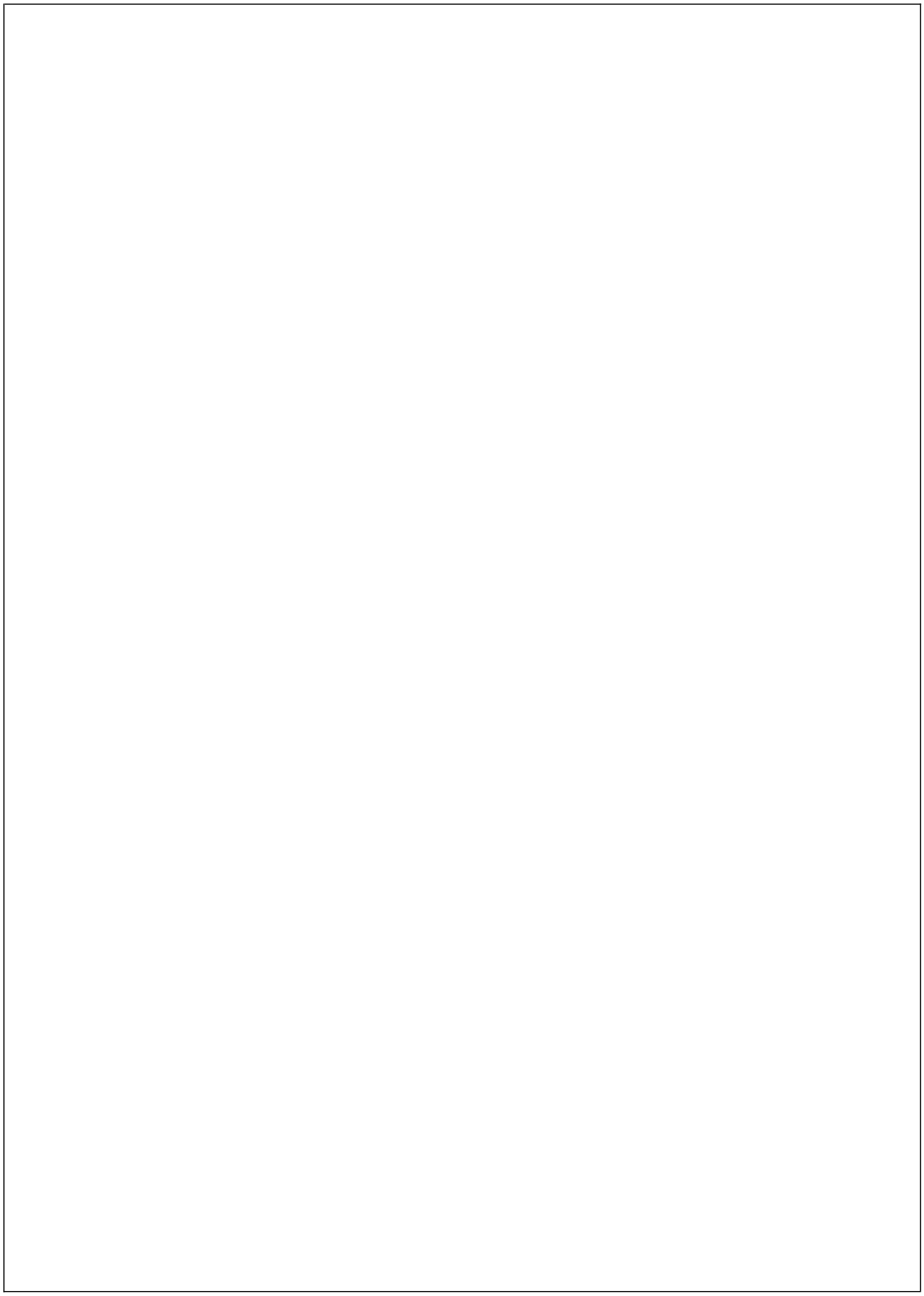
AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 8)	54ACTQ $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units
			Guaranteed Minimum	
t_S	Setup Time, H or L Bus to Clock	5.0	3.0	ns
t_H	Hold Time, H or L Bus to Clock	5.0	1.5	ns
t_W	Clock Pulse Width H or L	5.0	4.0	ns

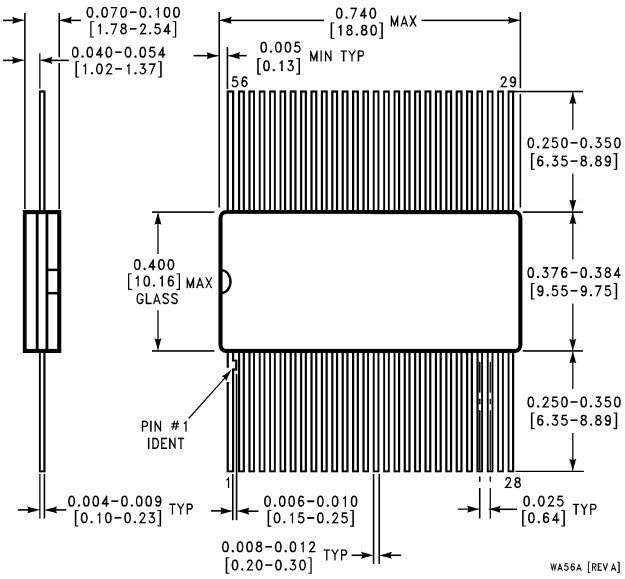
Note 8: Voltage Range 5.0 is 5.0V ±0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	95	pF	V_{CC} = 5.0V



Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead CERPAK
NS Package Number WA56A

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