

DESCRIPTION

The HY5118160 is the new generation and fast dynamic RAM organized 1,048,576 × 16-bit. The HY5118160 utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5118160 to be packaged in standard 42/42 pin plastic SOJ, 44/50 pin TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V±10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
- Max. battery back-up 3.3mW (SL-part)
Max. CMOS standby 2.2mW (SL-part)
5.5mW
- Max. TTL standby 11.0mW
- Max. operating

Speed	Power
70	880mW
80	770mW
100	660mW

- Single power supply of 5V±10%
- TTL compatible inputs and outputs
- Fast access Time

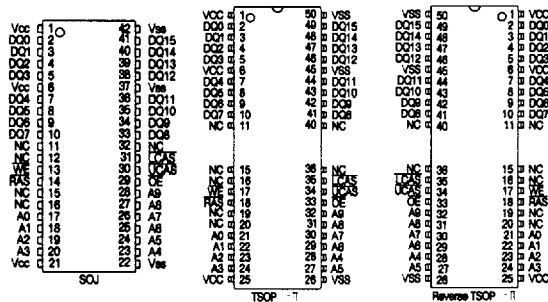
Speed	t _{RAC}	t _{CAC}	t _{PC}
70	70ns	20ns	45ns
80	80ns	20ns	50ns
100	100ns	25ns	60ns

- Fast page mode operation
- 2CAS inputs for upper and lower byte control
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self refresh capability
- 1024 refresh cycles /256ms (SL-part)
1024 refresh cycles /16ms

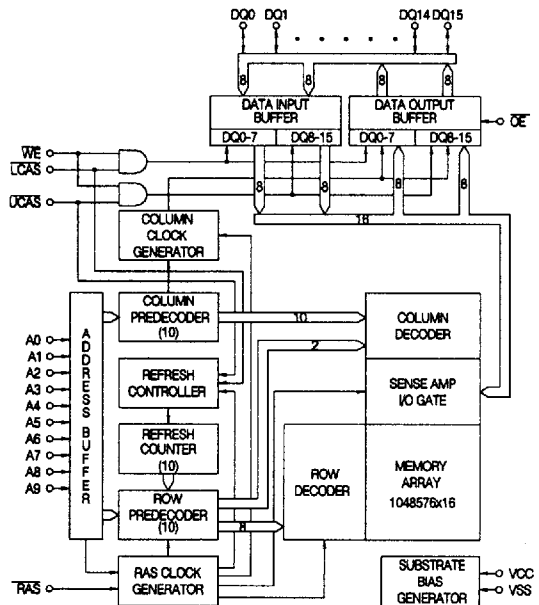
PIN DESCRIPTION

RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0 - A9	Address Input
DQ0 - DQ15	Data Input/Output
Vcc	Power (+5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	1.1	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE: All Voltage are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	V _{SS} ≤ V _{IN} ≤ V _{CC} +1.0, All other pins not under test = V _{SS}		-10	10	μA	
ILO	Output Leakage Current (High impedance State)	V _{SS} ≤ V _{OUT} ≤ V _{CC} RAS & CAS at V _{IH}		-10	10	μA	
ICC1	V _{CC} Supply Current, Operating	trc = trc (min.)	70 80 100	- - -	160 140 120	mA	1,2,3
ICC2	V _{CC} Supply Current, TTL Standby	RAS & CAS at V _{IH} , other inputs ≥ V _{SS}		-	2	mA	
ICC3	V _{CC} Supply Current, RAS-only refresh	trc = trc (min.)	70 80 100	- - -	160 140 120	mA	1,3
ICC4	V _{CC} Supply Current, Fast Page mode	tpc = tpc (min.)	70 80 100	- - -	120 110 100	mA	1,2,3
ICC5	V _{CC} Supply Current, CMOS Standby	RAS & CAS ≥ V _{CC} -0.2V	SL-part	-	1 0.4	mA	5
ICC6	V _{CC} Supply Current, CAS-before- RAS refresh	trc = trc (min.)	70 80 100	- - -	160 140 120	mA	1,3
ICC7	V _{CC} Supply Current, Battery Back Up (SL-part Only)	trc = 250μs, CAS = CBR cycling or 0.2V, WE=V _{CC} -0.2V, A0-A11 = V _{CC} -0.2V or 0.2V, D=V _{CC} -0.2V, 0.2V or open, Q=open	t _{RAS} ≤ 300ns t _{RAS} ≤ 1μs	-	450 600	μA	1, 4, 5
ICC8	V _{CC} Supply Current, Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V, other pins same as Icc7		-	500	μA	5
VOL	Output Low Voltage	IOL=4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH=-5mA		2.4	-	V	

NOTE :

1. Icc1, Icc3, Icc4, Icc6 and Icc7 depend on cycle rate.
2. Icc1 and Icc4 depend on output loading. Specified values are obtained with the output open.
3. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS =V_{IL}. Icc4, Address can be changed maximum once while CAS=V_{IH}.
4. t_{RAS}(max.) =1μs is only applied to refresh of battery backup but t_{RAS}(max.) =10μs is applied to normal functional operation.
5. Icc5(max.) =0.4mA, Icc7 and Icc8 are applied to SL-part only (HY5118160SLJC, HY5118160SLTC and HY5118160SLRC).

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HY5118160JC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-70		-80		-100			
			MIN	MAX	MIN	MAX	MIN	MAX		
1	tRC	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
3	tPC	Fast Page Mode Cycle Time	45	-	50	-	60	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	125	-	ns	
5	tRAC	Access Time from RAS	-	70	-	80	-	100	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	-	50	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	40	-	45	-	55	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	50	-	60	-	70	-	ns	
13	tRAS	RAS Pulse Width	70	10K	80	10K	100	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	70	100K	80	100K	100	100K	ns	
15	tRSH	RAS Hold Time	20	-	20	-	25	-	ns	
16	tCSH	CAS Hold Time	70	-	80	-	100	-	ns	
17	tCAS	CAS Pulse width	20	10K	20	10K	25	10K	ns	
18	tRCD	RAS to CAS Delay	20	50	20	60	25	75	ns	9
19	tRAD	RAS to Column Address Delay Time	15	35	15	40	20	50	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	10	-	ns	15
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	17
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold time	10	-	10	-	15	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	14
25	tCAH	Column Address Hold Time	15	-	15	-	20	-	ns	14
26	tAR	Column Address Hold Time from RAS	55	-	60	-	75	-	ns	
27	tRAL	Column Address to RAS Lead Time	35	-	40	-	50	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	14
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	20	-	ns	14
32	tWCR	Write Command Hold Time from RAS	55	-	60	-	75	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	20	-	ns	
34	tRWL	Write Command to RAS Lead Time	20	-	20	-	25	-	ns	
35	tCWL	Write Command to CAS Lead Time	20	-	20	-	25	-	ns	16
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	20	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	55	-	60	-	75	-	ns	
39	tREF	Refresh Period(1024cycle)	-	16	-	16	-	16	ms	12
		SL-part	-	256	-	256	-	256	ms	11
40	tWCS	Write Command Set up Time	0	-	0	-	0	-	ns	8,14

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY5118160JC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-70		-80		-100			
			MIN	MAX	MIN	MAX	MIN	MAX		
41	tCWD	CAS to WE Delay Time	50	-	50	-	60	-	ns	8
42	tRWD	RAS to WE Delay Time	100	-	110	-	135	-	ns	8
43	tAWD	Column Address to WE Delay Time	65	-	70	-	85	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	14
45	tCHR	CAS Hold Time (CBR Cycle)	15	-	15	-	20	-	ns	15
46	tRPC	RAS to CAS Precharge Time	10	-	10	-	10	-	ns	14
47	tCPT	CAS Precharge Time (CBR Counter Test)	40	-	40	-	50	-	ns	17
48	tROH	RAS Hold Time Reference to OE	20	-	20	-	20	-	ns	
49	tOEA	OE Access Time	-	20	-	20	-	25	ns	
50	tOED	OE to Data Delay	20	-	20	-	25	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time	0	15	0	15	0	15	ns	5
52	tOEH	OE Command Hold Time	20	-	20	-	25	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	70	-	75	-	90	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	45	-	45	-	55	-	ns	
55	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	µs	
56	tRPS	RAS Precharge Time (Self Refresh Cycle)	130	-	150	-	180	-	ns	
57	tCHS	CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	

NOTE:

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ -only refresh cycles are required.
2. If $\overline{\text{RAS}}=\text{Vss}$ during power-up, HY5118160 could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with Vcc during power-up or be held at valid VIH in order to minimize the power-up current.
3. $\text{VIH}(\text{min.})$ and $\text{VIL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition times are measured between $\text{VIH}(\text{min.})$ and $\text{VIL}(\text{max.})$, and are assumed to be 5ns for all inputs.
4. Measured at $\text{VOH}=2.4\text{V}$ and $\text{VOL}=0.4\text{V}$ with a load equivalent to 2 TTL loads and 100pF.
5. $\text{tOFF}(\text{max.})$ and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either trCH or trRH must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ leading edge in early write cycles and $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
8. twCS , trWD , tcWD , tAWD and tcpWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $\text{twCS}\geq\text{twCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $\text{trWD}\geq\text{trWD}(\text{min.})$, $\text{tcWD}\geq\text{tcWD}(\text{min.})$, $\text{tAWD}\geq\text{tAWD}(\text{min.})$, and $\text{tcpWD}\geq\text{tcpWD}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indetermined.
9. Operation within the $\text{trCD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met. $\text{trCD}(\text{max.})$ is specified as a reference point only. If trCD is greater than the specified $\text{trCD}(\text{max.})$ limit, then access time is controlled by tcAC .
10. Operation within the $\text{trAD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met. $\text{trAD}(\text{max.})$ is specified as a reference point only. If trAD is greater than the specified $\text{trAD}(\text{max.})$ limit, then access time is controlled by tAA .
11. $\text{tREF}(\text{max.})=256\text{ms}$ is applied to SL-parts only (HY5118160SLJC, HY5118160SLTC and HY5118160SLRC).
12. A burst of 1024 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles must be executed within 16ms (256ms for SL-part) after exiting self refresh.
13. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ must be transitioned simultaneously within a same read or write cycle.
14. These parameters are determined by the earlier falling edge of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$.
15. These parameters are determined by the later rising edge of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$.
16. tcWL must be satisfied by both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ for 16-bits access cycles.
17. tcp and tcPT are measured when both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ are high state.

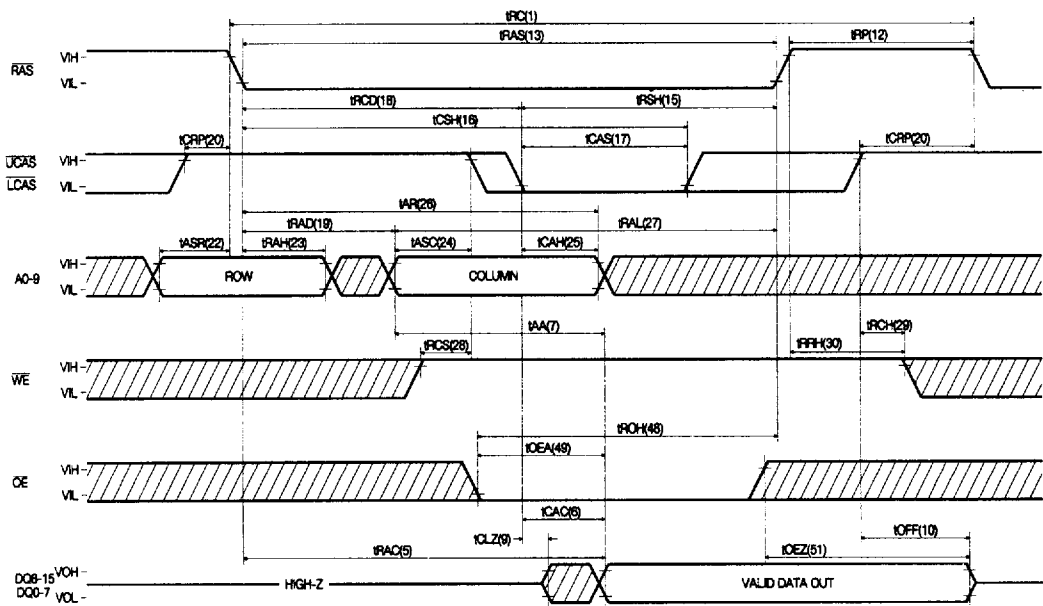
CAPACITANCE

($\text{TA}=25^\circ\text{C}$, $\text{Vcc}=5\text{V}\pm 10\%$, $\text{Vss}=0\text{V}$, $f=1\text{MHz}$, unless otherwise noted.)

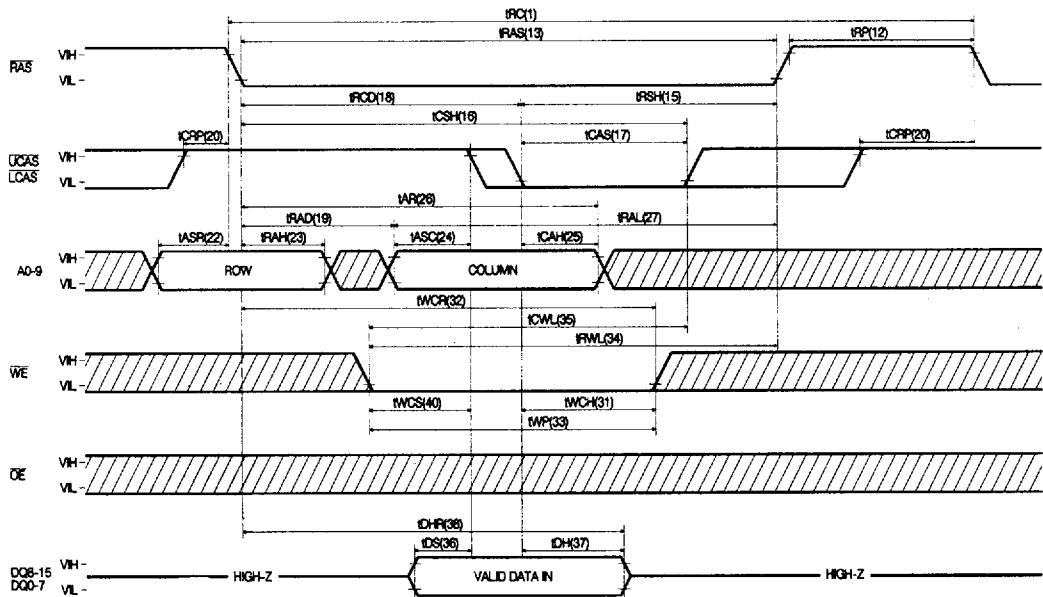
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A11)	-	5	pF
CIN2	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ15)	-	7	pF

TIMING DIAGRAM

READ CYCLE

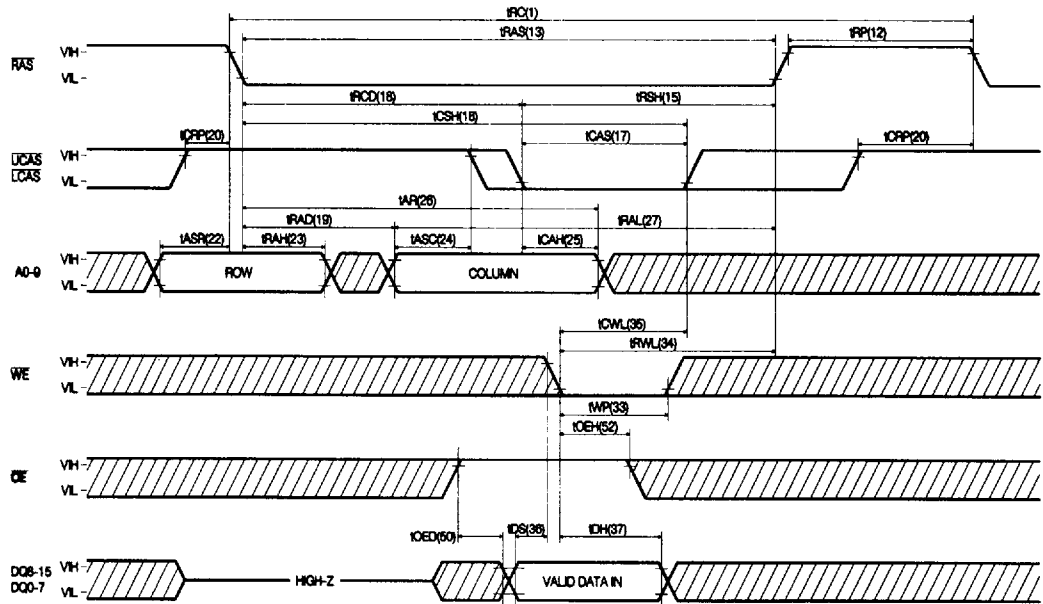


EARLY WRITE CYCLE

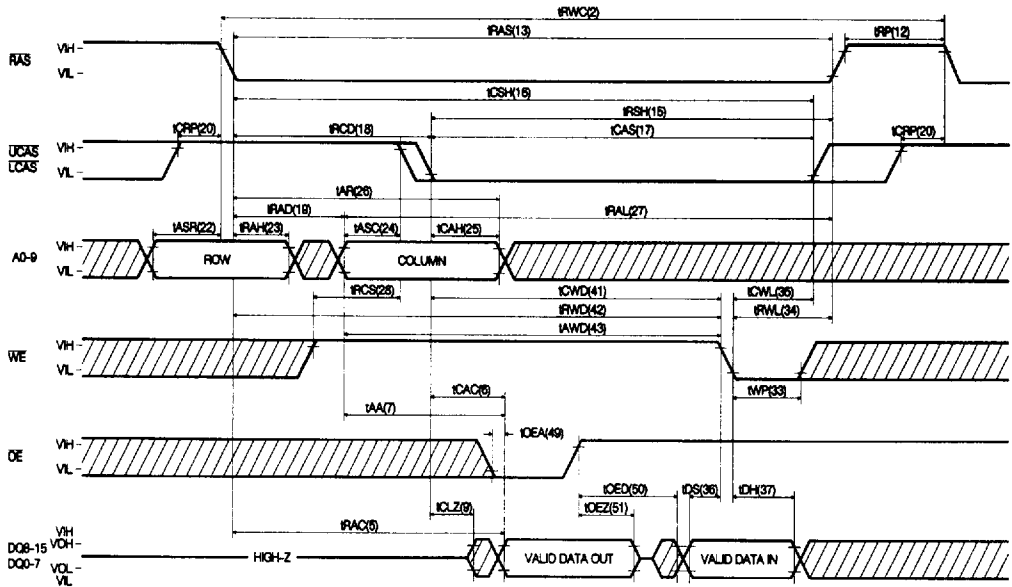


4675088 0004713 225

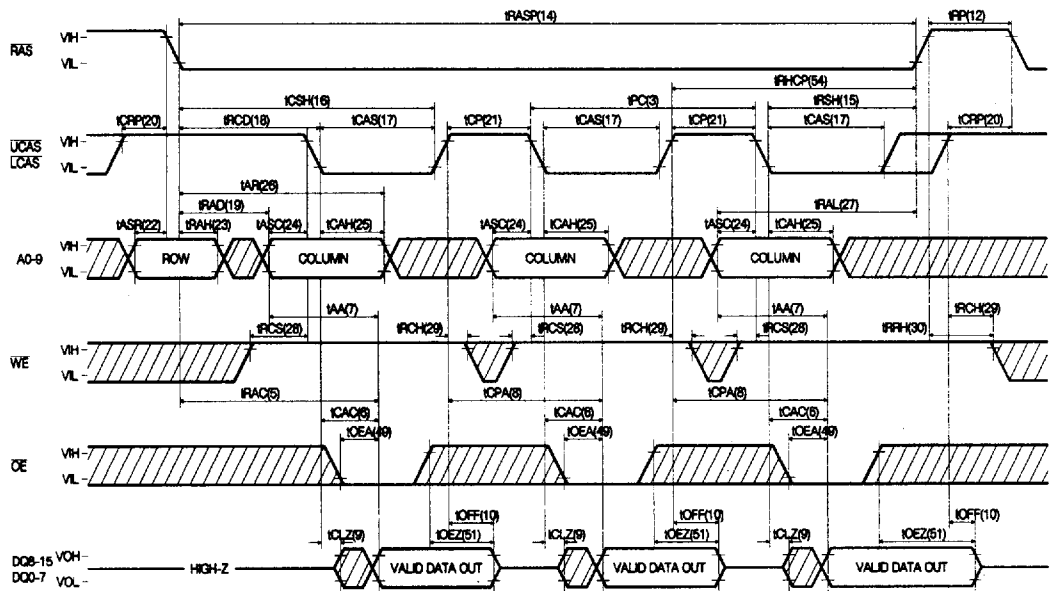
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



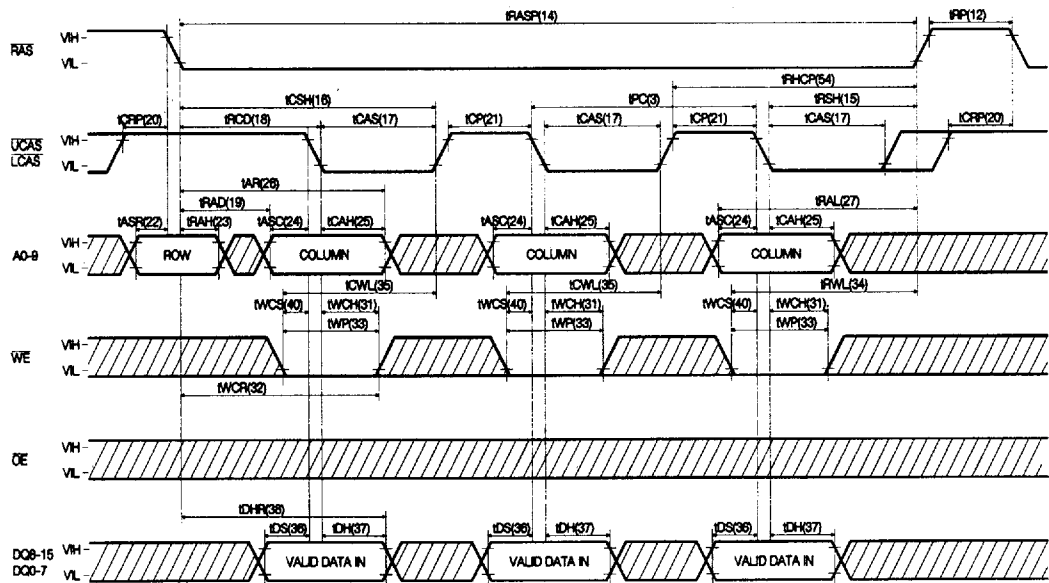
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

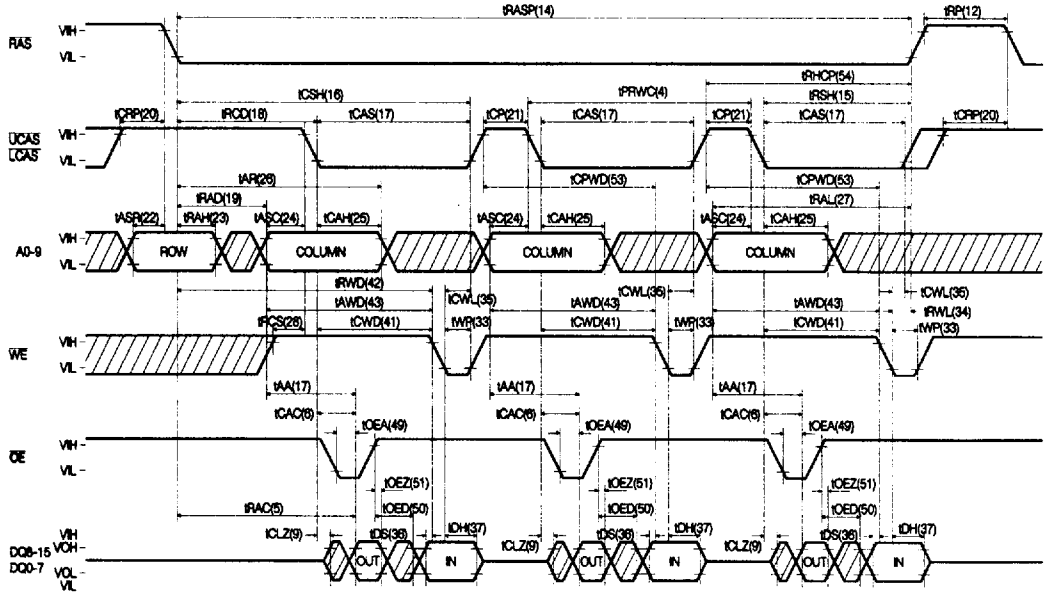


FAST PAGE MODE EARLY WRITE CYCLE

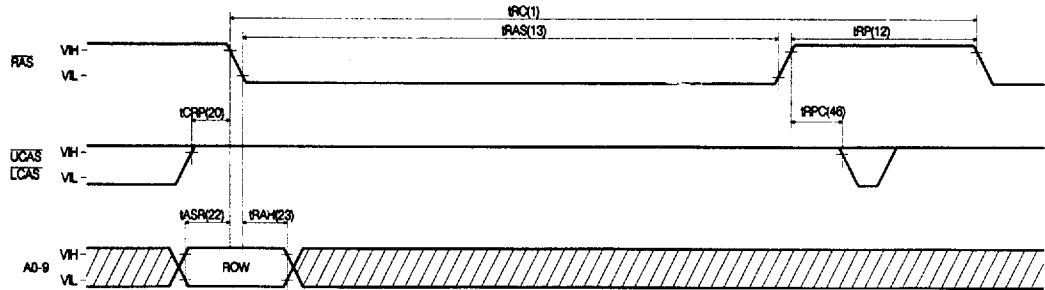


4675088 0004715 0T8

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

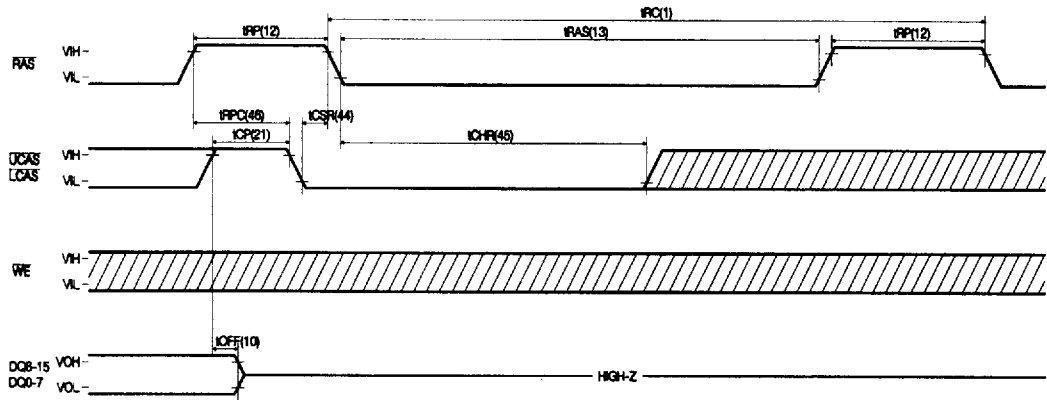


RAS-ONLY REFRESH CYCLE



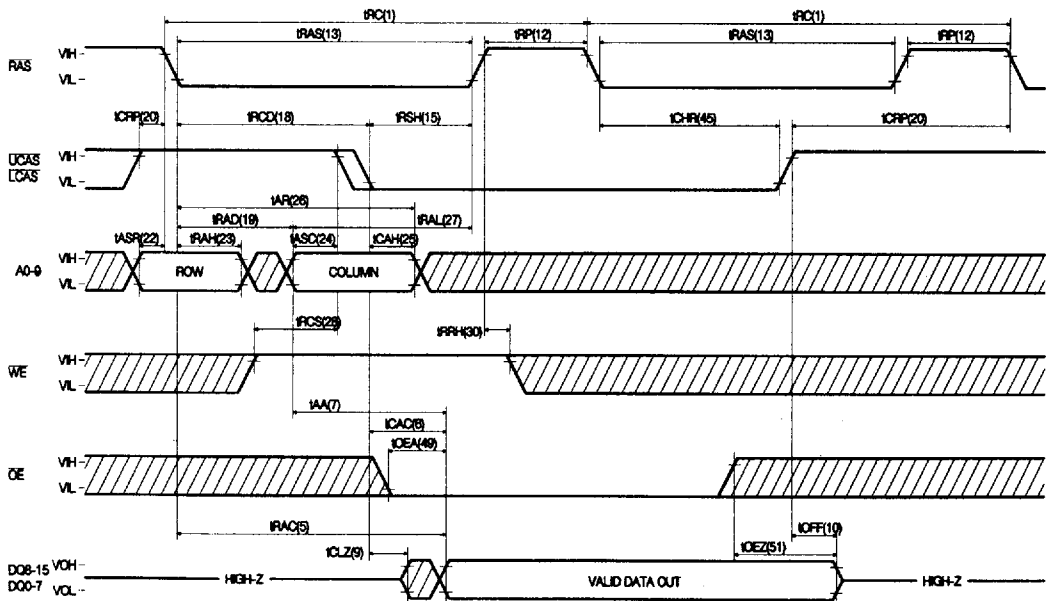
NOTE : OE and WE = "H" or "

CAS-BEFORE-RAS REFRESH CYCLE

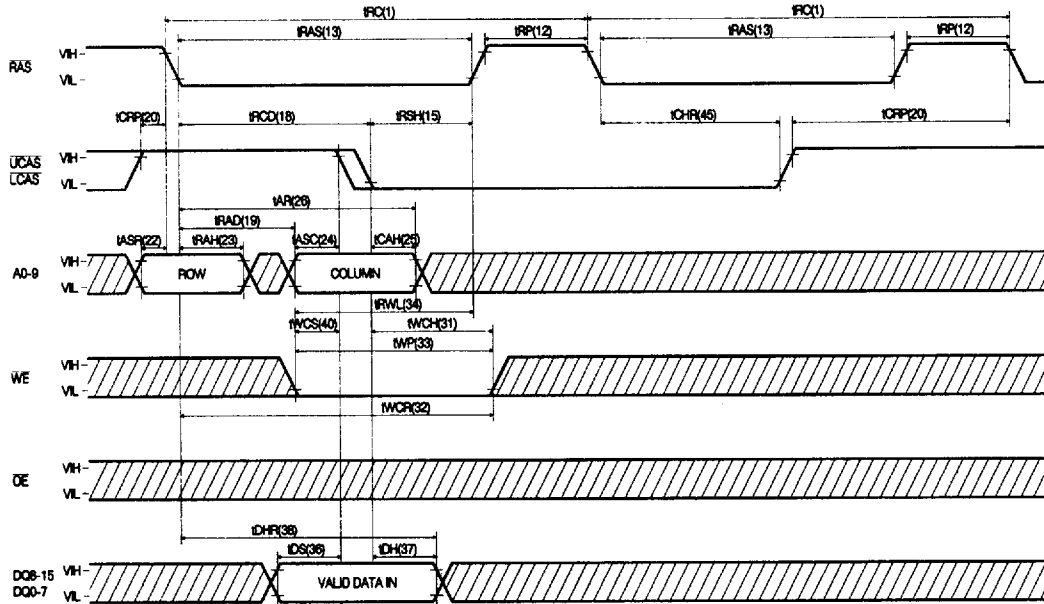


NOTE : A0-9 and OE = "H" or "L"

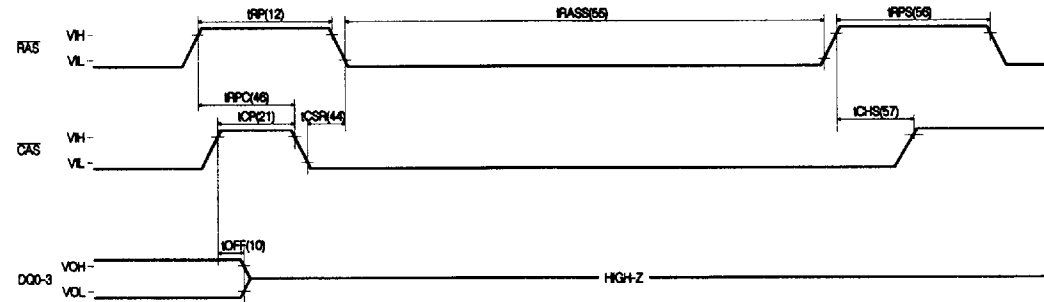
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

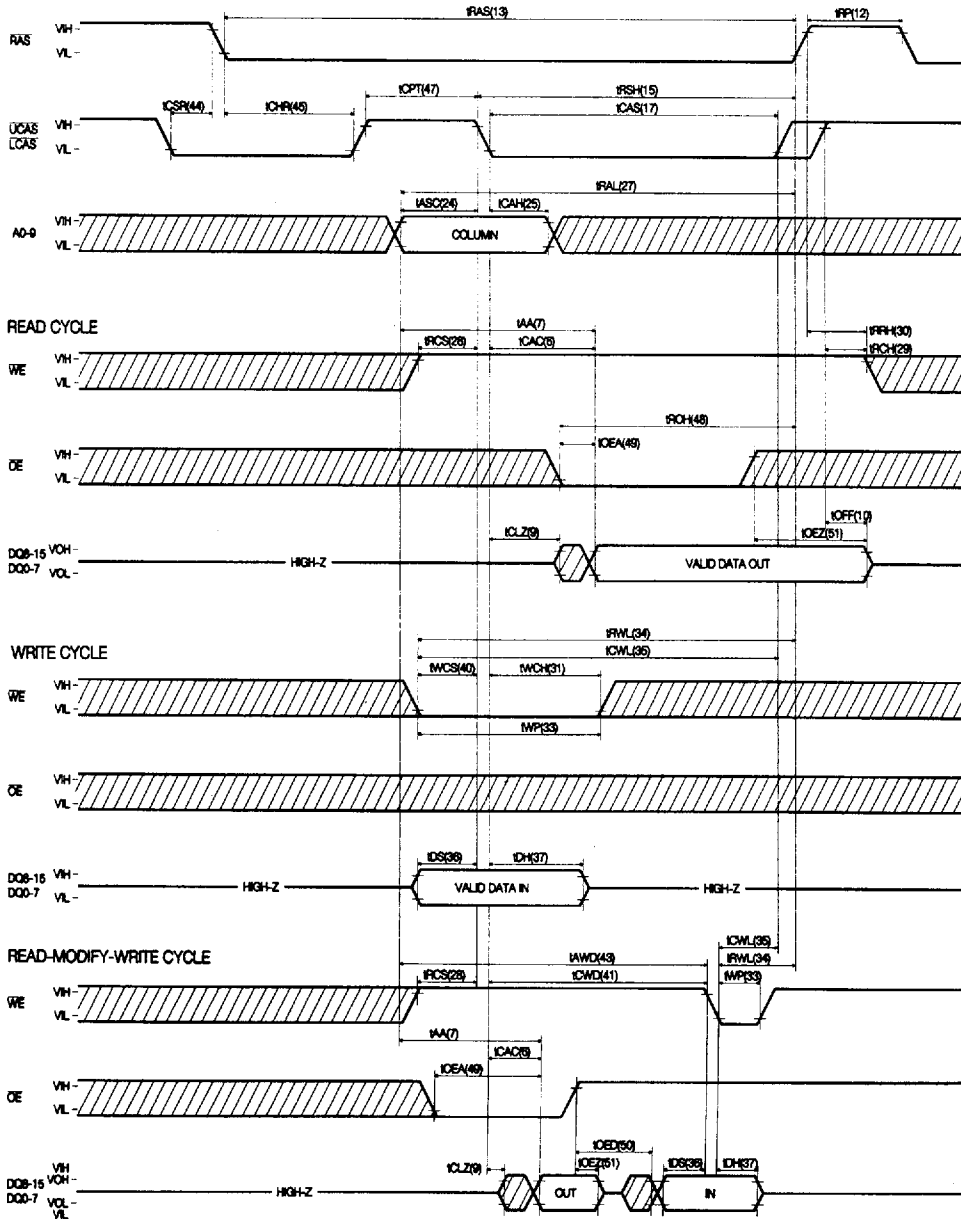


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : A0-9, OE and WE = 'H' or 'L'

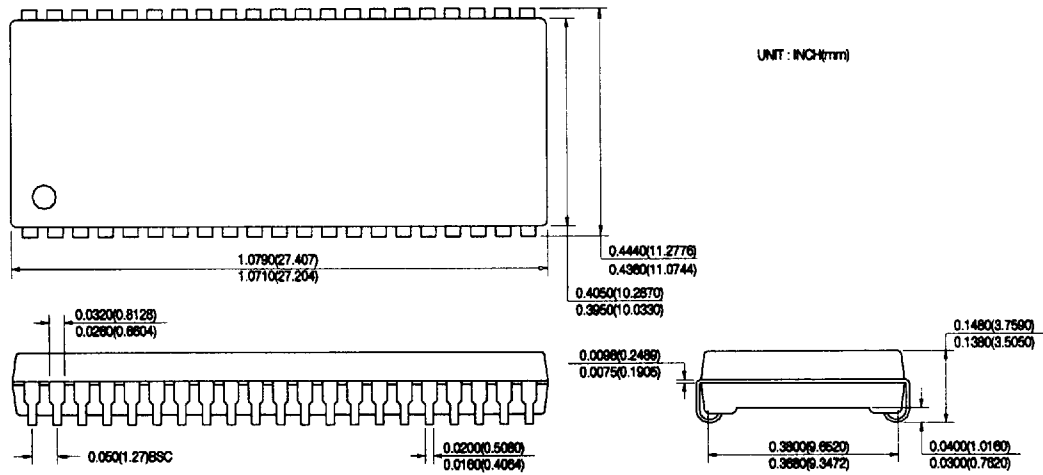
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



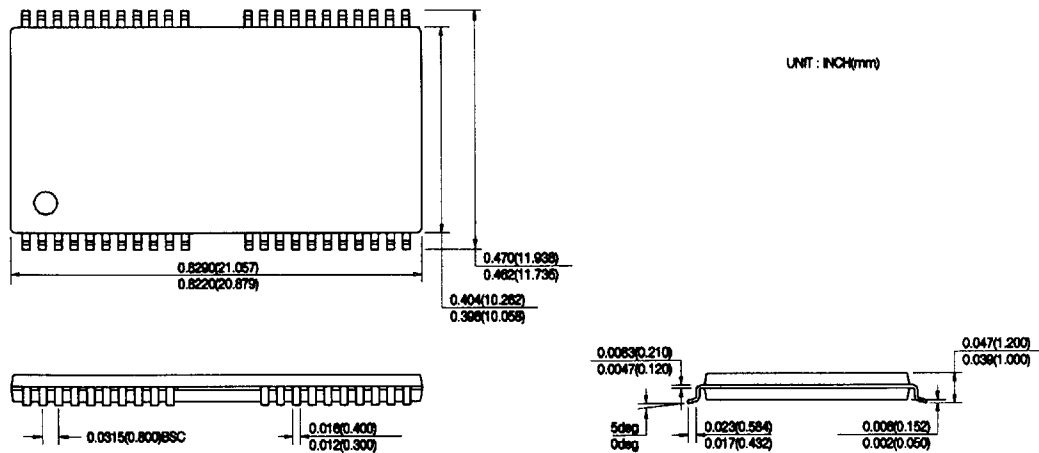
4675088 0004719 743

PACKAGE INFORMATION

400 mil 42/42 pin Small Outline J-form Package (JC)



400 mil 44/50 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY5118160JC	70/80/100		SOJ
HY5118160SLJC	70/80/100	SL-part	SOJ
HY5118160TC	70/80/100		TSOP-II
HY5118160SLTC	70/80/100	SL-part	TSOP-II
HY5118160RC	70/80/100		TSOP-II(R)
HY5118160SLRC	70/80/100	SL-part	TSOP-II(R)

■ 4675088 0004721 3T1 ■