MOTOROLA

MC74AC379
MC74ACT379

Product Preview

Quad Parallel Register with Enable

QUAD PARALLEL REGISTER WITH ENABLE

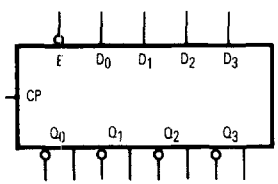
The MC74AC379/74ACT379 is a 4-bit register with a buffered common Enable. This device is similar to the MC74AC175/74ACT175 but features the common Enable rather than common Master Reset.

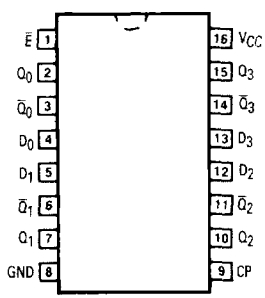
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Buffered Common Enable Input
- True and Complement Outputs
- Outputs Source/Sink 24 mA
- 'ACT379 Has TTL Compatible Inputs

N SUFFIX
CASE 648-08
PLASTIC

D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

$\overline{E}$	Enable Input
D_0–D_3	Data Inputs
CP	Clock Pulse Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

TRUTH TABLE

Inputs			Outputs	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⌐	X	NC	NC
L	⌐	H	H	L
L	⌐	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition
NC = No Change

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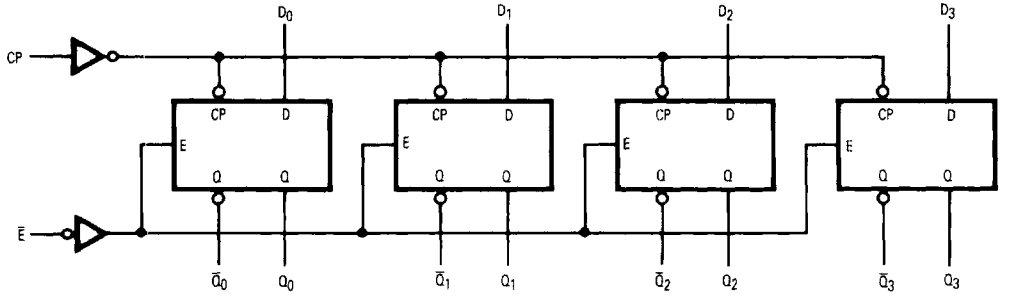
FUNCTIONAL DESCRIPTION

The MC74AC379/74ACT379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A =$ Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT379)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, $T_A =$ Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		118 160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n, $\overline{Q}_n$	3.3 5.0		8.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	3.3 5.0		8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	3.0 2.0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n, $\overline{Q}_n$	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	5.0		6.0				ns	3-6

*Voltage Range 5.0 s 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	5.0	2.0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

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