APPLICATION NOTE

AVAILABLE

AN95 • AN103 • AN107

128K X84129 MPS™ EEPROM

µPort Saver EEPROM

FEATURES

- **Up to 10MHz data transfer rate at 5V operator**
- **25ns Read Access Time**
- **Direct interface to microprocessors and microcontrollers**
  - **—Eliminates I/O port requirements**
  - **—No interface glue logic required**
  - **—Eliminates need for parallel to serial converters**
- **Low power CMOS**
  - **—2.5V–5.5V version**
  - **—Standby current less than 1µA**
  - **—Active current less than 1mA**
- **Byte or page write capable**
  - **—32-byte page write mode**
- **Typical nonvolatile write cycle time: 2ms**
- **High reliability**
  - **—100,000 endurance cycles**
  - **—Guaranteed data retention: 100 years**
- **Small packages options**
  - **—8-lead XBGA package**
  - **—14-lead SOIC package**
  - **—28-lead TSSOP package**

DESCRIPTION

The µPort Saver memories need no serial ports or special hardware and connect to the processor memory bus. Replacing bytewide data memory, the µPort Saver uses bytewide memory control functions, takes a fraction of the board space and consumes much less power. Replacing serial memories, the µPort Saver provides all the serial benefits, such as low cost, low power, low voltage, and small package size, while releasing I/Os for more important uses.

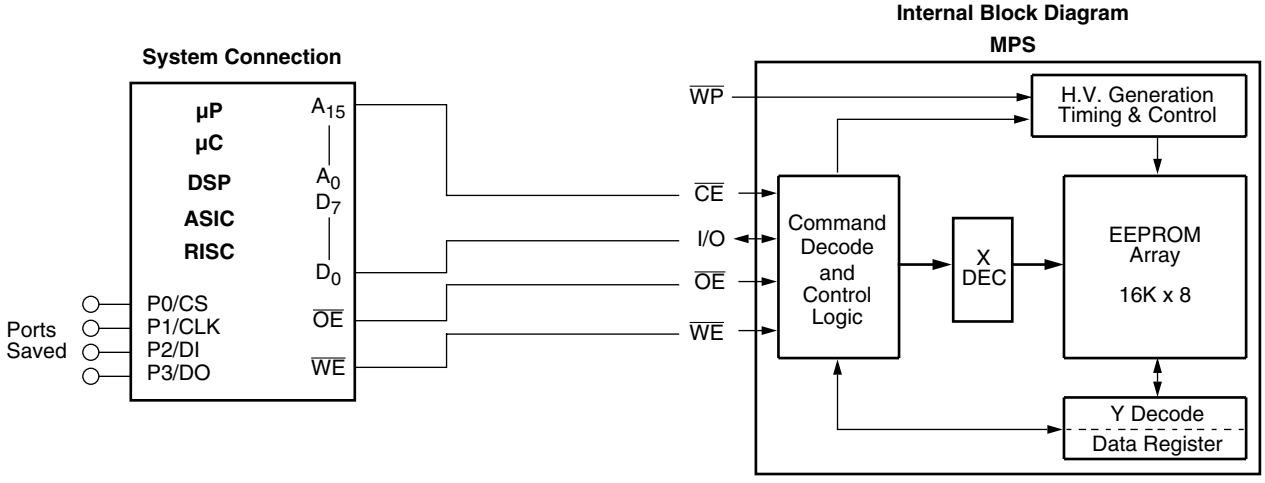
The µPort Saver memory outputs data within 25ns of an active read signal. This is less than the read access time of most hosts and provides “no-wait-state” operation. This prevents bottlenecks on the bus. With rates to 10MHz, the µPort Saver supplies data faster than required by most host read cycle specifications. This eliminates the need for software NOPs.

The µPort Saver memories communicate over one line of the data bus using a sequence of standard bus read and write operations. This “bit serial” interface allows the µPort Saver to work well in 8-bit, 16-bit, 32-bit, and 64-bit systems.

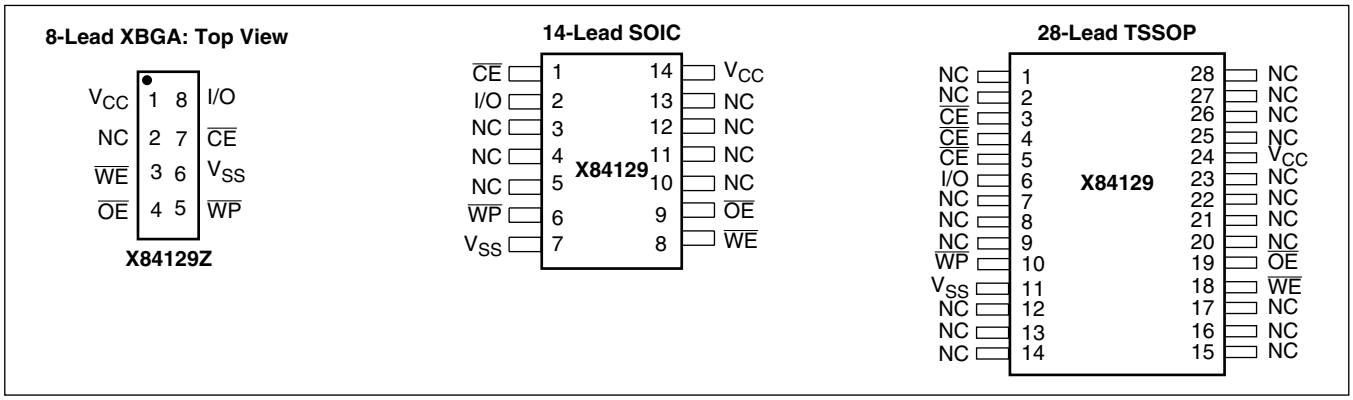
A Write Protect ($\overline{WP}$) pin prevents inadvertent writes to the memory.

Xicor EEPROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

Pin	Description
I/O	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{WP}$	Write Protect Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	No Connect

PACKAGE SELECTION GUIDE

84129	8-Lead XBGA 14-Lead SOIC 28-Lead TSSOP

PIN DESCRIPTIONS

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, the chip is deselected, the I/O pin is in the high impedance state, and unless a nonvolatile write operation is underway, the device is in the standby power mode.

Output Enable ($\overline{OE}$)

The Output Enable input must be LOW to enable the output buffer and to read data from the device on the I/O line.

Write Enable ($\overline{WE}$)

The Write Enable input must be LOW to write either data or command sequences to the device.

Data In/Data Out (I/O)

Data and command sequences are serially written to or serially read from the device through the I/O pin.

Write Protect ($\overline{WP}$)

When the Write Protect input is LOW, nonvolatile writes to the device are disabled. When $\overline{WP}$ is HIGH, all functions, including nonvolatile writes, operate normally. If a nonvolatile write cycle is in progress, $\overline{WP}$ going LOW will have no effect on the cycle already underway, but will inhibit any additional nonvolatile write cycles.

DEVICE OPERATION

The X84129 are serial EEPROMs designed to interface directly with most microprocessor buses. Standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ signals control the read and write operations, and a single I/O line is used to send and receive data and commands serially.

Data Timing

Data input on the I/O line is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Data output on the I/O line is active whenever both $\overline{OE}$ and $\overline{CE}$ are LOW. Care should be taken to ensure that $\overline{WE}$ and $\overline{OE}$ are never both LOW while $\overline{CE}$ is LOW.

Read Sequence

A read sequence consists of sending a 16-bit address followed by the reading of data serially. The address is written by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without a read cycle between the write cycles. The address is sent serially, most significant bit first, over the I/O line. Note that this sequence is fully static, with no special timing restrictions, and the processor is free to perform other tasks on the bus whenever the device $\overline{CE}$ pin is HIGH. Once the 16 address bits are sent, a byte of data can be read on the I/O line by issuing 8 separate read cycles ($\overline{OE}$ and $\overline{CE}$ LOW, $\overline{WE}$ HIGH). At this point, writing a '1' will terminate the read sequence and enter the low power standby state, otherwise the device will await further reads in the sequential read mode.

Sequential Read

The byte address is automatically incremented to the next higher address after each byte of data is read. The data stored in the memory at the next address can be read sequentially by continuing to issue read cycles. When the highest address in the array is reached, the address counter rolls over to address $0000 and reading may be continued indefinitely.

Reset Sequence

The reset sequence resets the device and sets an internal write enable latch. A reset sequence can be sent at any time by performing a read/write "0"/read operation (see Figs. 1 and 2). This breaks the multiple read or write cycle sequences that are normally used to read from or write to the part. The reset sequence can be used at any time to interrupt or end a sequential read or page load. As soon as the write "0" cycle is complete, the part is reset (unless a nonvolatile write cycle is in progress). The second read cycle in this sequence, and any further read cycles, will read a HIGH on the I/O pin until a valid read sequence (which includes the address) is issued. The reset sequence must be issued at the beginning of both read and write sequences to be sure the device initiates these operations properly.

Figure 1. Read Sequence

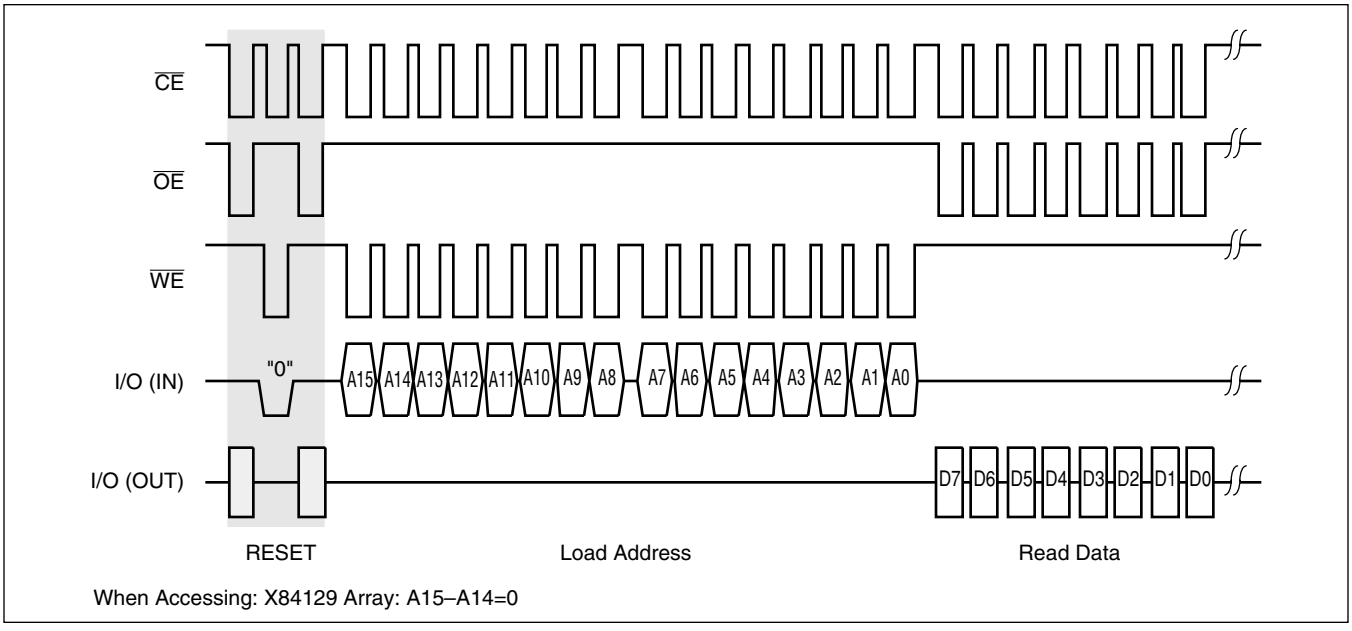
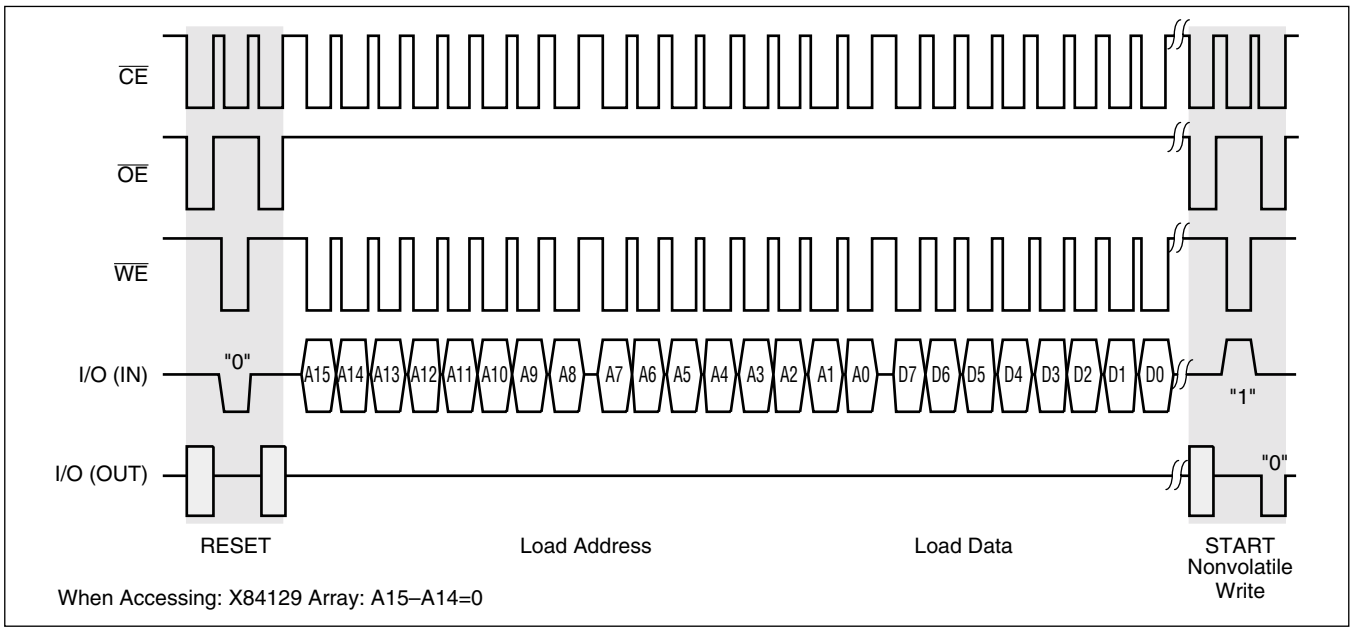


Figure 2. Write Sequence



Write Sequence

A nonvolatile write sequence consists of sending a reset sequence, a 16-bit address, up to 32 bytes of data, and then a special “start nonvolatile write cycle” command sequence.

The reset sequence is issued first (as described in the Reset Sequence section) to set an internal write enable latch. The address is written serially by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without any read cycles between the writes. The address is sent serially, most significant bit first, on the I/O pin. Up to 32 bytes of data are written by issuing a multiple of 8 write cycles. Again, no read cycles are allowed between writes.

The nonvolatile write cycle is initiated by issuing a special read/write “1”/read sequence. The first read cycle ends the page load, then the write “1” followed by a read starts the nonvolatile write cycle. The device recognizes 32-byte pages.

When sending data to the part, attempts to exceed the upper address of the page will result in the address counter “wrapping-around” to the first address on the page, where data loading can continue. For this reason, sending more than 256 consecutive data bits will result in overwriting previous data.

A nonvolatile write cycle will not start if a partial or incomplete write sequence is issued. The internal write enable latch is reset when the nonvolatile write cycle is completed and after an invalid write to prevent inadvertent writes. Note that this sequence is fully static, with no special timing restrictions. The processor is free to perform other tasks on the bus whenever the chip enable pin ($\overline{CE}$) is HIGH.

Nonvolatile Write Status

The status of a nonvolatile write cycle can be determined at any time by simply reading the state of the I/O pin on the device. This pin is read when $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH. During a nonvolatile write cycle the I/O pin is LOW. When the nonvolatile write cycle is complete, the I/O pin goes HIGH. A reset sequence can also be issued during a nonvolatile write cycle with the same result: I/O is LOW as long as a nonvolatile write cycle is in progress, and I/O is HIGH when the nonvolatile write cycle is done.

Low Power Operation

The device enters an idle state, which draws minimal current when:

– an illegal sequence is entered. The following are the more common illegal sequences:
  - Read/Write/Write—any time
  - Read/Write ‘1’—When writing the address or writing data.
  - Write ‘1’—when reading data
  - Read/Read/Write ‘1’—after data is written to device, but before entering the NV write sequence.

– the device powers-up;

– a nonvolatile write operation completes.

While a sequential read is in progress, the device remains in an active state. This state draws more current than the idle state, but not as much as during a read itself. To go back to the lowest power condition, an invalid condition is created by writing a ‘1’ after the last bit of a read operation.

Write Protection

The following circuitry has been included to prevent inadvertent nonvolatile writes:

– The internal Write Enable latch is reset upon power-up.

– A reset sequence must be issued to set the internal write enable latch before starting a write sequence.

– A special “start nonvolatile write” command sequence is required to start a nonvolatile write cycle.

– The internal Write Enable latch is reset automatically at the end of a nonvolatile write cycle.

– The internal Write Enable latch is reset and remains reset as long as the $\overline{WP}$ pin is LOW, which blocks all nonvolatile write cycles.

– The internal Write Enable latch resets on an invalid write operation.

ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....–65°C to +135°C
Storage temperature .....–65°C to +150°C
Terminal voltage with respect to V_{SS}.....–1V to +7V
DC output current..... 5mA
Lead temperature (soldering, 10 seconds).....300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions (above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

Supply Voltage	Limits
X84129-2.5	2.5V to 5.5V

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} supply current (read)		1	mA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 10MHz
I_{CC2}	V_{CC} supply current (write)		2	mA	I_{CC} during nonvolatile write cycle all inputs at CMOS levels
I_{SB1}	V_{CC} standby current		1	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS}
I_{LI}	Input leakage current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH voltage	V_{CC} – 0.8		V	I_{OH} = –1mA

Note: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not tested.

D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.5V to 5.5V)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} supply current (Read)		500	µA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 5MHz
I_{CC2}	V_{CC} supply current (Write)		2	mA	I_{CC} during nonvolatile write cycle all inputs at CMOS levels
I_{SB1}	V_{CC} standby current		1	µA	$\overline{CE}$ = V_{CC}, Other inputs = V_{CC} or V_{SS}
I_{LI}	Input leakage current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW voltage		0.4	V	I_{OL} = 1mA, V_{CC} = 3V
V_{OH}	Output HIGH voltage	V_{CC} – 0.4		V	I_{OH} = –400µA, V_{CC} = 3V

CAPACITANCE T_A = +25°C, F = 1MHZ, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Test Conditions
$C_{I/O}$(2)	Input/Output capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input capacitance	6	pF	V_{IN} = 0V

Note: (2) Periodically sampled, but not 100% tested.

POWER-UP TIMING

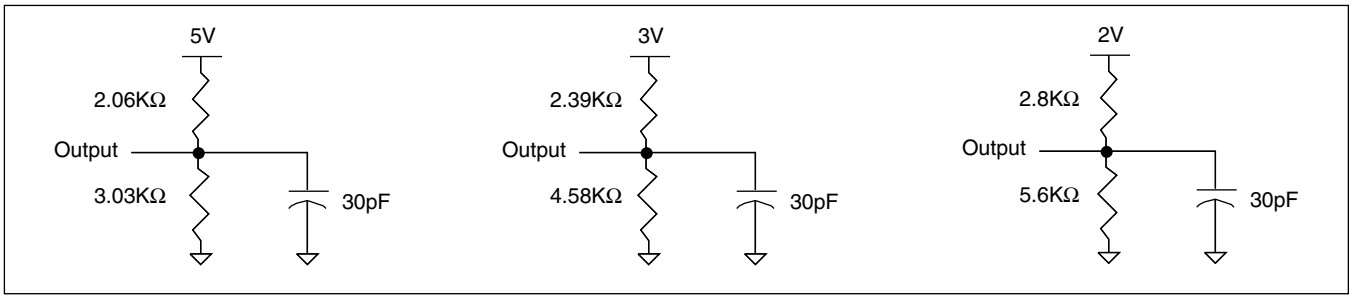
Symbol	Parameter	Max.	Unit
t_{PUR}(3)	Power-up to read operation	2	ms
t_{PUW}(3)	Power-up to write operation	5	ms

Note: (3) Time delays required from the time the V_{CC} is stable until the specific operation can be initiated. Periodically sampled, but not 100% tested.

A.C. CONDITIONS OF TEST

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	5ns
Input and output timing levels	V_{CC} x 0.5

EQUIVALENT A.C. LOAD CIRCUITS



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

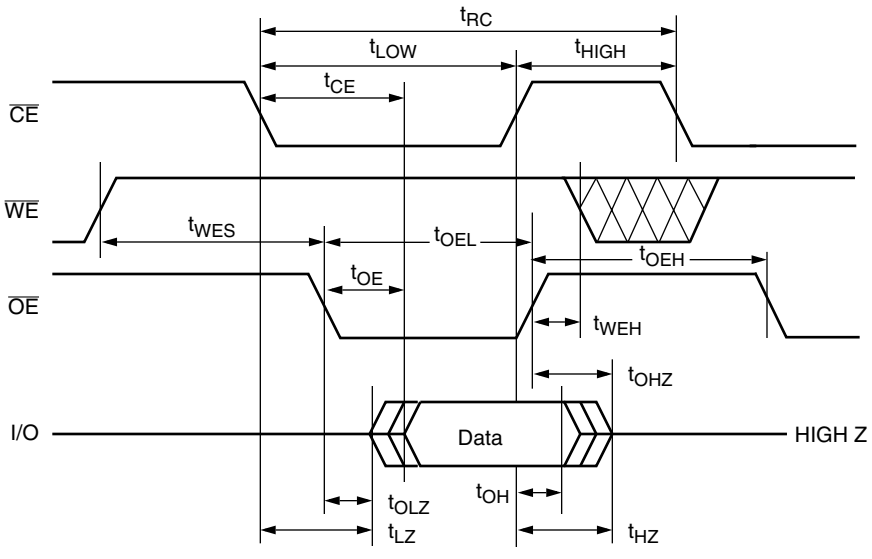
Read Cycle Limits–X84129†

Symbol	Parameter	V_{CC} = 2.5V – 5.5V		Unit
		Min.	Max.	
t_{RC}	Read cycle time	200		ns
t_{CE}	$\overline{CE}$ access time		50	ns
t_{OE}	$\overline{OE}$ access time		50	ns
t_{OEL}	$\overline{OE}$ pulse width	60		ns
t_{OEH}	$\overline{OE}$ High recovery time	60		ns
t_{LOW}	$\overline{CE}$ LOW time	70		ns
t_{HIGH}	$\overline{CE}$ HIGH time	120		ns
t_{LZ}(4)	$\overline{CE}$ LOW to output in low Z	0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to output in high Z	0	30	ns
t_{OLZ}(4)	$\overline{OE}$ LOW to output in low Z	0		ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to output in high Z	0	30	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$ HIGH	0		ns
t_{WES}	$\overline{WE}$ HIGH setup time	25		ns
t_{WEH}	$\overline{WE}$ HIGH hold time	25		ns

Note: (4) Periodically sampled, but not 100% tested. t_{HZ} and t_{OHZ} are measured from the point where $\overline{CE}$ or $\overline{OE}$ goes HIGH (whichever occurs first) to the time when I/O is no longer being driven into a 5pF load.

† Contact factory for 10MHz X84129 availability

Read Cycle

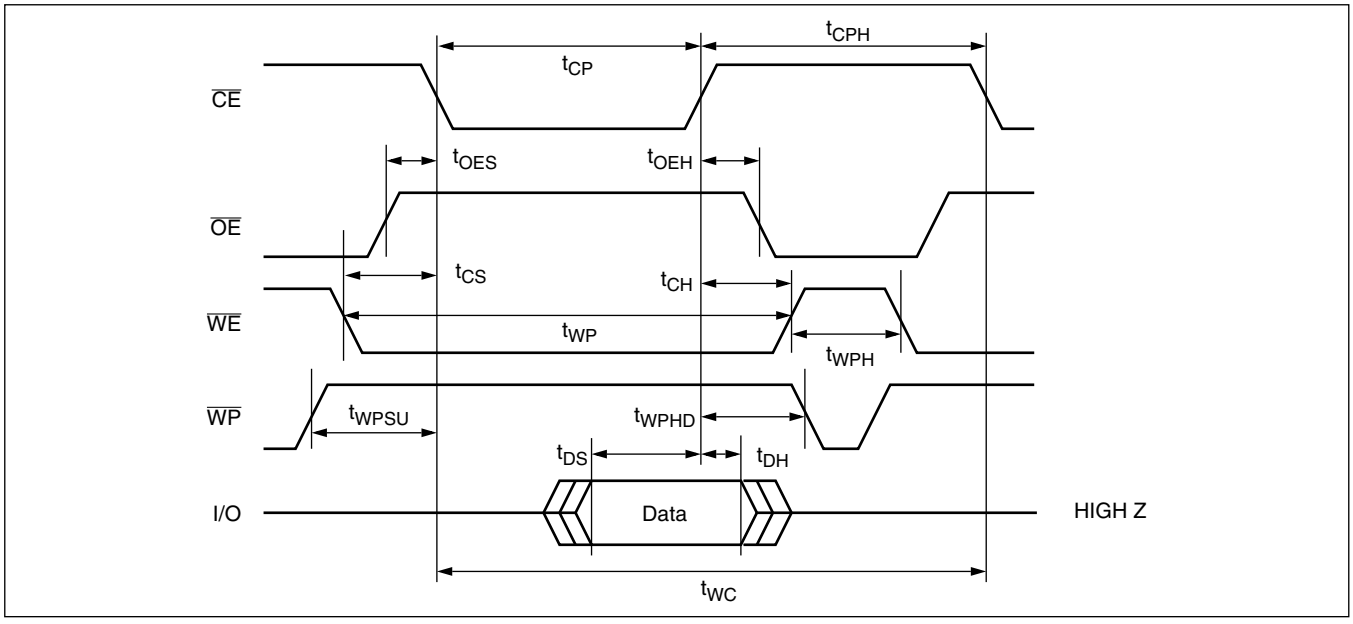


Write Cycle Limits–X84129

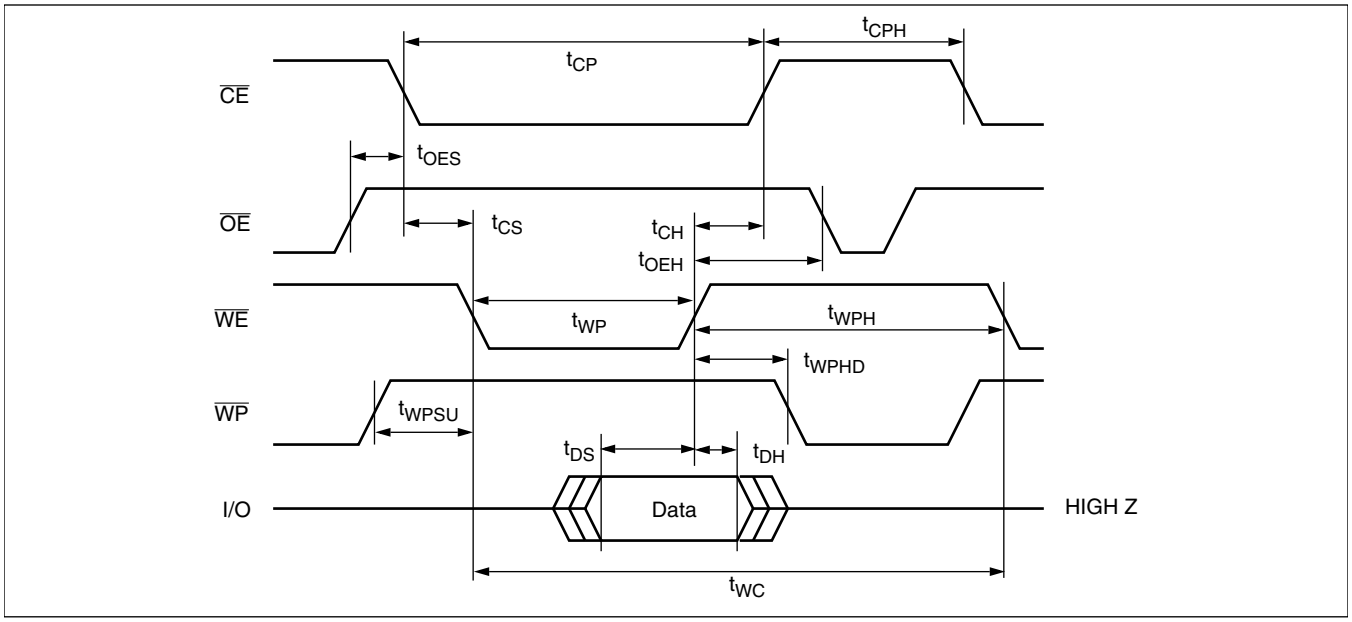
Symbol	Parameter	V_{CC} = 2.5V – 5.5V		Unit
		Min.	Max.	
t_{NVWC}[5]	Nonvolatile write cycle time		5	ms
t_{WC}	Write cycle time	200		ns
t_{WP}	$\overline{WE}$ pulse width	40		ns
t_{WPH}	$\overline{WE}$ HIGH recovery time	150		ns
t_{CS}	Write setup time	0		ns
t_{CH}	Write hold time	0		ns
t_{CP}	$\overline{CE}$ pulse width	40		ns
t_{CPH}	$\overline{CE}$ HIGH recovery time	150		ns
t_{OES}	$\overline{OE}$ HIGH setup time	25		ns
t_{OEH}	$\overline{OE}$ HIGH hold time	25		ns
t_{DS}[6]	Data setup time	20		ns
t_{DH}[6]	Data hold time	5		ns
t_{WPSU}[7]	$\overline{WP}$ HIGH setup	100		ns
t_{WPHD}[7]	$\overline{WP}$ HIGH hold	100		ns

Notes: (5) t_{NVWC} is the time from the falling edge of $\overline{OE}$ or $\overline{CE}$ (whichever occurs last) of the second read cycle in the “start nonvolatile write cycle” sequence until the self-timed, internal nonvolatile write cycle is completed.
(6) Data is latched into the X84129 on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(7) Periodically sampled, but not 100% tested.

$\overline{CE}$ Controlled Write Cycle



$\overline{WE}$ Controlled Write Cycle



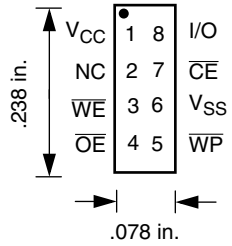
PACKAGING INFORMATION

8-Lead XBGA

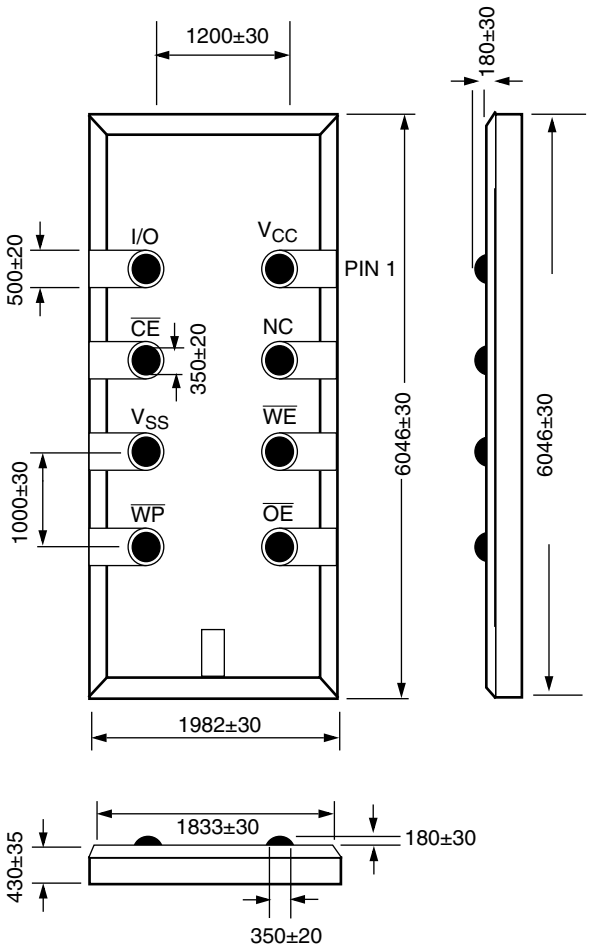
8-Lead XBGA Package

Complete Part Number	Top Mark
X84129Z - 2.5	XAAG
X84129ZI - 2.5	XADF

8-Lead XBGA: Top View



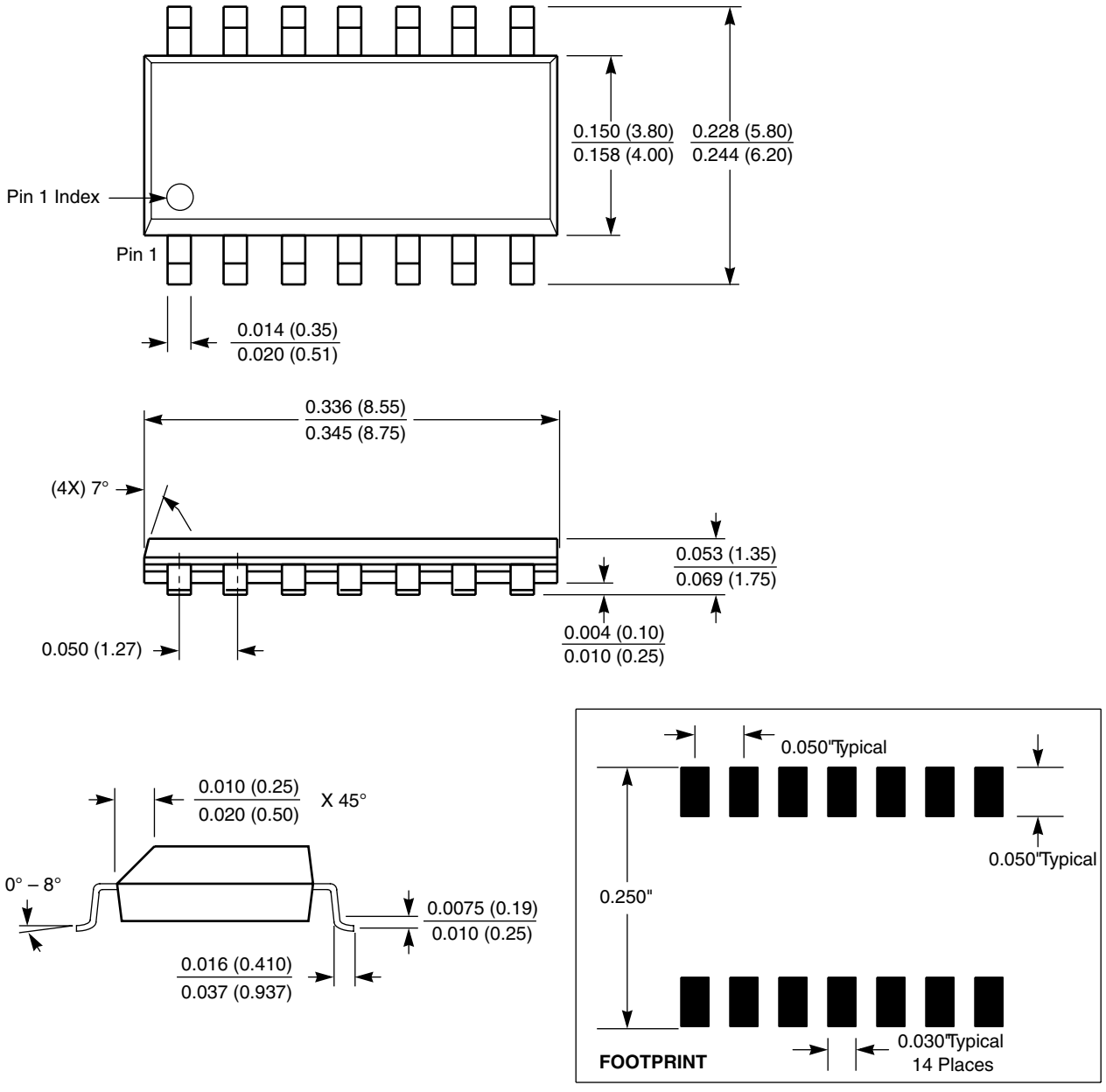
X84129: Bottom View



NOTE: ALL DIMENSIONS IN µM (to convert into inches, 1µm = 3.94 x 10^{-5} inch)
ALL DIMENSIONS ARE TYPICAL VALUES

PACKAGING INFORMATION

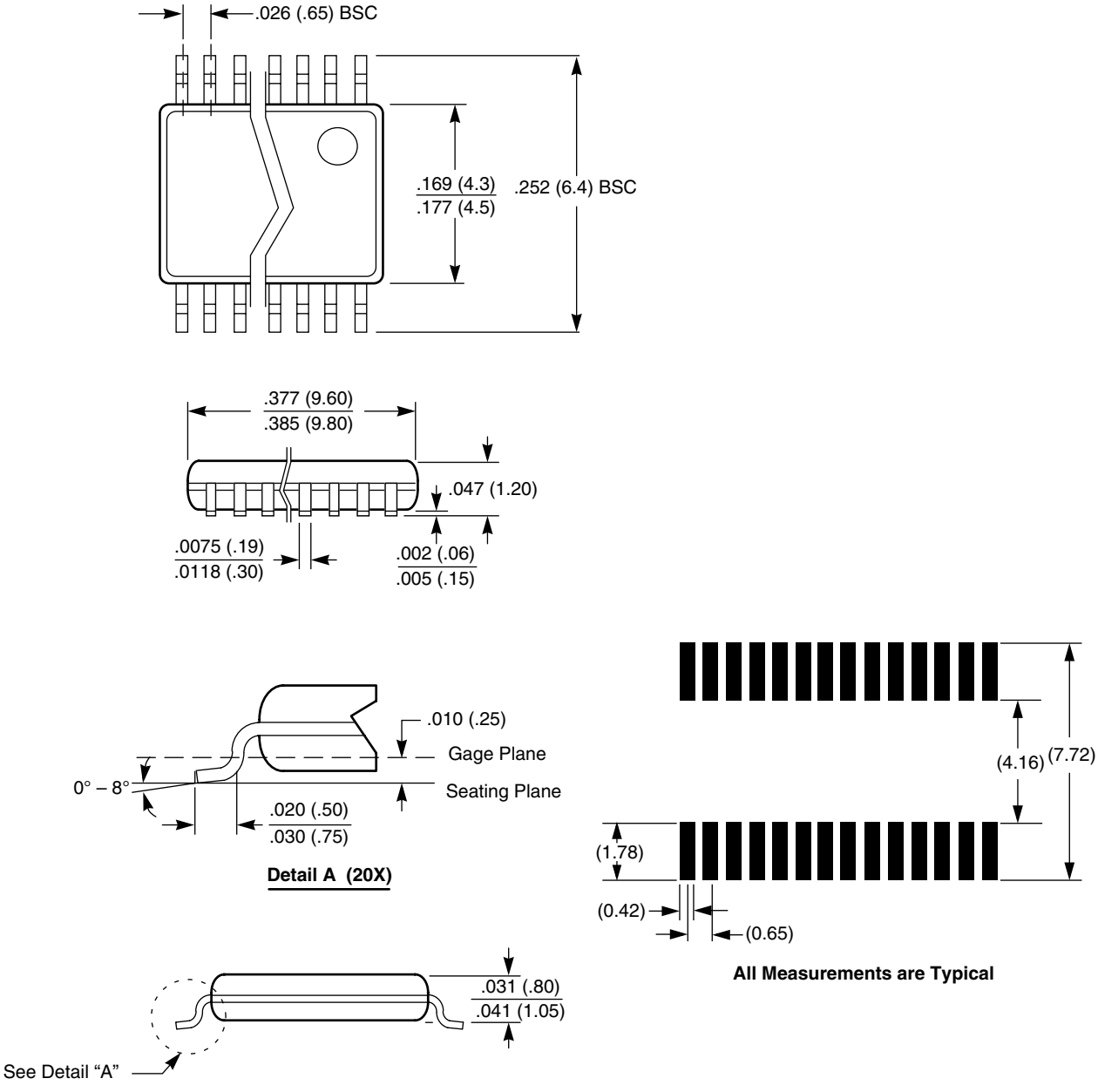
14-Lead Plastic Small Outline Gullwing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

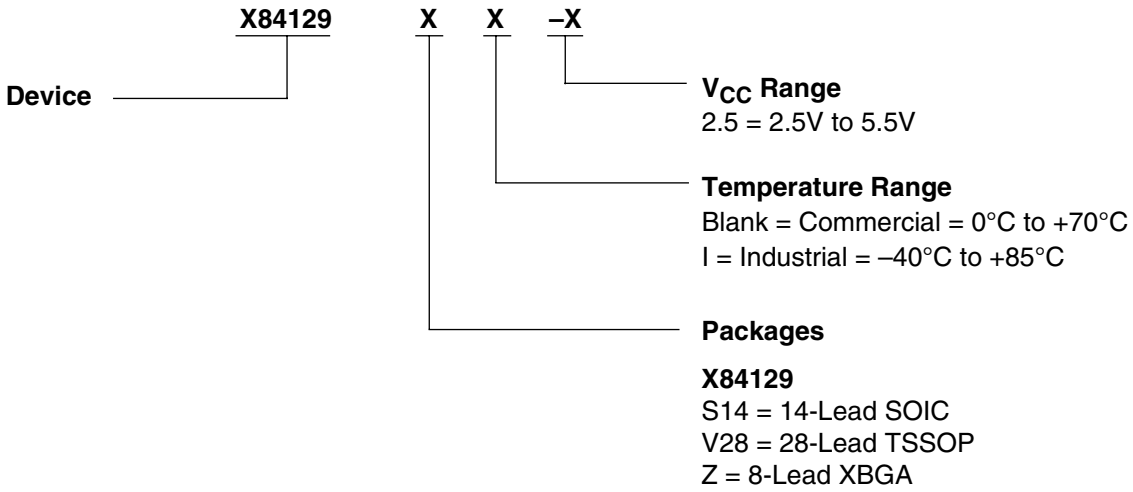
PACKAGING INFORMATION

28-Lead Plastic, TSSOP Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information



Part Mark Convention

8-Lead XBGA Package

Complete Part Number	Top Mark
X84129Z-2.5	XAAG
X84129ZI-2.5	XADF