256K x 36/512K x 18 Pipelined SRAM with NoBL™ Architecture

Features

- **Pin-compatible and functionally equivalent to ZBT™**
- **Supports 250-MHz bus operations with zero wait states**
  - **Available speed grades are 250, 200 and 166 MHz**
- **Internally self-timed output buffer control to eliminate the need to use asynchronous OE**
- **Fully registered (inputs and outputs) for pipelined operation**
- **Byte Write capability**
- **Separate V_{DDQ} for 3.3V or 2.5V I/O**
- **Single 3.3V power supply**
- **Fast clock-to-output times**
  - **2.6 ns (for 250-MHz device)**
  - **3.0ns (for 200-MHz device)**
  - **3.5 ns (for 166-MHz device)**
- **Clock Enable (CEN) pin to suspend operation**
- **Synchronous self-timed writes**
- **Available in 100 TQFP, 119 BGA, and 165 fBGA packages**
- **IEEE 1149.1 JTAG-compatible Boundary Scan**
- **Burst capability—linear or interleaved burst order**
- **"ZZ" Sleep Mode option and Stop Clock option**

Functional Description

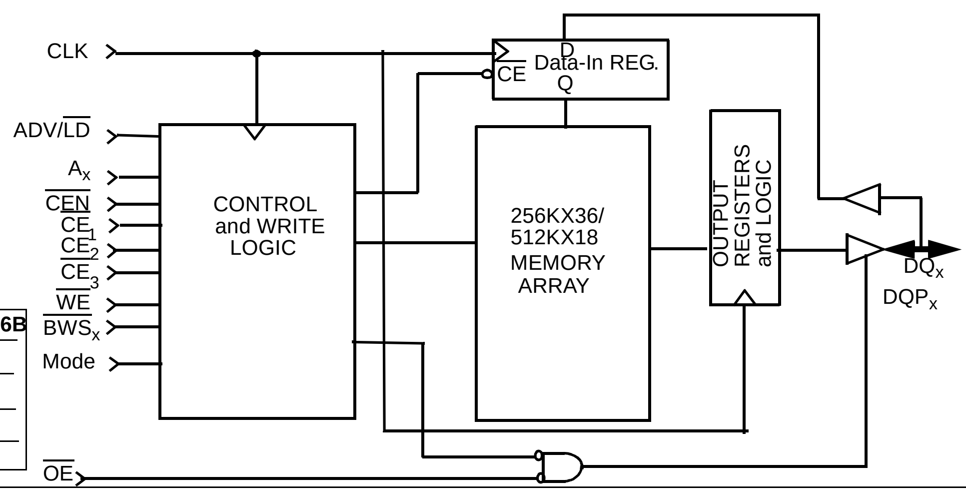
The CY7C1354B and CY7C1356B are 3.3V, 256K x 36 and 512K x 18 Synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The CY7C1354B and CY7C1356B are equipped with the advanced (NoBL) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write/Read transitions. The CY7C1354B and CY7C1356B are pin compatible and functionally equivalent to ZBT devices.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable (CEN) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 2.6 ns (250-MHz device).

Write operations are controlled by the Byte Write Selects (BWS_a–BWS_d for CY7C1354B and BWS_a–BWS_b for CY7C1356B) and a Write Enable (WE) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables (CE_1, CE_2, CE_3) and an asynchronous Output Enable (OE) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drivers are synchronously three-stated during the data portion of a write sequence.

Logic Block Diagram



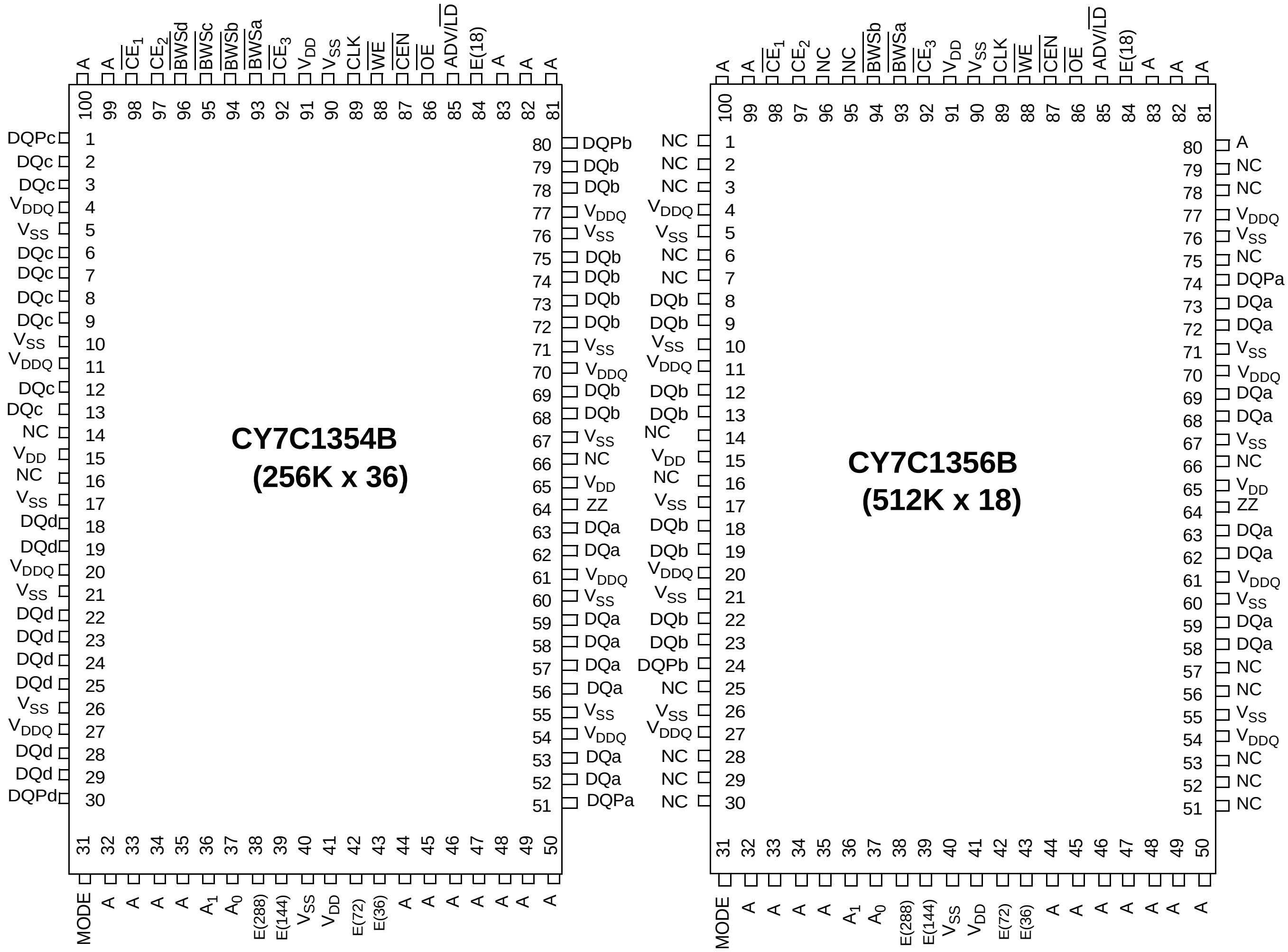
	CY7C1354B	CY7C1356B
A_X	X = 17:0	X = 18:0
DQ_X	X = a, b, c, d	X = a, b
DQP_X	X = a, b, c, d	X = a, b
BWS_X	X = a, b, c, d	X = a, b

Selection Guide

		CY7C1354B-250 CY7C1356B-250	CY7C1354B-200 CY7C1356B-200	CY7C1354B-166 CY7C1356B-166	Unit
Maximum Access Time		2.6	3.0	3.5	ns
Maximum Operating Current	Com'l	250	220	180	mA
Maximum CMOS Standby Current	Com'l	30	30	30	mA

Pin Configurations

100-pin TQFP Packages



Pin Configurations (continued)

119-ball BGA Pinout

CY7C1354B (256K x 36)–7 x 17 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	E(18)	A	A	V_{DDQ}
B	NC	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE}_3$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_c	DQP_c	V_{SS}	NC	V_{SS}	DQP_b	DQ_b
E	DQ_c	DQ_c	V_{SS}	$\overline{CE}_1$	V_{SS}	DQ_b	DQ_b
F	V_{DDQ}	DQ_c	V_{SS}	$\overline{OE}$	V_{SS}	DQ_b	V_{DDQ}
G	DQ_c	DQ_c	$\overline{BWS}_c$	A	$\overline{BWS}_b$	DQ_b	DQ_b
H	DQ_c	DQ_c	V_{SS}	$\overline{WE}$	V_{SS}	DQ_b	DQ_b
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_d	DQ_d	V_{SS}	CLK	V_{SS}	DQ_a	DQ_a
L	DQ_d	DQ_d	$\overline{BWS}_d$	NC	$\overline{BWS}_a$	DQ_a	DQ_a
M	V_{DDQ}	DQ_d	V_{SS}	$\overline{CEN}$	V_{SS}	DQ_a	V_{DDQ}
N	DQ_d	DQ_d	V_{SS}	A1	V_{SS}	DQ_a	DQ_a
P	DQ_d	DQP_d	V_{SS}	A0	V_{SS}	DQP_a	DQ_a
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	E(72)	A	A	A	E(36)	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1356B (512K x 18)–7 x 17 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	E(18)	A	A	V_{DDQ}
B	NC	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE}_3$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_b	NC	V_{SS}	NC	V_{SS}	DQP_a	NC
E	NC	DQ_b	V_{SS}	$\overline{CE}_1$	V_{SS}	NC	DQ_a
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_a	V_{DDQ}
G	NC	DQ_b	$\overline{BWS}_b$	A	V_{SS}	NC	DQ_a
H	DQ_b	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQ_a	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_b	V_{SS}	CLK	V_{SS}	NC	DQ_a
L	DQ_b	NC	V_{SS}	NC	$\overline{BWS}_a$	DQ_a	NC
M	V_{DDQ}	DQ_b	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	DQ_b	NC	V_{SS}	A1	V_{SS}	DQ_a	NC
P	NC	DQP_b	V_{SS}	A0	V_{SS}	NC	DQ_a
R	NC	A	MODE	V_{DD}	NC	A	NC
T	E(72)	A	A	E(36)	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

165-Ball fBGA Pinout

CY7C1354B (256K x 36)–13 x 15 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	E(288)	A	$\overline{CE_1}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{CE_3}$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC	A	CE2	$\overline{BW_d}$	$\overline{BW_a}$	CLK	$\overline{WE}$	$\overline{OE}$	E(18)	A	E(144)
C	DQP_c	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_b
D	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
E	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
F	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
G	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
K	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
L	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
M	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
N	DQP_d	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_a
P	NC	E(72)	A	A	TDI	A1	TDO	A	A	A	NC
R	MODE	E(36)	A	A	TMS	A0	TCK	A	A	A	A

CY7C1356B (512K x 18)–13 x 15 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	E(288)	A	$\overline{CE_1}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{CE_3}$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	A
B	NC	A	CE2	$\overline{BW_d}$	$\overline{BW_a}$	CLK	$\overline{WE}$	$\overline{OE}$	E(18)	A	E(144)
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_b
D	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_b
E	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_b
F	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_b
G	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_b
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
K	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
L	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
M	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
N	DQP_b	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	E(72)	A	A	TDI	A1	TDO	A	A	A	NC
R	MODE	E(36)	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Pin Name	I/O Type	Pin Description
A0 A1 A	Input- Synchronous	**Address Inputs used to select one of the address locations**. Sampled at the rising edge of the CLK.
$\overline{BWS}_a$ $\overline{BWS}_b$ $\overline{BWS}_c$ $\overline{BWS}_d$	Input- Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BWS}_a$ controls DQ_a and DQP_a, $\overline{BWS}_b$ controls DQ_b and DQP_b, $\overline{BWS}_c$ controls DQ_c and DQP_c, $\overline{BWS}_d$ controls DQ_d and DQP_d.
$\overline{WE}$	Input- Synchronous	**Write Enable Input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input- Synchronous	**Advance/Load Input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
CLK	Input- Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input- Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input- Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input- Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input- Asynchronous	**Output Enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input- Synchronous	**Clock Enable Input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_a DQ_b DQ_c DQ_d	I/O- Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a three-state condition. The outputs are automatically three-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_a DQP_b DQP_c DQP_d	I/O- Synchronous	**Bidirectional Data Parity I/O lines**. Functionally, these signals are identical to $DQ_{[31:0]}$. During write sequences, DQP_a is controlled by $\overline{BWS}_a$, DQP_b is controlled by $\overline{BWS}_b$, DQP_c is controlled by $\overline{BWS}_c$, and DQP_d is controlled by $\overline{BWS}_d$.
MODE	Input Strap Pin	**Mode Input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK.
TDI	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK.
TMS	Test Mode Select Synchronous	**This pin controls the Test Access Port state machine**. Sampled on the rising edge of TCK.
TCK	JTAG-Clock	**Clock input to the JTAG circuitry**.
V_{DD}	Power Supply	**Power supply for the 3.3V control logic**.
V_{DDQ}	I/O Power Supply	**Either 3.3V or 2.5V power supply for the I/O circuitry**.

Pin Definitions

Pin Name	I/O Type	Pin Description
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
NC	–	**No connects**.
E(18,36,72, 144, 288)	–	**These pins are not connected**. They will be used for expansion to the 18M, 36M, 72M, 144M and 288M densities.
ZZ	Input-Asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin can be connected to Vss or left floating.

Introduction

Functional Overview

The CY7C1354B and CY7C1356B are synchronous-pipelined Burst NoBL SRAMs designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.6 ns (250-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $\overline{BWS}_{[d:a]}$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.0 ns (200-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will three-state following the next clock rise.

Burst Read Accesses

The CY7C1354B and CY7C1356B have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented to A_0–A_{16} is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically three-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b}$ for CY7C1354B and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356B). In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the Address Register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b}$ for CY7C1354B & $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356B) (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the Write operation is controlled by $\overline{BWS}$ ($\overline{BWS}_{a,b,c,d}$ for CY7C1354B and $\overline{BWS}_{a,b}$ for CY7C1356B) signals. The CY7C1354B/56BV25 provides byte write capability that is described in the Write Cycle Description table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BWS}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations.

Byte write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1354B and CY7C1356B are common I/O devices, data should not be driven into the device while the outputs are active. The Output Enable (OE) can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b}$ for CY7C1354B and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356B) inputs. Doing so will three-state the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}$/ $DQP_{a,b}$ for CY7C1354B and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356B) are automatically three-stated during the data portion of a write cycle, regardless of the state of OE.

Burst Write Accesses

The CY7C1354B/56B has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four WRITE operations without reasserting the address inputs. ADV/LD must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables (CE_1, CE_2, and CE_3) and WE inputs are ignored and the burst counter is incremented. The correct BWS ($BWS_{a,b,c,d}$ for CY7C1354B and $BWS_{a,b}$ for CY7C1356B) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. CE_1, CE_2, CE_3, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		35	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

Cycle Description Truth Table[1, 2, 3, 4, 5, 6]

Operation	Address Used	CE	CEN	ADV/LD/	WE	BWS_x	CLK	Comments
Deselected	External	1	0	L	X	X	L-H	I/Os three-state following next recognized clock.
Suspend	–	X	1	X	X	X	L-H	Clock ignored, all operations suspended.
Begin Read	External	0	0	0	1	X	L-H	Address latched.
Begin Write	External	0	0	0	0	Valid	L-H	Address latched, data presented two valid clocks later.
Burst Read Operation	Internal	X	0	1	X	X	L-H	Burst Read operation. Previous access was a Read operation. Addresses incremented internally in conjunction with the state of Mode.
Burst Write Operation	Internal	X	0	1	X	Valid	L-H	Burst Write operation. Previous access was a Write operation. Addresses incremented internally in conjunction with the state of MODE. Bytes written are determined by $BWS_{[d:a]}$.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Notes:

1. X = "don't care," 1 = Logic HIGH, 0 = Logic LOW, CE stands for ALL Chip Enables active. BWS_X = 0 signifies at least one Byte Write Select is active, BWS_X = Valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by WE and BWS_X. See Write Cycle Description table for details.
3. The DQ and DQP pins are controlled by the current cycle and the OE signal.
4. CEN = 1 inserts wait states.
5. Device will power-up deselected and the I/Os in a three-state condition, regardless of OE.
6. OE assumed LOW.

Write Cycle Description[1, 2]

Function (CY7C1354B)	$\overline{WE}$	$\overline{BWS_d}$	$\overline{BWS_c}$	$\overline{BWS_b}$	$\overline{BWS_a}$
Read	1	X	X	X	X
Write – No bytes written	0	1	1	1	1
Write Byte 0 – (DQa and DQPa)	0	1	1	1	0
Write Byte 1 – (DQb and DQPb)	0	1	1	0	1
Write Bytes 1, 0	0	1	1	0	0
Write Byte 2 – (DQc and DQPc)	0	1	0	1	1
Write Bytes 2, 0	0	1	0	1	0
Write Bytes 2, 1	0	1	0	0	1
Write Bytes 2, 1, 0	0	1	0	0	0
Write Byte 3 – (DQd and DQPd)	0	0	1	1	1
Write Bytes 3, 0	0	0	1	1	0
Write Bytes 3, 1	0	0	1	0	1
Write Bytes 3, 1, 0	0	0	1	0	0
Write Bytes 3, 2	0	0	0	1	1
Write Bytes 3, 2, 0	0	0	0	1	0
Write Bytes 3, 2, 1	0	0	0	0	1
Write All Bytes	0	0	0	0	0

Function (CY7C1356B)	$\overline{WE}$	$\overline{BWS_b}$	$\overline{BWS_a}$
Read	1	x	x
Write – No Bytes Written	0	1	1
Write Byte 0 – (DQ_a and DQP_a)	0	1	0
Write Byte 1 – (DQ_b and DQP_b)	0	0	1
Write Both Bytes	0	0	0

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1354B/CY7C1356B incorporates a serial boundary scan Test Access Port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 3.3V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port–Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK. TDO is connected to the Least Significant Bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a xx-bit-long register, and the x18 configuration has a yy-bit-long register.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the Inputs and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant to the 1149.1 standard.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

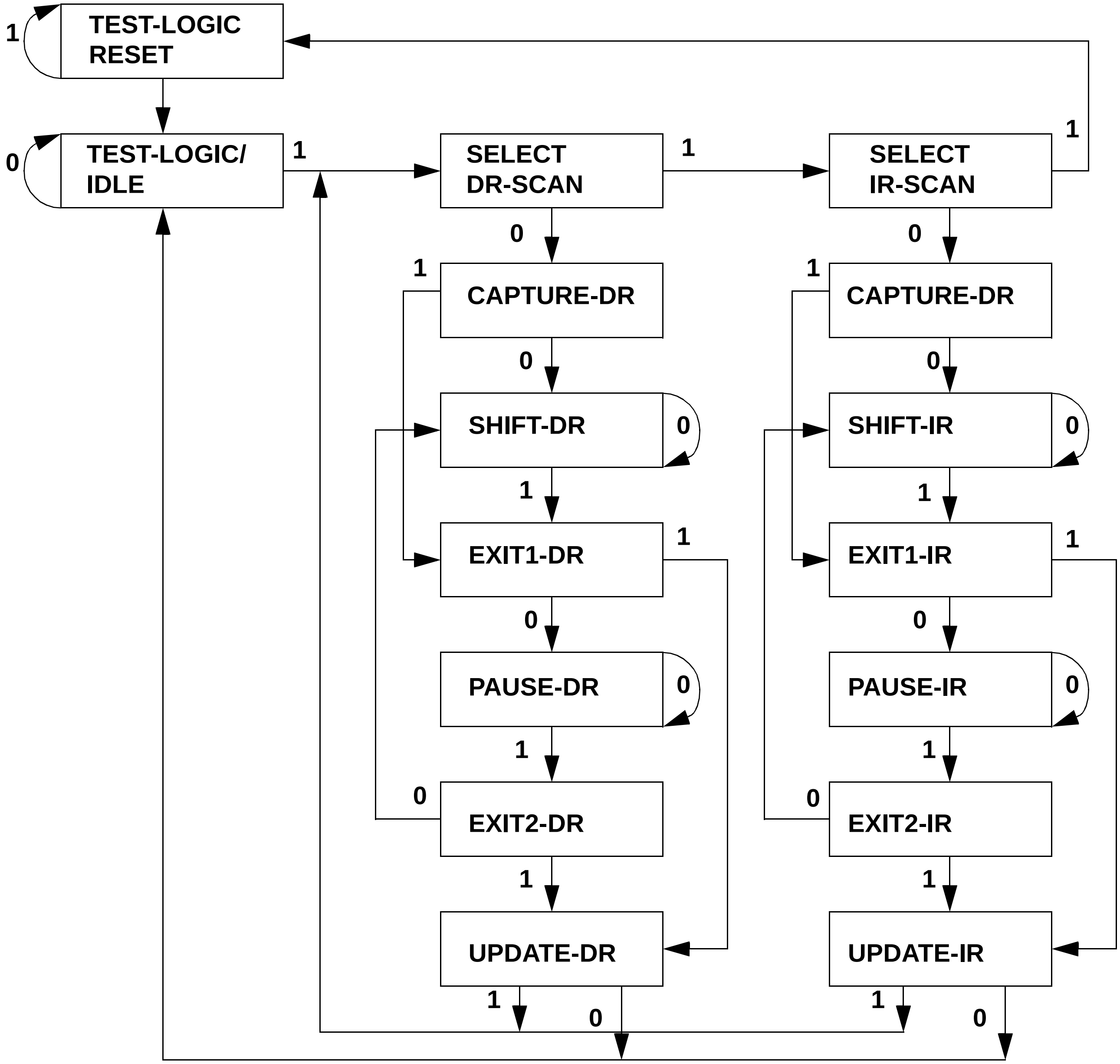
Bypass

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

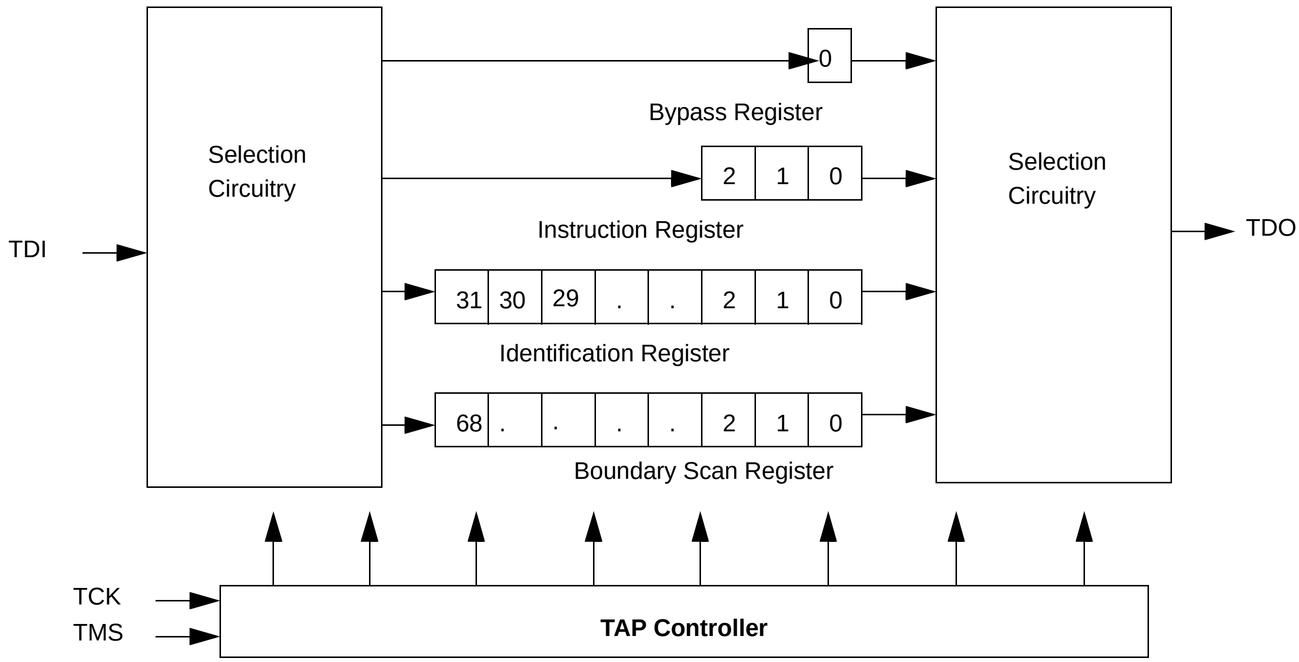
TAP Controller State Diagram[7]



Note:

7. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[8, 9]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{DDQ} = 3.3V	2.0		V
		I_{OH} = –2.0 mA, V_{DDQ} = 2.5V	1.7		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA, V_{DDQ} = 3.3V	2.0		V
		I_{OH} = –100 µA, V_{DDQ} = 2.5V	2.0		V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA		0.7	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}	–30	30	µA
I_X	Input Load Current TMS and TDI	GND ≤ V_I ≤ V_{DDQ}	–30	30	µA

TAP AC Switching Characteristics Over the Operating Range [10, 11]

Parameter	Description	Min.	Max.	Unit
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH	40		ns
t_{TL}	TCK Clock LOW	40		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{CS}	Capture Set-up to TCK Rise	10		ns

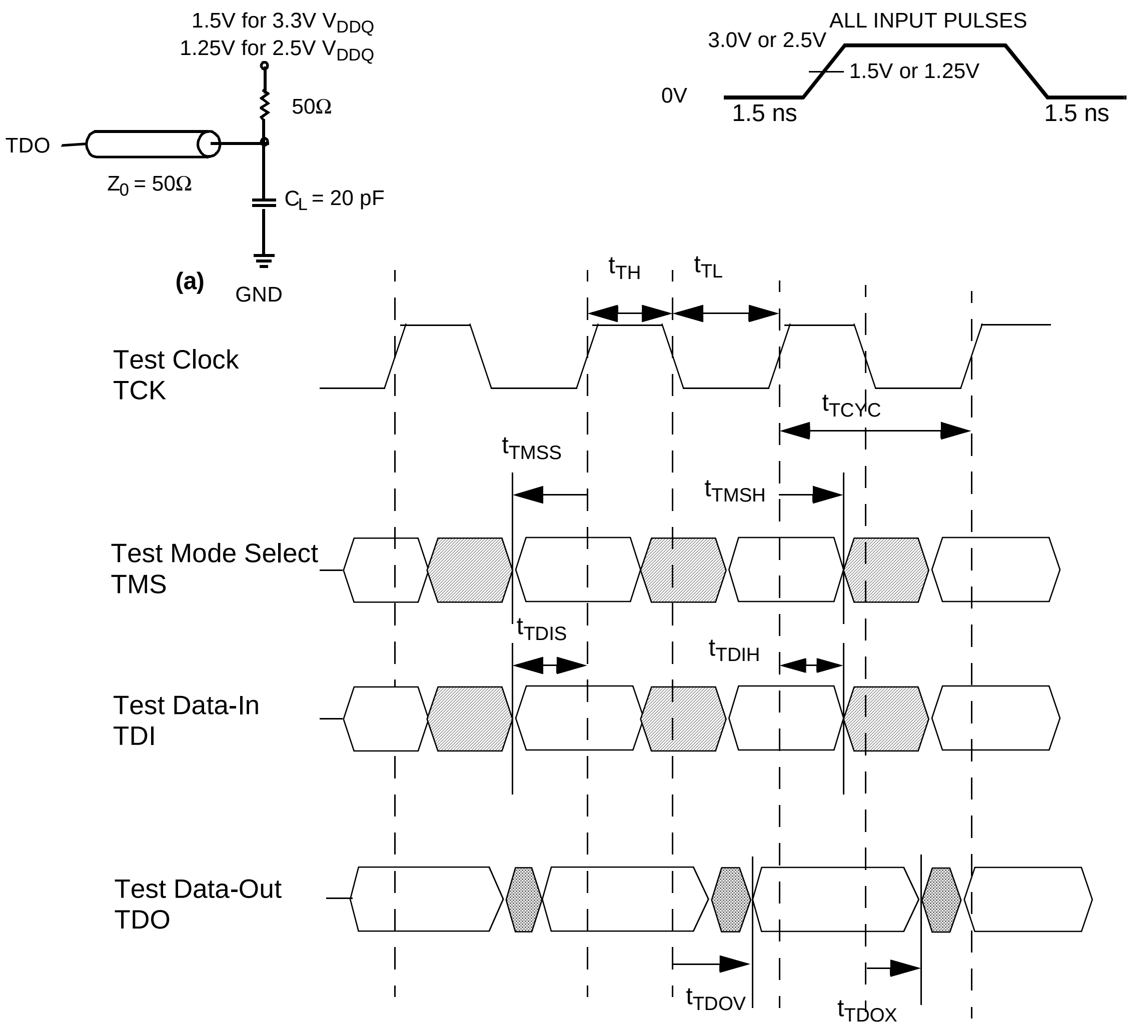
Notes:

8. All voltage referenced to ground.
9. Overshoot: $V_{IH}(AC) \leq V_{DD} + 1.5V$ for $t \leq t_{TCYC}/2$; undershoot: $V_{IL}(AC) \leq 0.5V$ for $t \leq t_{TCYC}/2$; power-up: $V_{IH} < 2.6V$ and $V_{DD} < 2.4V$ and $V_{DDQ} < 1.4V$ for $t < 200$ ms.
10. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

TAP AC Switching Characteristics Over the Operating Range (continued)[10, 11]

Parameter	Description	Min.	Max.	Unit
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after Clock Rise	10		ns
t_{CH}	Capture Hold after clock rise	10		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		20	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

TAP Timing and Test Conditions



Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	TBD	Reserved for version number.
Device Depth (27:23)	TBD	Defines depth of SRAM.
Device Width (22:18)	TBD	Defines width of the SRAM.
Cypress Device ID (17:12)	TBD	Reserved for future use.
Cypress JEDEC ID (11:1)	TBD	Allows unique identification of SRAM vendor.
ID Register Presence (0)	TBD	Indicate the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	69

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Exit Order (x36)

Bit #	Signal Name	119-Ball ID	165-Ball ID
1	TBD	TBD	TBD
2	TBD	TBD	TBD
3	TBD	TBD	TBD
4	TBD	TBD	TBD
5	TBD	TBD	TBD
6	TBD	TBD	TBD
7	TBD	TBD	TBD
8	TBD	TBD	TBD
9	TBD	TBD	TBD
10	TBD	TBD	TBD
11	TBD	TBD	TBD
12	TBD	TBD	TBD
13	TBD	TBD	TBD
14	TBD	TBD	TBD
15	TBD	TBD	TBD
16	TBD	TBD	TBD
17	TBD	TBD	TBD
18	TBD	TBD	TBD
19	TBD	TBD	TBD
20	TBD	TBD	TBD
21	TBD	TBD	TBD
22	TBD	TBD	TBD
23	TBD	TBD	TBD

Boundary Scan Exit Order (x36) (continued)

Bit #	Signal Name	119-Ball ID	165-Ball ID
24	TBD	TBD	TBD
25	TBD	TBD	TBD
26	TBD	TBD	TBD
27	TBD	TBD	TBD
28	TBD	TBD	TBD
29	TBD	TBD	TBD
30	TBD	TBD	TBD
31	TBD	TBD	TBD
32	TBD	TBD	TBD
33	TBD	TBD	TBD
34	TBD	TBD	TBD
35	TBD	TBD	TBD
36	TBD	TBD	TBD
37	TBD	TBD	TBD
38	TBD	TBD	TBD
39	TBD	TBD	TBD
40	TBD	TBD	TBD
41	TBD	TBD	TBD
42	TBD	TBD	TBD
43	TBD	TBD	TBD
44	TBD	TBD	TBD
45	TBD	TBD	TBD
46	TBD	TBD	TBD

Boundary Scan Exit Order (x36) (continued)

Bit #	Signal Name	119-Ball ID	165-Ball ID
47	TBD	TBD	TBD
48	TBD	TBD	TBD
49	TBD	TBD	TBD
50	TBD	TBD	TBD
51	TBD	TBD	TBD
52	TBD	TBD	TBD
53	TBD	TBD	TBD
54	TBD	TBD	TBD
55	TBD	TBD	TBD
56	TBD	TBD	TBD
57	TBD	TBD	TBD
58	TBD	TBD	TBD
59	TBD	TBD	TBD
60	TBD	TBD	TBD
61	TBD	TBD	TBD
62	TBD	TBD	TBD
63	TBD	TBD	TBD
64	TBD	TBD	TBD
65	TBD	TBD	TBD
66	TBD	TBD	TBD
67	TBD	TBD	TBD
68	TBD	TBD	TBD
69	TBD	TBD	TBD
70	TBD	TBD	TBD

Boundary Scan Exit Order (x18)

Bit #	Signal Name	119-Ball ID	165-Ball ID
1	TBD	TBD	TBD
2	TBD	TBD	TBD
3	TBD	TBD	TBD
4	TBD	TBD	TBD
5	TBD	TBD	TBD
6	TBD	TBD	TBD
7	TBD	TBD	TBD
8	TBD	TBD	TBD
9	TBD	TBD	TBD
10	TBD	TBD	TBD
11	TBD	TBD	TBD
12	TBD	TBD	TBD
13	TBD	TBD	TBD
14	TBD	TBD	TBD
15	TBD	TBD	TBD
16	TBD	TBD	TBD
17	TBD	TBD	TBD
18	TBD	TBD	TBD

Boundary Scan Exit Order (x18) (continued)

Bit #	Signal Name	119-Ball ID	165-Ball ID
19	TBD	TBD	TBD
20	TBD	TBD	TBD
21	TBD	TBD	TBD
22	TBD	TBD	TBD
23	TBD	TBD	TBD
24	TBD	TBD	TBD
25	TBD	TBD	TBD
26	TBD	TBD	TBD
27	TBD	TBD	TBD
28	TBD	TBD	TBD
29	TBD	TBD	TBD
30	TBD	TBD	TBD
31	TBD	TBD	TBD
32	TBD	TBD	TBD
33	TBD	TBD	TBD
34	TBD	TBD	TBD
35	TBD	TBD	TBD
36	TBD	TBD	TBD
37	TBD	TBD	TBD
38	TBD	TBD	TBD
39	TBD	TBD	TBD
40	TBD	TBD	TBD
41	TBD	TBD	TBD
42	TBD	TBD	TBD
43	TBD	TBD	TBD
44	TBD	TBD	TBD
45	TBD	TBD	TBD
46	TBD	TBD	TBD
47	TBD	TBD	TBD
48	TBD	TBD	TBD
49	TBD	TBD	TBD
50	TBD	TBD	TBD
51	TBD	TBD	TBD

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65×C to +150×C

Ambient Temperature with
Power Applied..–55×C to +125×C

Supply Voltage on V_{DD} Relative to GND........ –0.5V to +3.6V

DC to Outputs in High-Z State[13]........ –0.5V to V_{DDQ} + 0.5V

DC Input Voltage[13] .... –0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current... > 200 mA

Operating Range

Range	Ambient Temperature[12]	V_{DD}/V_{DDQ}
Commercial	0°C to +70°C	3.135 – 3.6V / 3.135 – 3.6V or 2.375 – 2.9V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage	I_{0H}=1.0 mA		3.135	3.465	V
V_{DDQ}	I/O Supply Voltage	V_{DDQ} = 3.3V		3.135	V_{DD}	V
		V_{DDQ} = 2.5V		2.375	2.9	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA, V_{DDQ} = 3.3V		2.4		V
		V_{DD} = Min., I_{OH} = –1.0 mA, V_{DDQ} = 2.5V		2.0		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OH} = 8.0 mA, V_{DDQ} = 3.3V			0.4	V
		V_{DD} = Min., I_{OH} = 1.0 mA, V_{DDQ} = 2.5V			0.4	V
V_{IH}	Input HIGH Voltage	V_{DDQ} = 3.3V		2.0	V_{DD} + 0.3V	V
		V_{DDQ} = 2.5V		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[13]	V_{DDQ} = 3.3V		–0.3	0.8	V
		V_{DDQ} = 2.5V		–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE			–30	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz		250	mA
			5-ns cycle, 200 MHz		220	mA
			6-ns cycle, 166 MHz		180	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz		250	mA
			5-ns cycle, 200 MHz		220	mA
			6-ns cycle, 166 MHz		180	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speed grades		30	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz		250	mA
			5-ns cycle, 200 MHz		220	mA
			6-ns cycle, 166 MHz		180	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speed grades		40	mA

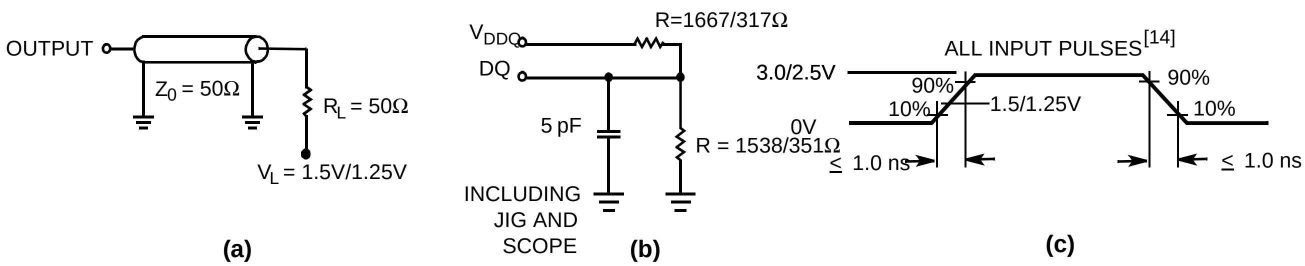
Notes:

12. T_A is the case temperature.
13. Minimum voltage equals –2.0V for pulse durations of less than 1 ns or -0.5V for 20 ns.

Capacitance[15]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V V_{DDQ} = 2.5V	4	pF
C_{CLK}	Clock Input Capacitance		4	pF
$C_{I/O}$	Input/Output Capacitance		4	pF

AC Test Loads and Waveforms



Thermal Resistance

Parameters	Description	Test Conditions	BGA Typ.	fBGA Typ.	TQFP Typ.	Unit	Notes
Q_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	25	27	25	°C/W	15
Q_{JC}	Thermal Resistance (Junction to Case)		6	6	9	°C/W	15

Switching Characteristics Over the Operating Range [16, 20]

Parameter	Description	-250		-200		-166		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock								
t_{CYC}	Clock Cycle Time	4.0		5		6		ns
F_{MAX}	Maximum Operating Frequency		250		200		166	MHz
t_{CH}	Clock HIGH	1.7		2.0		2.4		ns
t_{CL}	Clock LOW	1.7		2.0		2.4		ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise		2.6		3.0		3.5	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[15, 17, 19]		2.6		3.0		3.5	ns
t_{DOH}	Data Output Hold After CLK Rise	1.25		1.5		1.5		ns
t_{CHZ}	Clock to High-Z[15, 16, 17, 18, 19]	1.25	2.6	1.5	3.0	1.5	3.5	ns
t_{CLZ}	Clock to Low-Z[15, 16, 17, 18, 19]	1.25		1.5		1.5		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[16, 17, 19]		2.6		3.0		3.5	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[16, 17, 19]	0		0		0		ns
Set-up Times								
t_{AS}	Address Set-up Before CLK Rise	1.2		1.5		1.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.2		1.5		1.5		ns

Notes:

14. Input waveform should have a slew rate of ≥ 1 V/ns.
15. Tested initially and after any design or process change that may affect these parameters.
16. Unless otherwise noted, test conditions assume signal transition time of 1 ns or less, timing reference levels of 1.5V or 1.25V, input pulse levels of 0 to 3.0V or 2.5V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a), (b) and (c) of AC test loads.
17. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
18. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
19. This parameter is sampled and not 100% tested.
20. AC parameters may violate minimums and maximums during the first 20 microseconds of operation.

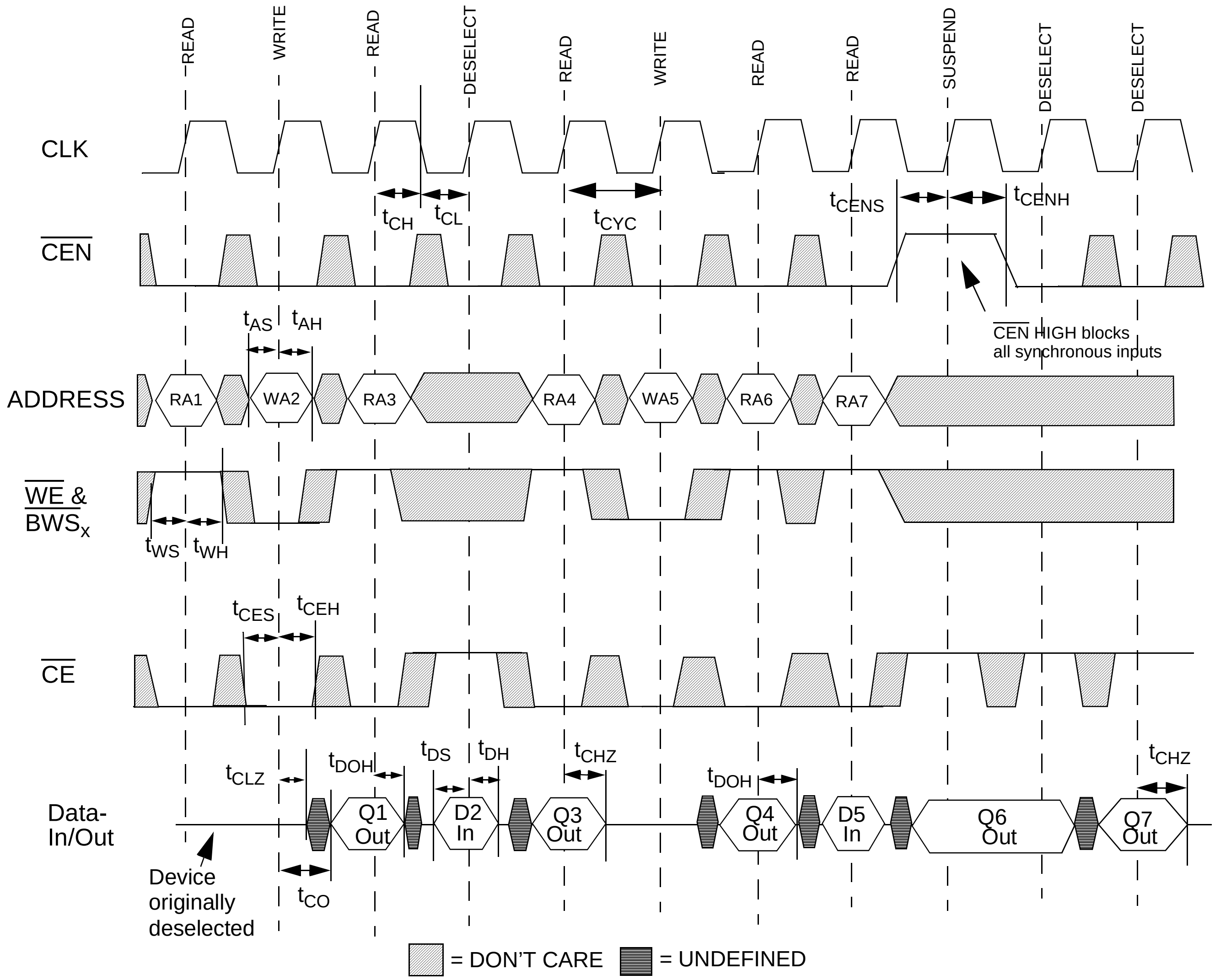
Switching Characteristics Over the Operating Range (continued)[16, 20]

Parameter	Description	-250		-200		-166		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CENS}	CEN Set-up Before CLK Rise	1.2		1.5		1.5		ns
t_{WES}	WE, BWS_X Set-up Before CLK Rise	1.2		1.5		1.5		ns
t_{ALS}	ADV/LD Set-up Before CLK Rise	1.2		1.5		1.5		ns
t_{CES}	Chip Select Set-up	1.2		1.5		1.5		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.3		0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.3		0.5		0.5		ns
t_{CENH}	CEN Hold After CLK Rise	0.3		0.5		0.5		ns
t_{WEH}	WE, BW_X Hold After CLK Rise	0.3		0.5		0.5		ns
t_{ALH}	ADV/LD Hold after CLK Rise	0.3		0.5		0.5		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.3		0.5		0.5		ns

Shaded areas contain advance information.

Switching Waveforms

READ/WRITE/DESELECT Sequence[21]

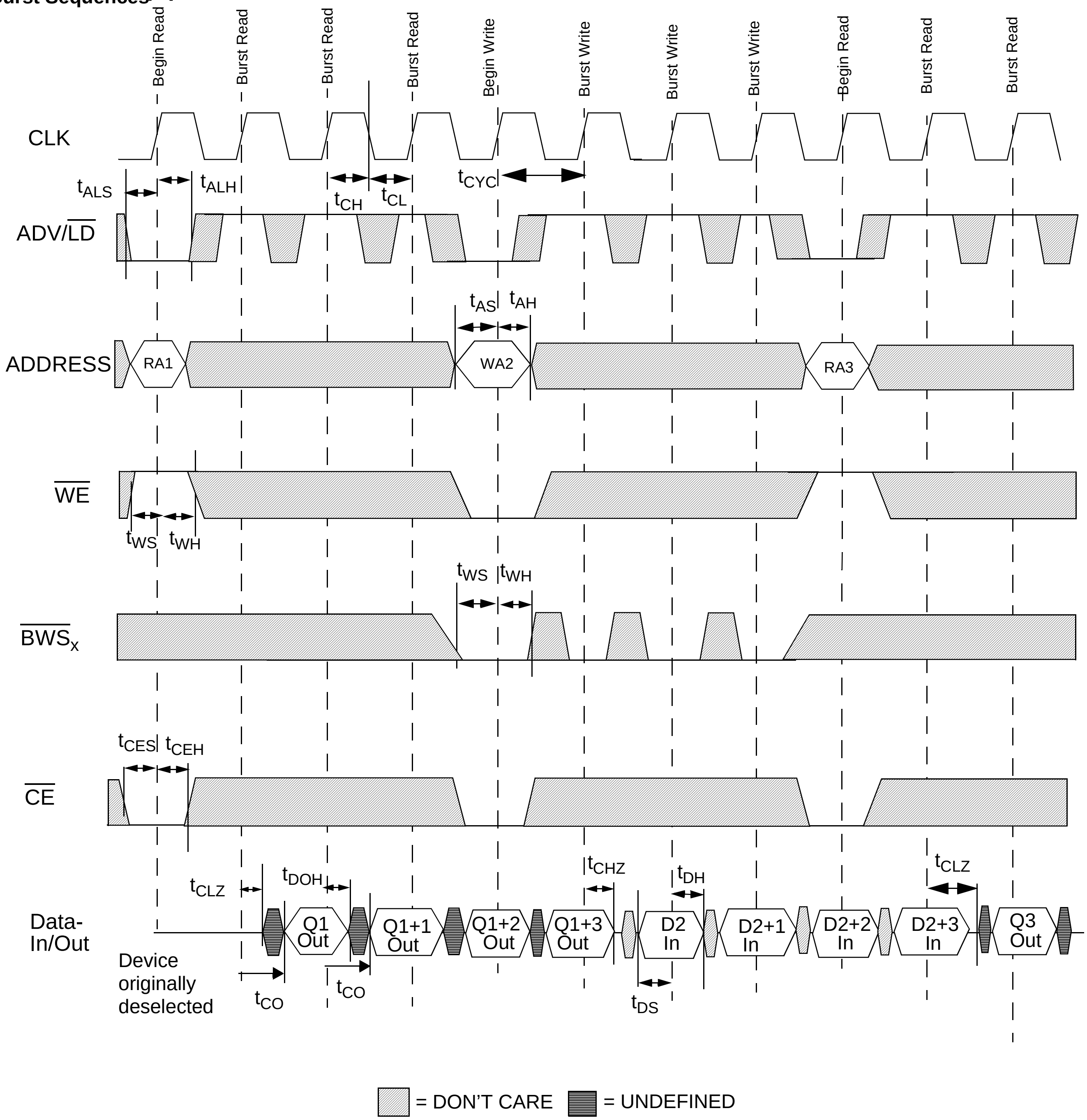


Note:

21. The combination of $\overline{WE}$ and $\overline{BWS_x}$ (x = a, b, c, d for CY7C1354B and x = a, b for CY7C1356B) define a write cycle (see Write Cycle Description table) $\overline{CE}$ is the combination of $\overline{CE_1}$, CE_2, and $\overline{CE_3}$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WAx Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. ADV/$\overline{LD}$ held LOW. $\overline{OE}$ held LOW.

Switching Waveforms (continued)

Burst Sequences[22]

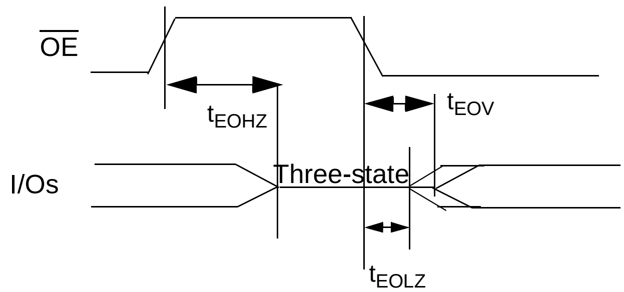


Note:

22. The combination of $\overline{WE}$ and $\overline{BWS_x}$(x = a, b c, d) define a write cycle (see Write Cycle Description table). $\overline{CE}$ is the combination of $\overline{CE_1}$, CE_2, and $\overline{CE_3}$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BWS_x}$ input signals. Burst order determined by the state of the MODE input. $\overline{CEN}$ held LOW. $\overline{OE}$ held LOW.

Switching Waveforms (continued)

OE Timing



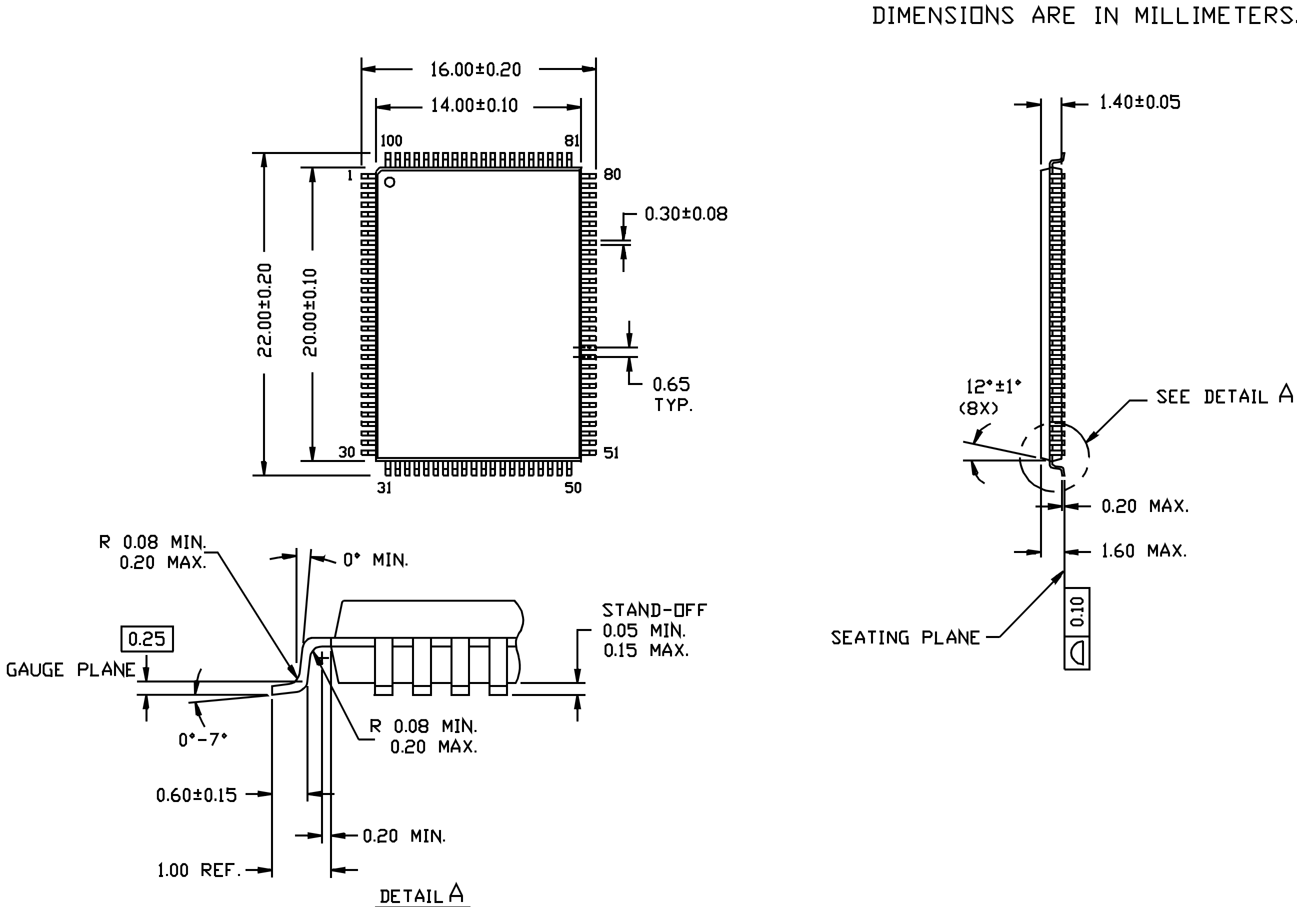
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CY7C1354B-250AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	Commercial
	CY7C1356B-250AC			
	CY7C1354B-250BGC	BG119	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1356B-250BGC			
	CY7C1354B-250BZC	BB165A	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.2 mm)	
	CY7C1356B-250BZC			
200	CY7C1354B-200AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	
	CY7C1356B-200AC			
	CY7C1354B-200BGC	BG119	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1356B-200BGC			
	CY7C1354B-200BZC	BB165A	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.2 mm)	
	CY7C1356B-200BZC			
166	CY7C1354B-166AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	
	CY7C1356B-166AC			
	CY7C1354B-166BGC	BG119	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1356B-166BGC			
	CY7C1354B-166BZC	BB165A	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.2 mm)	
	CY7C1356B-166BZC			

Shaded areas contain advance information.

Package Diagrams

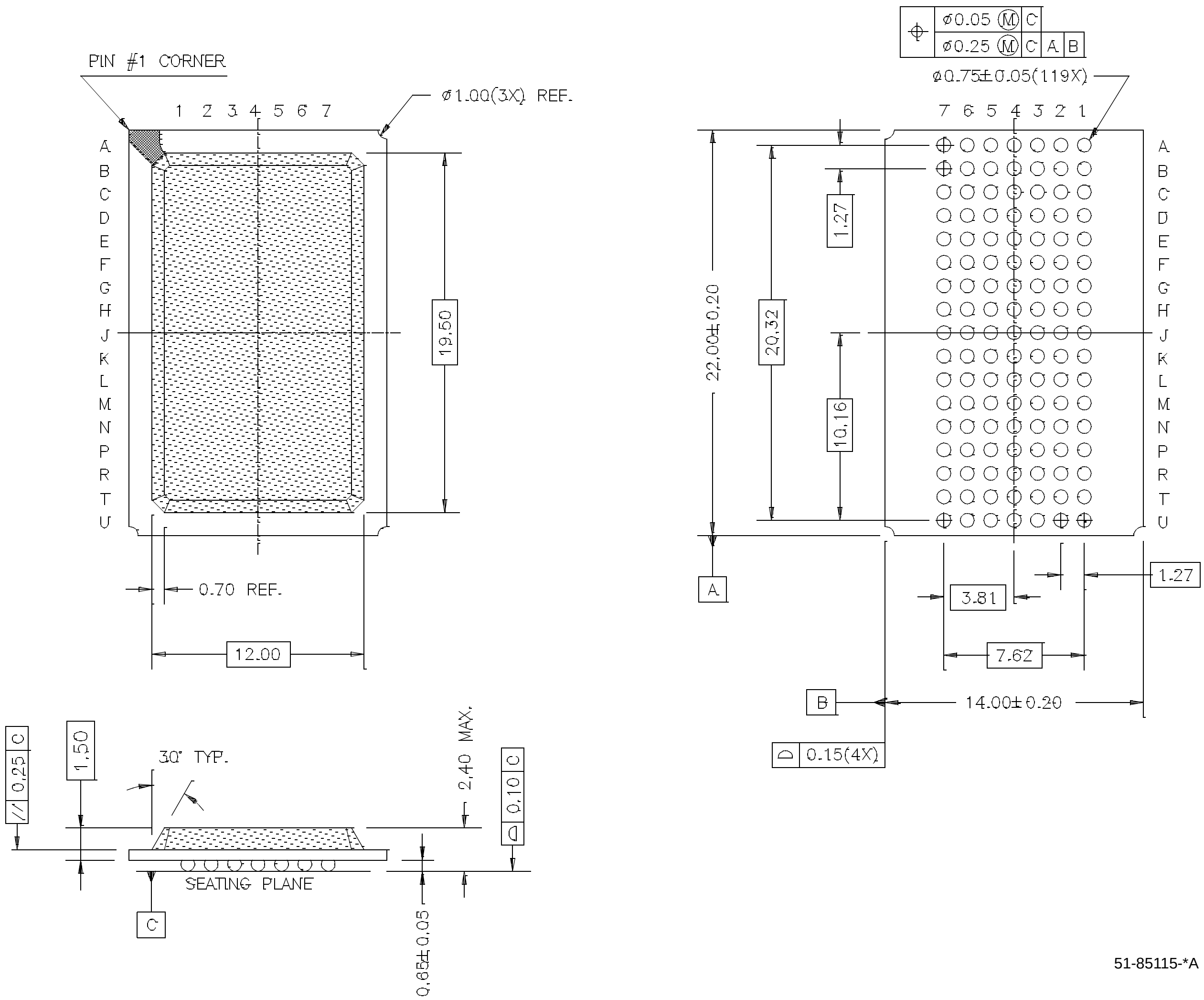
100-pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



51-85050-A

Package Diagrams (continued)

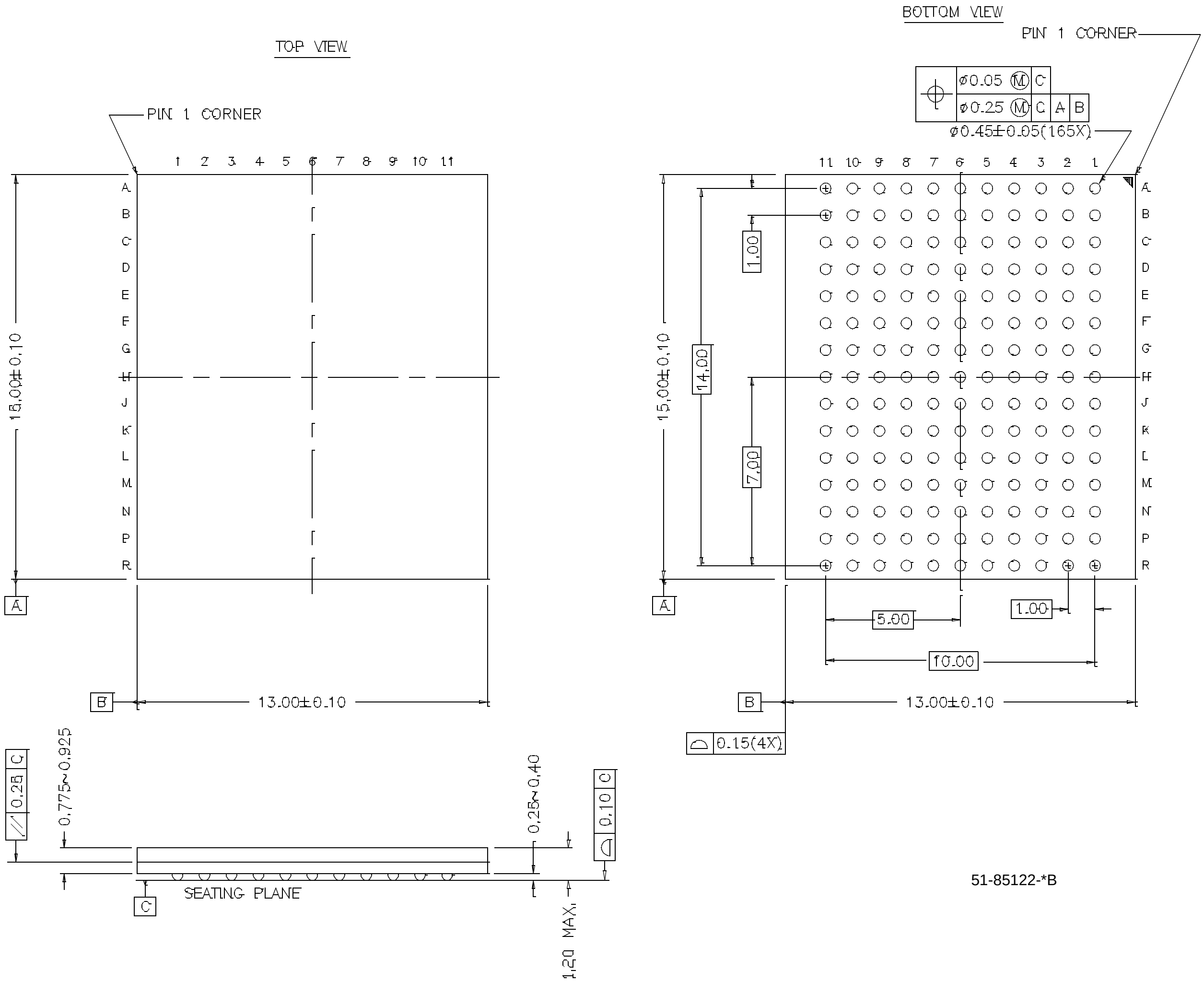
119-Lead BGA (14 x 22 x 2.4) BG119



51-85115-*A

Package Diagrams (continued)

165-ball FBGA (13 x 15 x 1.2 mm) BB165A



51-85122-*B

ZBT is a registered trademark of Integrated Device Technology. No Bus Latency and NoBL are trademarks of Cypress Semiconductor Corporation.

Document Title: CY7C1354B/CY7C1356B 256K x 36/512K x 18 Pipelined SRAM with NoBL™ Architecture Document Number: 38-05114				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	117904	08/28/02	RCS	New Data Sheet