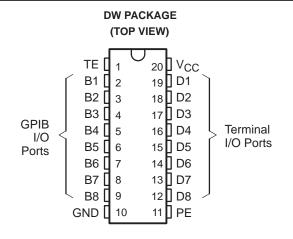
SLLS021E - JUNE 1986 - REVISED MAY 1998

- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch Free)



description

NOT RECOMMENDED FOR NEW DESIGNS

The SN75ALS163 octal general-purpose interface bus transceiver is a monolithic, high-speed, advanced low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state mode. If talk enable (TE) is high, these outputs have the characteristics of open-collector outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and 400 mV minimum of hysteresis for increased noise immunity.

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when $V_{CC} = 0$.

The SN75ALS163 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Function Tables

EACH DRIVER

	INPUTS	OUTPUT	
D	TE	PE	В
Н	Н	Н	Н
L	Н	Χ	L
Н	X	L	Z
Х	L	X	Z

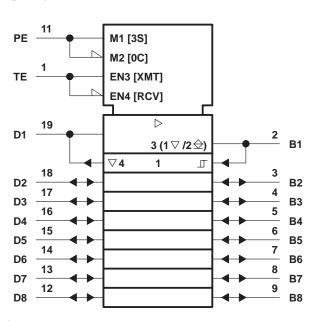
EACH RECEIVER

	INPUTS		OUTPUT
В	TE	PE	D
L	L	Χ	L
Н	L	X	Н
Х	Н	Χ	z

H = high level, L = low level,

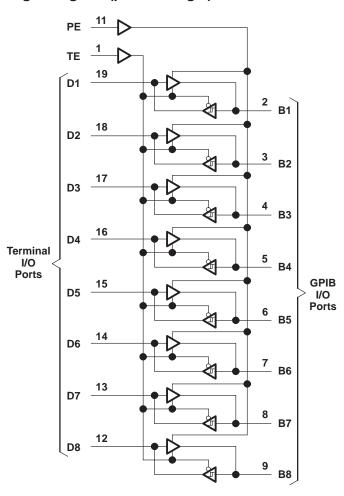
X = irrelevant, Z = high-impedance state

logic symbol†



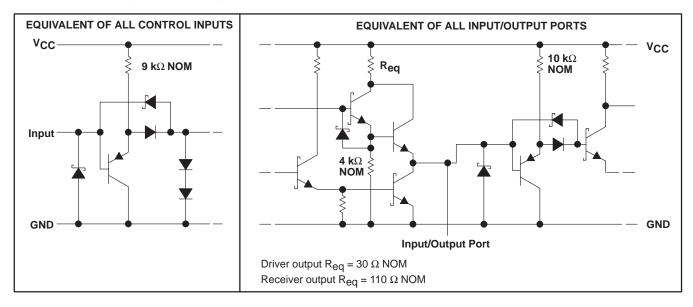
- [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- ∇ Designates 3-state outputs

logic diagram (positive logic)





schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage, V _I	5.5 V
Low-level driver output current	100 mA
Package thermal impedance, θ _{JA} (see Note 2)	97°C/W
Storage temperature range, T _{stq}	. − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

recommended operating conditions

		N	ΛIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4	.75	5	5.25	V	
High-level input voltage, VIH		2			V	
Low-level input voltage, V _{IL}					0.8	V
High-level output current, IOH	Bus ports with pullups active				- 5.2	mA
	Terminal ports				- 800	μΑ
Lauriana antanta antanta antanta de la composito de la composi	Bus ports				48	A
Low-level output current, IOL	Terminal ports				16	mA
Operating free-air temperature, T _A					70	°C

^{2.} The package thermal impedance is calculated in accordance with JESD 51.

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electrical characteristics over recommended supply-voltage and operating free-air temperature ranges (unless otherwise noted)

	PARAMETER		TE	EST CONDITIONS	MIN	TYP [†]	MAX	UNIT	
VIK	Input clamp voltage		I _I = -18 mA			- 0.8	-1.5	V	
V _{hys}	Hysteresis (V _{T+} – V _T)	Bus			0.4	0.65		V	
\/a	High level autout valence	Terminal	$I_{OH} = -800 \mu A$,	TE at 0.8 V	2.7	3.5		V	
VOH	High-level output voltage	Bus	$I_{OH} = -5.2 \text{ mA},$	PE and TE at 2 V	2.5	3.3		v	
\/o.	Low lovel output voltage	Terminal	$I_{OL} = 16 \text{ mA},$	TE at 0.8 V		0.3	0.5	V	
VOL	Low-level output voltage	Bus	$I_{OL} = 48 \text{ mA},$	TE at 2 V		0.35	0.5	V	
IOH	High-level output current (open-collector mode)	Bus	V _O = 5.5 V,	PE at 0.8 V, D and TE at 2 V			100	μΑ	
1	Off-state output current		PE at 2 V,	V _O = 2.7 V			20	^	
loz	(3-state mode)	bus	TE at 0.8 V	V _O = 0.5 V			-100	μΑ	
Ц	Input current at maximum input voltage	Terminal	V _I = 5.5 V			0.2	100	μΑ	
lн	High-level input current	Terminal,	V _I = 2.7 V	V _I = 2.7 V			20	μΑ	
Iμ	Low-level input current	PE, or TE	V _I = 0.5 V			-10	-100	μΑ	
	Short-circuit output	Terminal			- 15	- 35	- 7 5	mA	
los	current	Bus			- 25	- 50	-125	IIIA	
Icc	Supply current		No load	Terminal outputs low and enabled		42	65	mA	
				Bus outputs low and enabled		52	80		
C _{I/O(bus)}	Bus-port capacitance		$V_{CC} = 0 \text{ to } 5 \text{ V},$	$V_{I/O} = 0 \text{ to } 2 \text{ V}, \qquad f = 1 \text{ MHz}$		30		pF	

 $[\]overline{\dagger}$ All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.

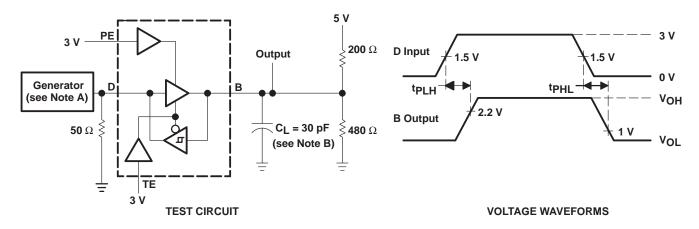
switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $\rm V_{CC}$ = 5 $\rm V$

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN TYPT	MAX	UNIT		
^t PLH	Propagation delay time, low-to-high-level output	Torminal	rminal Bus	C _L = 30 pF, See Figure 1	7	20	ns		
tPHL	Propagation delay time, high-to-low-level output	Temma			8	20			
^t PLH	Propagation delay time, low-to-high-level output	Puo	Torminal	C _L = 30 pF,	7	14			
tPHL	Propagation delay time, high-to-low-level output	Bus Terminal		See Figure 2	9	14	ns		
^t PZH	Output enable time to high level				19	30			
^t PHZ	Output disable time from high level	TE	Bus	C _L = 15 pF,	5	12	20		
tPZL	Output enable time to low level] '-	Bus	See Figure 3	16	35	ns		
tPLZ	Output disable time from low level				9	20			
^t PZH	Output enable time to high level				13	30			
^t PHZ	Output disable time from high level	TE	Terminal	C _L = 15 pF,	12	20			
tPZL	Output enable time to low level	'E	'E	15	Terrilliai	See Figure 4	12	20	ns
tPLZ	Output disable time from low level				11	20			
t _{en}	Output pull-up enable time	PE	Bus	C _L = 15 pF,	11	22	20		
tdis	Output pull-up disable time		Bus	See Figure 5	6	12	ns		

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

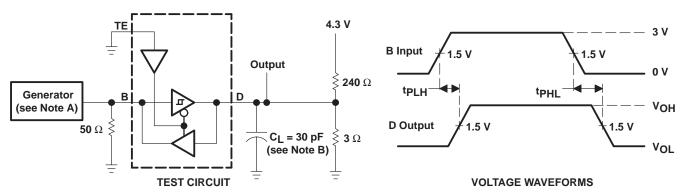


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{\Gamma} \leq$ 6 ns, $t_{\Gamma} \leq$ 7 ns, $t_{\Gamma} \leq$ 8 ns, $t_{\Gamma} \leq$ 8 ns, $t_{\Gamma} \leq$ 9 ns, $t_$
 - B. C_L includes probe and jig capacitance.

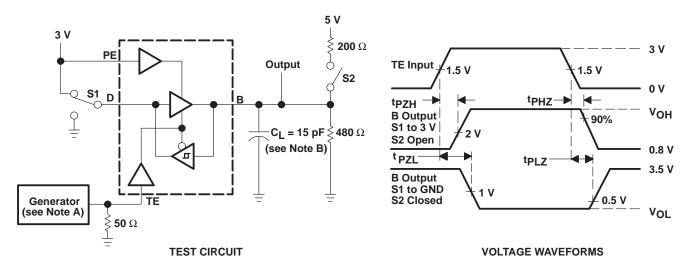
Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, t_f
 - B. C_L includes probe and jig capacitance.

Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

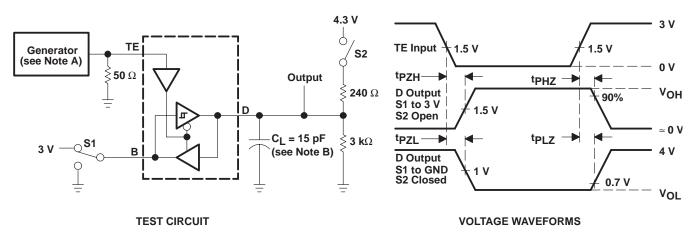
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 7 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, t_f

B. CL includes probe and jig capacitance.

Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{\Gamma} \leq$ 6 ns, $t_{Q} = 50 \Omega$.

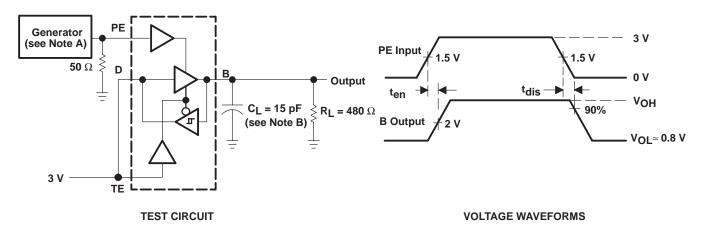
B. C_I includes probe and jig capacitance.

Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms



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PARAMETER MEASUREMENT INFORMATION



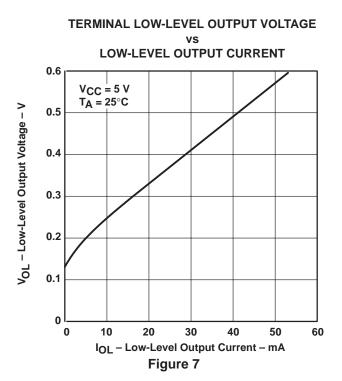
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50~\Omega$.

B. C_L includes probe and jig capacitance.

Figure 5. PE-to-Bus Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE HIGH-LEVEL OUTPUT CURRENT $V_{CC} = 5$ V T_A = 25°C 3.5 V_{OH} - High-Level Output Voltage - V 3 2.5 2 1.5 1 0.5 0 0 -10 -15 -20 -25 -30 -35 -40 IOH - High-Level Output Current - mA Figure 6



TERMINAL OUTPUT VOLTAGE

VS BUS INPUT VOLTAGE

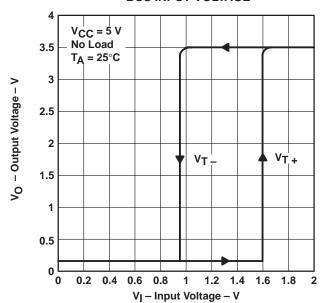
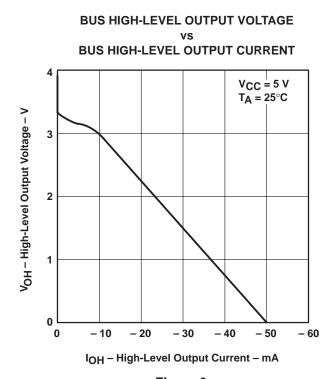


Figure 8

TYPICAL CHARACTERISTICS



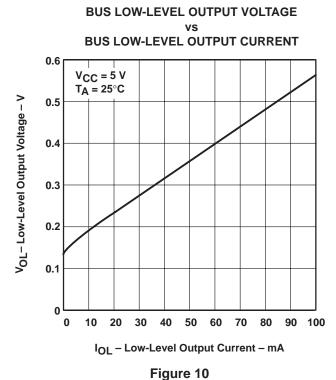
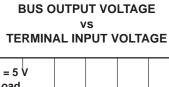


Figure 9



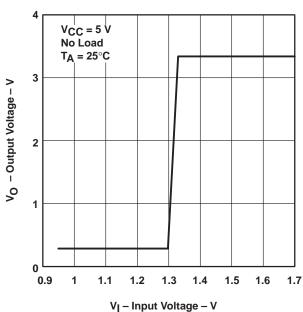


Figure 11



PACKAGE OPTION ADDENDUM

31-Oct-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing	Qty	(2)	(6)	(3)		(4/5)	
SN75ALS163N	OBSOLETE	PDIP	N	20	TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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