TC74LVQ573F/FW/FS

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74LVQ573 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
This 8bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.
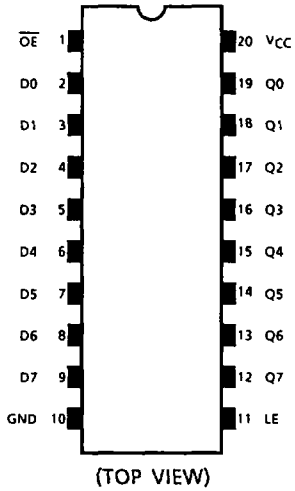
FEATURES

- High speed : $t_{pd} = 5.7ns$ (Typ.) ($V_{CC} = 3.3V$)

- Low power dissipation : $I_{CC} = 4\mu A$ (Max.) (Ta = 25°C)

- Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$)
  $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)

- symmetrical output impedance
  : $|I_{OH}| = I_{OL} = 12mA$ (Min.)

- Balanced propagation delays
  : $t_{pLH} \simeq t_{pHL}$

- Pin and function compatible with 74HC573

TC74LVQ573F

SOP20-P-300

TC74LVQ573FW

SOL20-P-300

TC74LVQ573FS
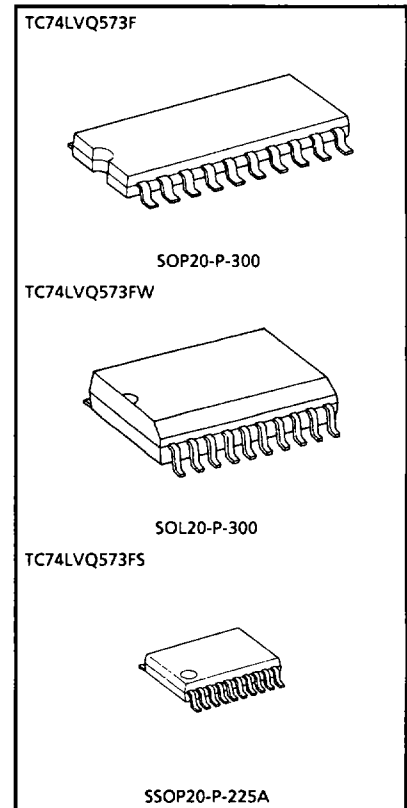
SSOP20-P-225A

Weight SOP20-P-300 : 0.22g (Typ.)
SOL20-P-300 : 0.46g (Typ.)
SSOP20-P-225A : 0.09g (Typ.)

PIN ASSIGNMENT

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        ┌───┐
 OE  1 │   │ 20  VCC
 D0  2 │   │ 19  Q0
 D1  3 │   │ 18  Q1
 D2  4 │   │ 17  Q2
 D3  5 │   │ 16  Q3
 D4  6 │   │ 15  Q4
 D5  7 │   │ 14  Q5
 D6  8 │   │ 13  Q6
 D7  9 │   │ 12  Q7
GND 10 │   │ 11  LE
        └───┘
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(TOP VIEW)

TRUTH TABLE

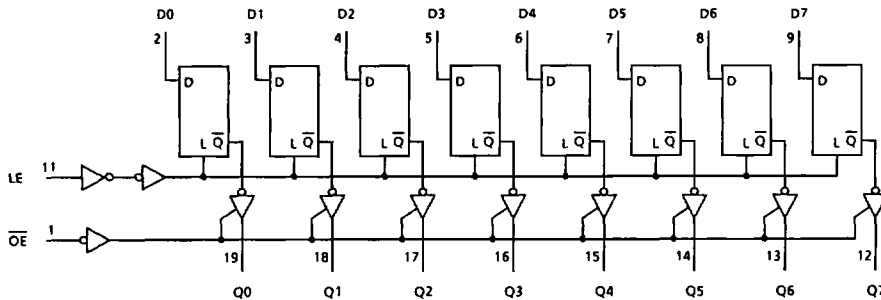| INPUTS			OUTPUTS
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care

Z : High Impedance

Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL
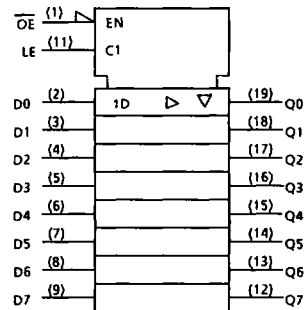
SYSTEM DIAGRAM

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} / Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10s	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 3.6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise And Fall Time	dt / dv	$0 \sim 100$	ns / V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYM-BOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = $-40 \sim 85$°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	"H" Level	V_{IH}			3.0	2.0	—	—	2.0	—	V
	"L" Level	V_{IL}			3.0	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	3.0	2.9	3.0	—	2.9	—	V
				$I_{OH} = -12mA$	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu A$	3.0	—	0.0	0.1	—	0.1	
				$I_{OL} = 12mA$	3.0	—	—	0.36	—	0.44	
3-state Output Off-state Current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		3.6	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current		I_{IN}	$V_{IN} = V_{CC}$ or GND		3.6	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current		I_{CC}	$V_{IN} = V_{CC}$ or GND		3.6	—	—	4.0	—	40.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (LE)	t_W (H)		2.7	9.0	10.0	ns
			3.3 ± 0.3	7.0	7.0	
Minimum Set-up Time	t_s		2.7	9.0	10.0	ns
			3.3 ± 0.3	7.0	7.0	
Minimum Hold Time	t_h		2.7	1.0	1.0	ns
			3.3 ± 0.3	1.0	1.0	

AC characteristics (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C MIN.	TYP.	MAX.	Ta = −40~85°C MIN.	MAX.	UNIT
Propagation Delay Time (LE-Q)	t_{pLH} t_{pHL}		2.7	—	7.9	16.9	1.0	19.0	ns
			3.3 ± 0.3	—	6.6	12.0	1.0	13.5	
Propagation Delay Time (D-Q)	t_{pLH} t_{pHL}		2.7	—	7.7	14.8	1.0	17.0	ns
			3.3 ± 0.3	—	6.4	10.5	1.0	12.0	
Output Enable Time	t_{pZL} t_{pZH}		2.7	—	8.5	18.3	1.0	19.0	ns
			3.3 ± 0.3	—	7.1	13.0	1.0	13.5	
Output Disable Time	t_{pLZ} t_{pHZ}		2.7	—	8.0	20.4	1.0	22.0	ns
			3.3 ± 0.3	—	6.7	14.5	1.0	15.0	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)	—	5	10	—	10		pF
Output Capacitance	C_{OUT}		—	10	—	—	—		pF
Power Dissipation Capacitance	C_{PD}	(Note 3)	—	32	—	—	—		pF

(Note 1) Parameter guaranteed by design.

$(t_{osLH} = |t_{pLHm} - t_{pLHn}|,\ t_{osHL} = |t_{pHLm} - t_{pHLn}|)$

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

I_{CC} (opr.) $= C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Latch)

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

C_{PD} (total) $= 21 + 11 \cdot n$

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.7	1.1	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	− 0.7	− 1.1	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V