TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (II-MOS VII)

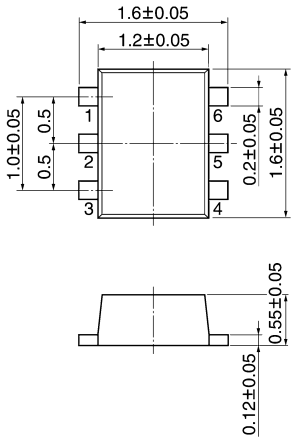
SSM6K30FE

○ High-speed switching

○ DC-DC Converter

- Small package
- Low $R_{DS\ (ON)}$: $R_{DS(ON)}$ = 210 mΩ (max) (@V_{GS} = 10 V)
  : $R_{DS(ON)}$ = 420 mΩ (max) (@V_{GS} = 4 V)
- High-speed switching: t_{on} = 19 ns (typ.)
  : t_{off} = 10 ns (typ.)

Unit: mm



1,2,5,6: Drain
3: Gate
4: Source

ES6

JEDEC	—
JEITA	—
TOSHIBA	2-2N1J

Weight: 3 mg (typ.)

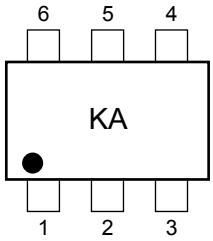
Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	20	V
Gate-Source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	1.2	A
	Pulse	I_{DP}	2.4	
Drain power dissipation		P_D (Note 1)	500	mW
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	−55 to 150	°C

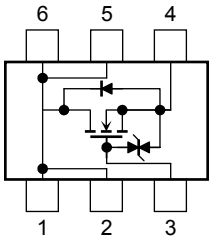
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm (t), Cu pad: 645 mm^2)

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

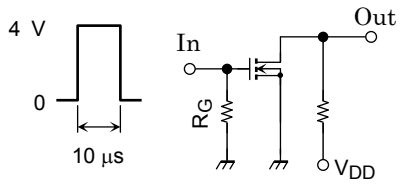
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0 V	20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 5 V, I_D = 0.1 mA	1.1	—	2.3	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 5 V, I_D = 0.6 A (Note 2)	0.68	—	—	S
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = 0.6 A, V_{GS} = 10 V (Note 2)	—	145	210	mΩ
			I_D = 0.6 A, V_{GS} = 4 V (Note 2)	—	260	420	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	60	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	17	—	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	47	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 0.6 A,	—	19	—	ns
	Turn-off time	t_{off}	V_{GS} = 0 to 4 V, R_G = 10 Ω	—	10	—	

Note 2: Pulse measurement

Switching Time Test Circuit

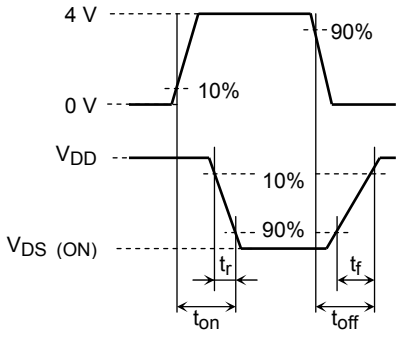
(a) Test circuit



V_{DD} = 10 V
R_G = 10 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}

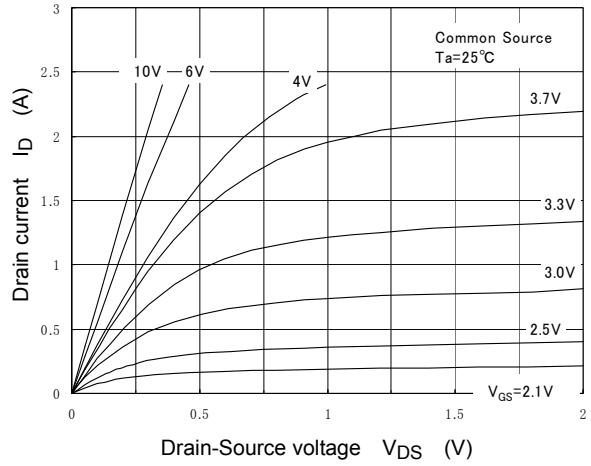


Precaution

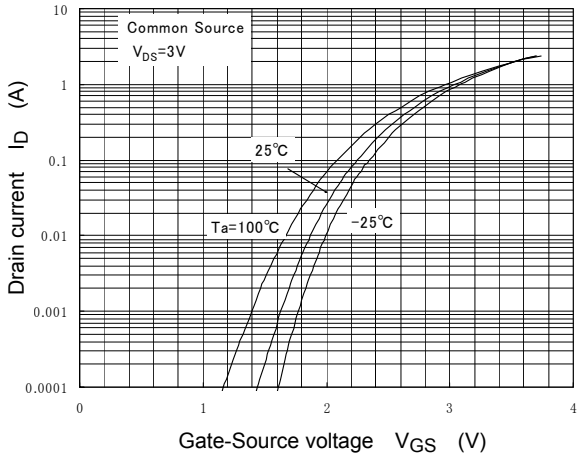
V_{th} can be expressed as the voltage between the gate and source when the low operating current value is I_D = 0.1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

Be sure to take this into consideration when using the device.

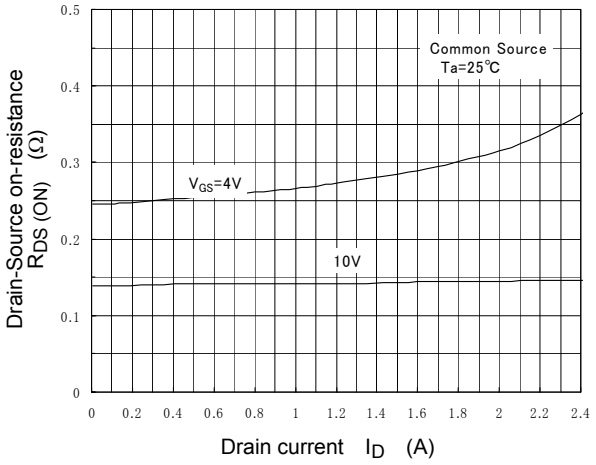
$I_D - V_{DS}$



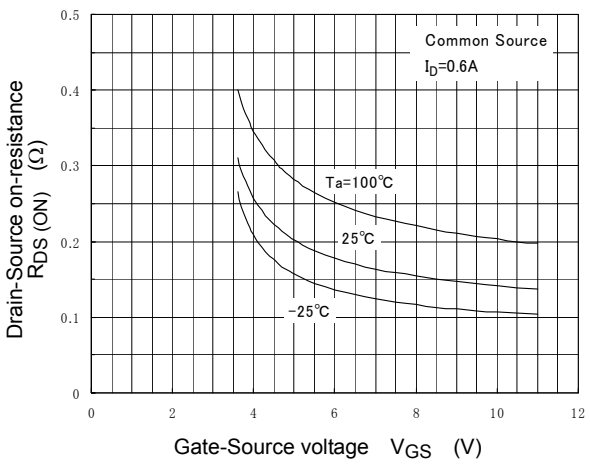
$I_D - V_{GS}$



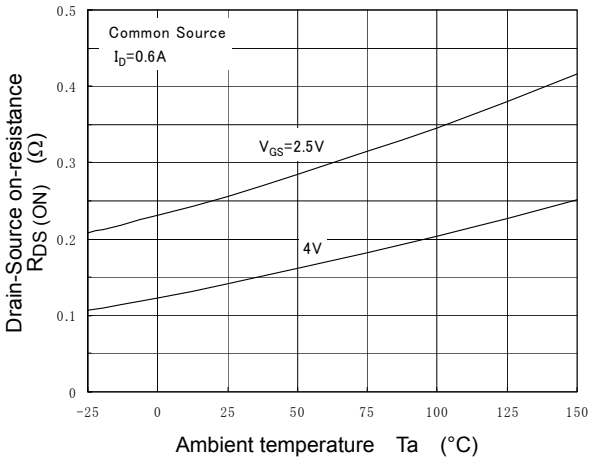
$R_{DS(ON)} - I_D$



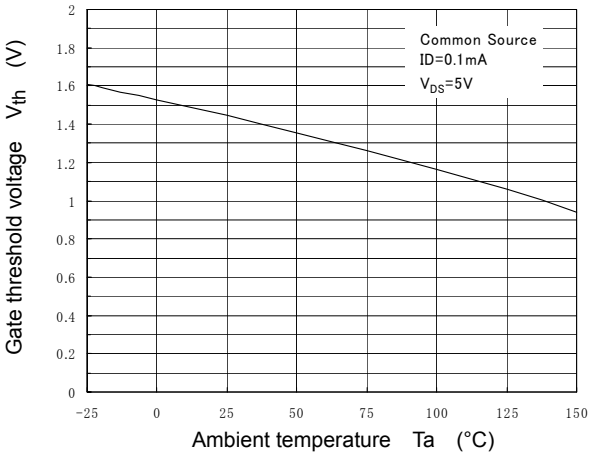
$R_{DS(ON)} - V_{GS}$



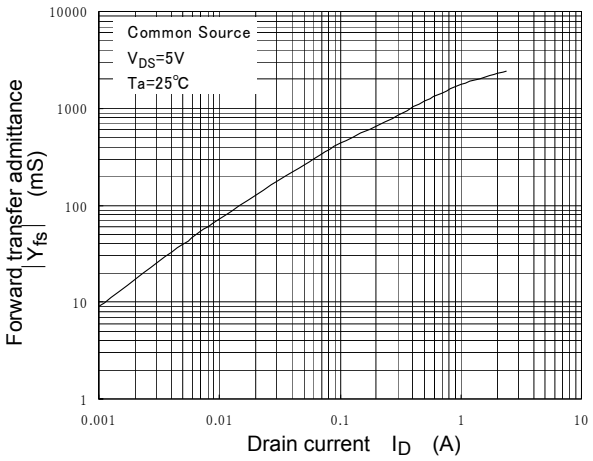
$R_{DS(ON)} - Ta$



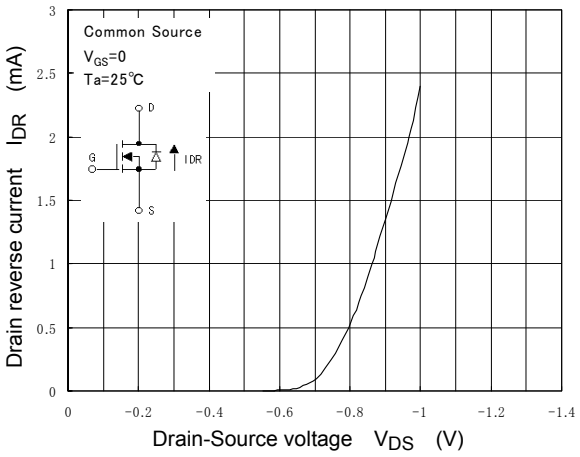
$V_{th} - Ta$



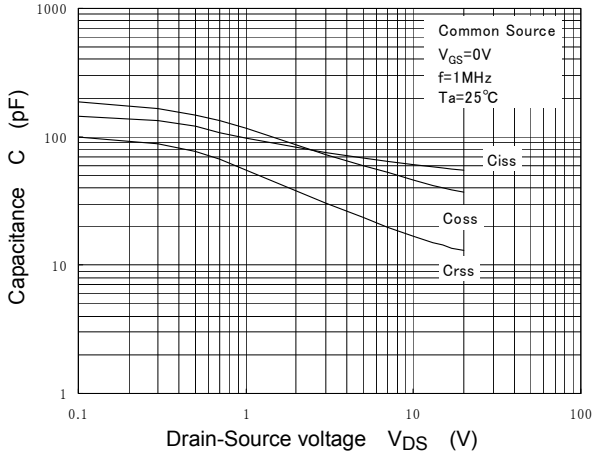
$|Y_{fs}| - I_D$



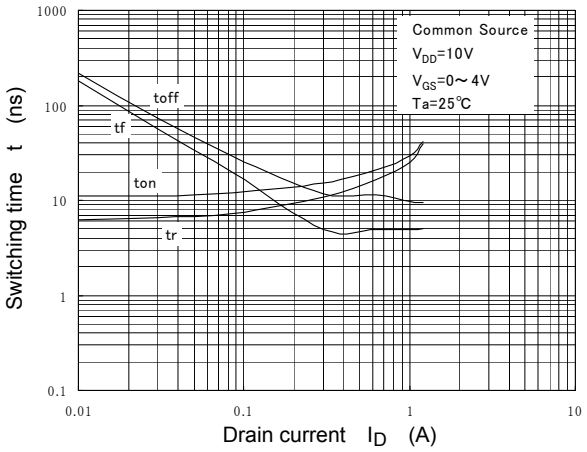
$I_{DR} - V_{DS}$



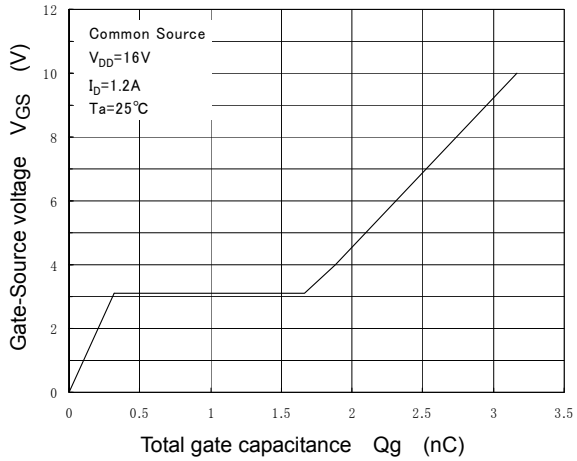
$C - V_{DS}$



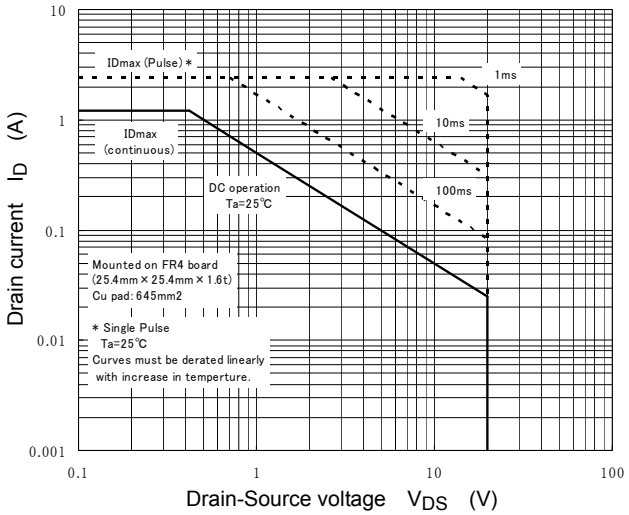
$t - I_D$



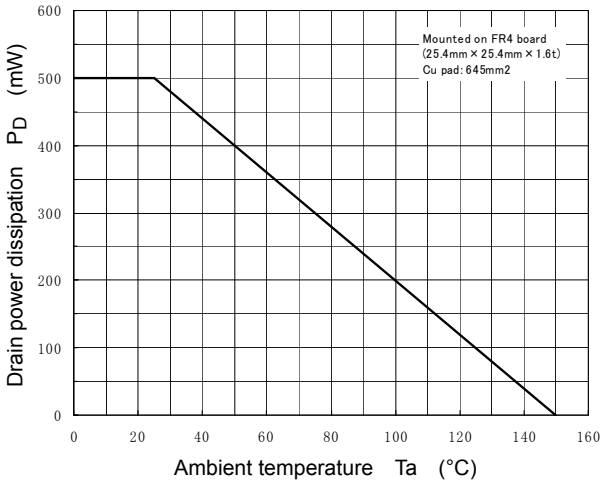
Dynamic Input Characteristics



Safe operating area



P_D – Ta



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