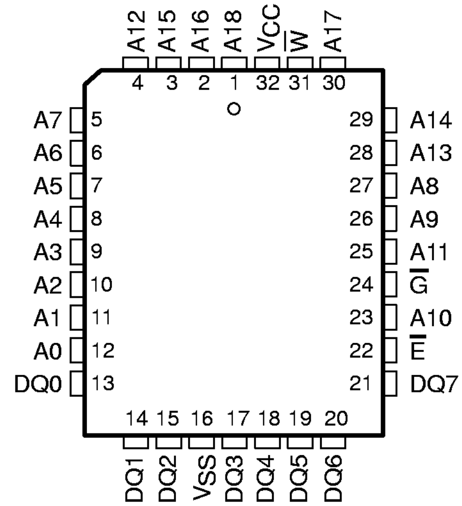
- **Single Power Supply**
  3.3 V ± 0.3 V – ’29LF040
  2.7 V to 3.6 V – ’29VF040
  5 V ± 10 % – See ’29F040 Data Sheet
- **Organization . . . 512K × 8**
- **Eight Equal Sectors of 64K Bytes**
  - **Any Combination of Sectors Can Be Erased**
  - **Any Combination of Sectors Can Be Marked as Read-Only**
- **Compatible With JEDEC EEPROM Command Set**
- **Fully Automated On-Chip Erase and Byte-Program Operations**
- **100000 Program/Erase Cycles**
- **Suspend-Erase/Resume-Erase Operation**
- **Compatible With JEDEC Byte-Wide Pinouts**
- **Low-Power Dissipation**
  - **Active Read . . . 20 mA Typical**
  - **Active PGM/Erase . . . 30 mA Typical**
  - **Standby . . . 25 µA Typical**
- **All Inputs/Outputs TTL Compatible**

FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A18	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	3.3-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

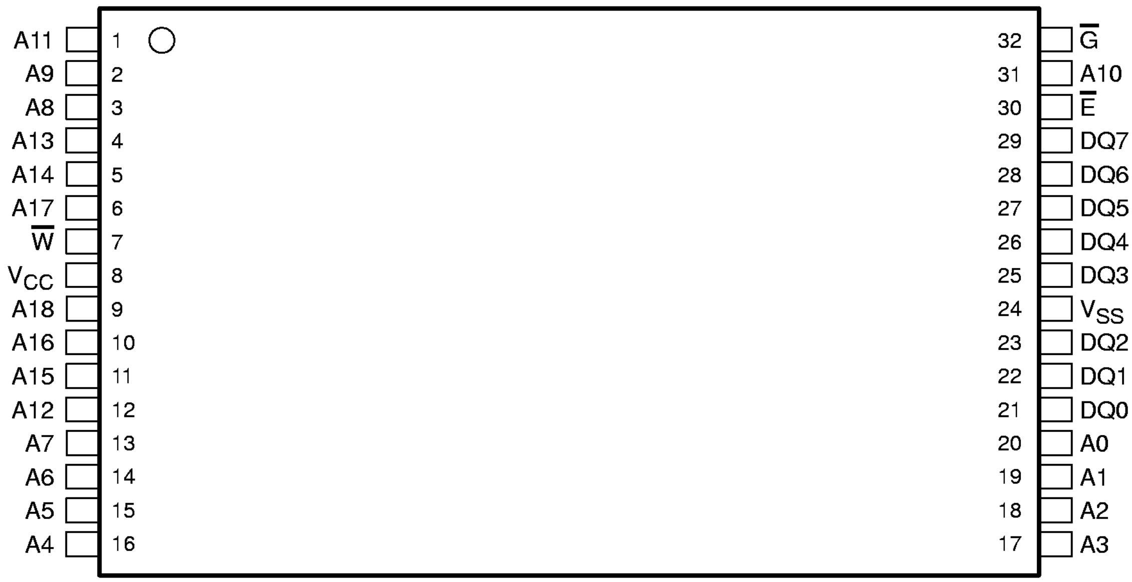
The TMS29LF040 and TMS29VF040 are 4194304-bit, low-voltage single-supply, programmable read-only memories that can be erased electrically and reprogrammed. These devices are organized as eight independent 64K-byte blocks and are offered with access times between 60 ns and 200 ns.

An on-chip state machine controls the program and erase operations. The embedded byte program and sector/chip-erase functions are fully automatic. The command set is compatible with that of JEDEC 4M-bit EEPROMs. A suspend/resume feature allows access to unaltered memory blocks during a sector-erase operation. Data protection of any sector combination is accomplished using a hardware sector-protection feature.

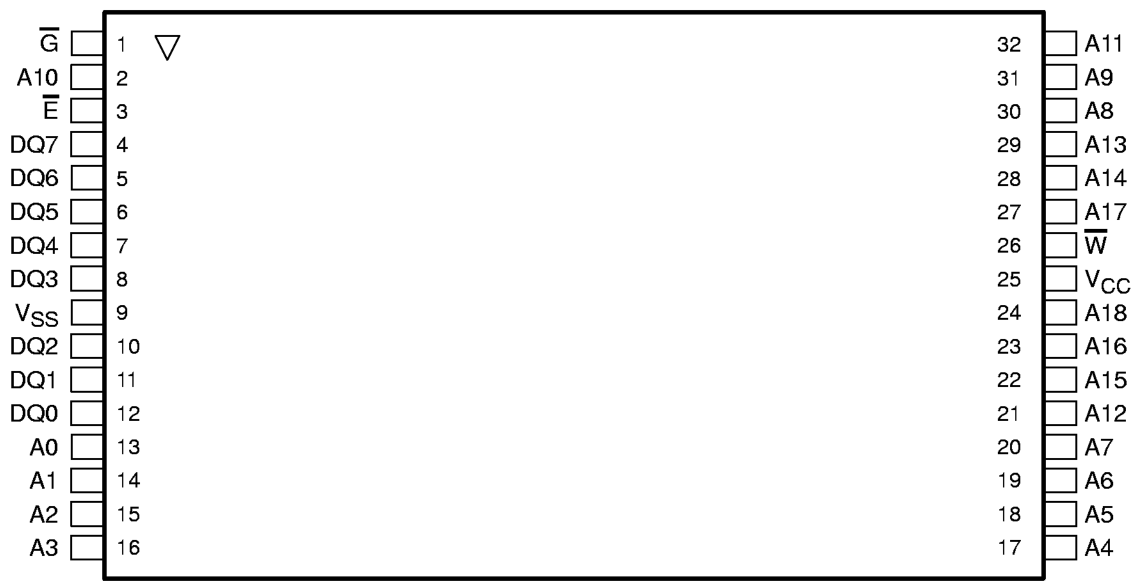
Device operations are selected by writing JEDEC-standard commands into the command register using standard microprocessor write timings. The command register acts as input to an internal state machine that interprets the commands, controls the erase and programming operations, outputs the status of the device, outputs data stored in the device, and outputs the device algorithm-selection code. On initial power-up operation, the device defaults to the read mode.

The TMS29xF040 is offered in a 32-pin plastic leaded chip carrier (FM suffix) using 1.25 mm (50-mil) lead pitch, a 32-pin thin small-outline package (DD suffix), and a reverse pinout thin small-outline package (DU suffix).

DD PACKAGE
(TOP VIEW)



DU PACKAGE
REVERSE PINOUT
(TOP VIEW)



device symbol nomenclature

TMS29LF040 -10 C5 FM L 4

PEP4 Burn-In
- 4 = 168 Hour Burn-In (blank if no burn-in)

Temperature Range Designator
- L = 0°C to 70°C
- E = – 40°C to 85°C

Package Designator
- FM = Plastic Leaded Chip Carrier
- DD = Thin Small-Outline Package
- DU = Thin Small-Outline Package, Reverse Pinout

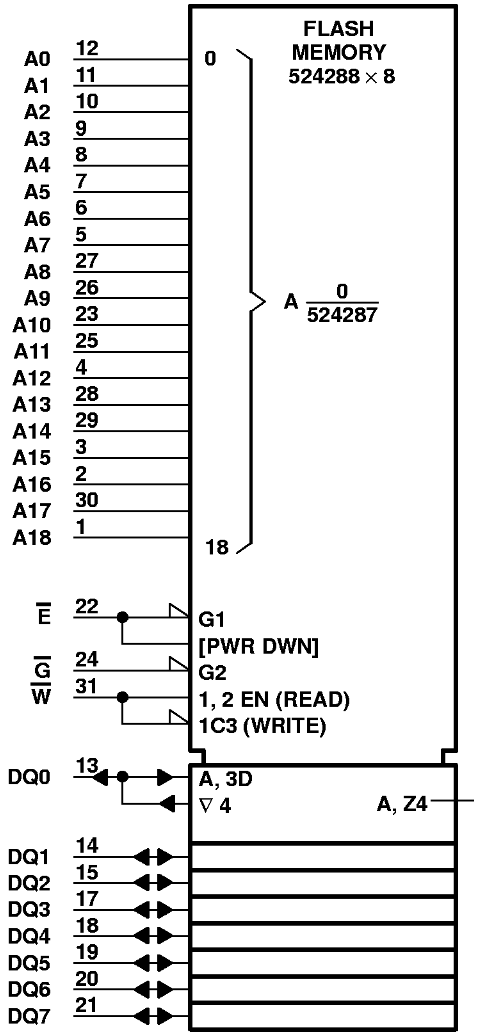
Program / Erase Endurance
- C5 = 100 000 Cycles

L V_{CC} Range Speed Designator
- -60 = 60 ns
- -75 = 75 ns
- -90 = 90 ns
- -10 = 100 ns

V V_{CC} Range Speed Designator
- -12 = 120 ns
- -15 = 150 ns
- -20 = 200 ns

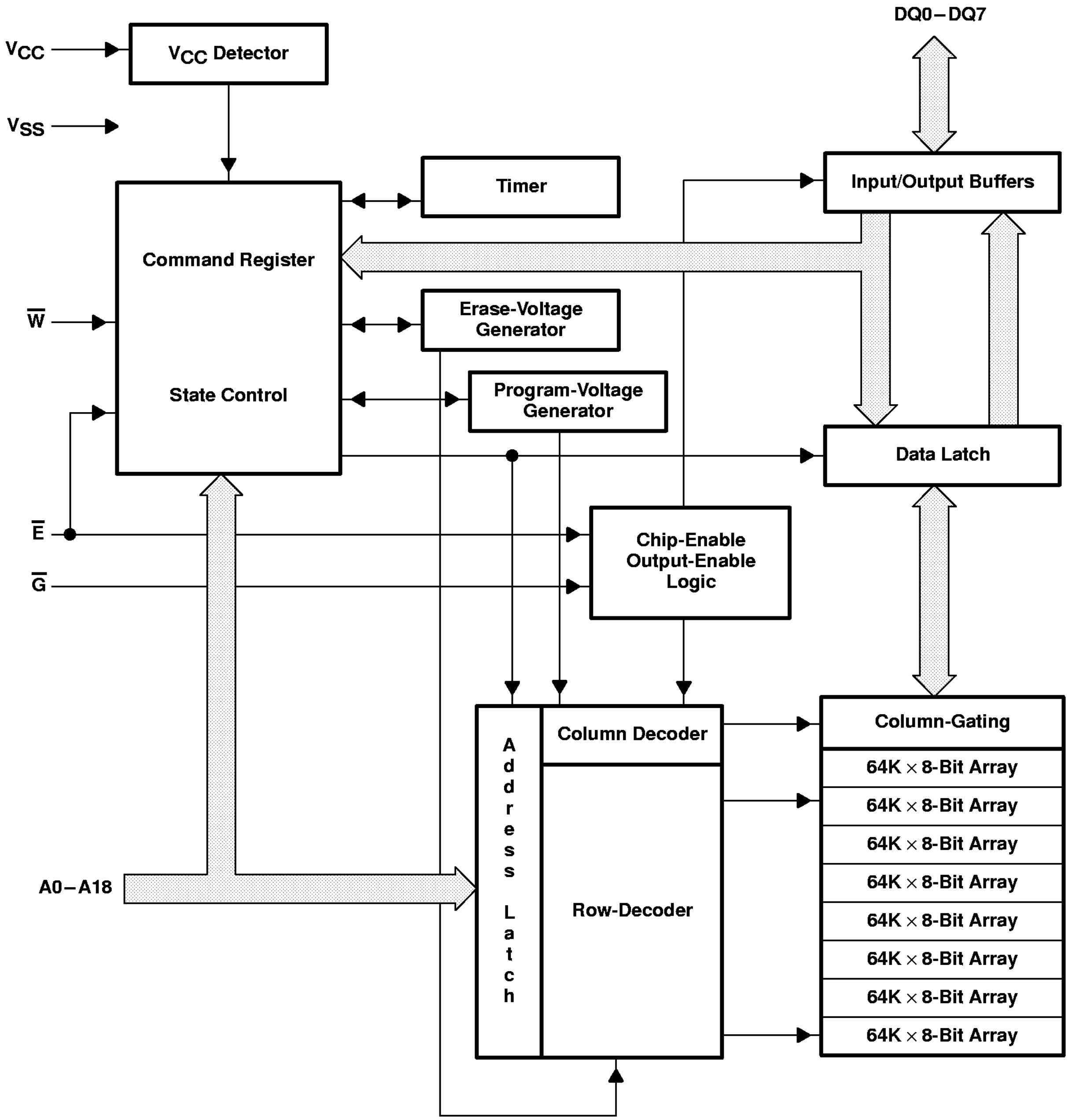
V_{CC} Range Designator
- L = 3.3 V ± 0.3 V V_{CC} (Low Voltage)
- V = 2.7 V – 3.6 V V_{CC} (Very Low Voltage)

logic symbol†

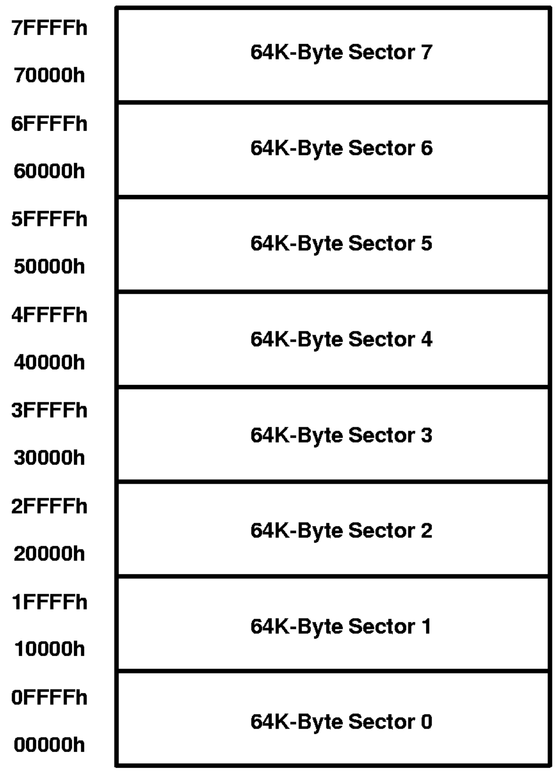


† This symbol is in accordance with ANSI / IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FM package.

block diagram



memory sector architecture



	A18	A17	A16	Address Range
Sector 0	0	0	0	00000h – 0FFFFH
Sector 1	0	0	1	10000h – 1FFFFH
Sector 2	0	1	0	20000h – 2FFFFH
Sector 3	0	1	1	30000h – 3FFFFH
Sector 4	1	0	0	40000h – 4FFFFH
Sector 5	1	0	1	50000h – 5FFFFH
Sector 6	1	1	0	60000h – 6FFFFH
Sector 7	1	1	1	70000h – 7FFFFH

memory sector architecture (continued)

Table 1. Operation Modes

MODE	FUNCTIONS†							
	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	DQ0–DQ7
Read‡	V_{IL}	V_{IL}	V_{IH}	X	X	X	X	Data out
Output disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	Hi-Z
Standby and write inhibit	V_{IH}	X	X	X	X	X	X	Hi-Z
Algorithm-selection mode	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Mfr equivalent code 97h
				V_{IH}				Device equivalent code 94h
Write§	V_{IL}	V_{IH}	V_{IL}	A0	A1	A6	A9	Data in
Sector protect	V_{IL}	V_{ID}	V_{IL}	X	X	X	V_{ID}	X
Sector protect verify	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Data out
Sector unprotect	See Figure 16	See Figure 16	V_{IL}	V_{IL}	V_{IH}	V_{IH}	See Figure 16	Data out
Sector unprotect verify	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Data out
Erase operations	V_{IL}	V_{IH}	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1

† X can be V_{IL} or V_{IH}.
‡ If $\overline{G} = V_{IL}$, then $\overline{W}$ can be V_{IL}. $\overline{G} = V_{IH}$ permits write operations.
§ Refer to Table 3 for valid address and data during write.
NOTE 1: Refer to Figure 6, Figure 7, Figure 8, and Figure 9.

operation

read mode

To read the output of the TMS29xF040, a low-level logic signal is applied to the $\overline{E}$ and $\overline{G}$ pins. When two or more TMS29xF040 devices are connected in parallel, the output of any one device can be read without interference. The $\overline{E}$ pin is power control and should be used for device selection. The $\overline{G}$ pin is output control and should be used to gate the data output onto the bus from the selected device.

The address access time (t_{AVQV}) is the delay from stable address to valid output data. The chip-enable access time (t_{ELQV}) is the delay from $\overline{E}$ = logic low and stable addresses to valid output data. The output-enable access time (t_{GLQV}) is the delay from $\overline{G}$ = logic low to valid output data, when $\overline{E}$ = logic low and addresses are stable for at least $t_{AVQV} - t_{GLQV}$.

standby mode

I_{CC} supply current is reduced by applying a logic-high level on $\overline{E}$ to enter the standby mode. In the standby mode, the outputs are placed in the high-impedance state. Applying a CMOS logic-high level on $\overline{E}$ reduces the current to 100 µA maximum. Applying a TTL logic-high level on $\overline{E}$ reduces the current to 1 mA maximum.

If the TMS29xF040 is deselected during erasure or programming, the device continues to draw active current until the operation is complete.

output disable

When $\overline{G} = V_{IH}$ or $\overline{E} = V_{IH}$, output from the device is disabled and the output pins (DQ0–DQ7) are placed in the high-impedance state.

algorithm selection

The algorithm-selection mode provides access to a binary code that matches the device with its proper programming and erase command operations. This mode is activated when V_{ID} (11.5 V to 12.5 V) is placed on address pin A9. Address pins A1 and A6 must be logic-low. Two bytes of code are accessed by toggling address pin A0 from V_{IL} to V_{IH}. Address pins other than A0, A1 and A6 can be logic-low or logic-high.

The algorithm-selection code also can be read by using the command register. This is useful when V_{ID} is not available to be placed on address pin A9. Table 2 shows the binary algorithm selection codes for the TMS29xF040.

Table 2. Algorithm Selection Codes†

ALGORITHM SELECTION	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Byte 0	0	1	0	0	1	0	1	1	1	97h
Byte 1	1	1	0	0	1	0	1	0	0	94h

† A1 = V_{IL}, A6 = V_{IL}, $\overline{E}$ = $\overline{G}$ = V_{IL}

erasure and programming

Erasure and programming of the TMS29xF040 are accomplished by writing a sequence of commands using standard microprocessor write timing. The commands are written to a command register and input to the command-state machine. The command-state machine interprets the command entered and initiates program, erase, suspend, and resume operations as instructed. The command-state machine acts as the interface between the write-state machine and external-chip operations. The write-state machine controls all voltage generation, pulse generation, preconditioning, and verification of the contents of the memory. Program and block/chip-erase functions are fully automatic. Once the end of a program or erase operation has been reached, the device internally resets to the read mode. If V_{CC} drops below the low-voltage-detect level (VLKO), any operation in progress is aborted and the device resets to the read mode. If a byte program or chip-erase operation is in progress, additional program/erase commands are ignored until the operation in progress completes.

command definitions

Device operating modes are selected by writing specific address and data sequences into the command register. Table 3 defines the valid command sequences. Writing incorrect address and data values or writing them in the incorrect sequence causes the device to reset to the read mode. The command register does not occupy an addressable memory location. The register is used to store the command sequence along with the address and data needed by the memory array. Commands are written by setting $\overline{E}$ = V_{IL} and $\overline{G}$ = V_{IH} and bringing $\overline{W}$ from logic-high to logic-low. Addresses are latched on the falling edge of $\overline{W}$ and data is latched on the rising edge of $\overline{W}$. Holding $\overline{W}$ = V_{IL} and toggling $\overline{E}$ can be used as an alternative. Refer to the switching characteristics of write/erase/program operations section for specific timing information.

command definitions (continued)

Table 3. Command Definitions†

COMMAND	BUS CYCLES	1ST CYCLE ADDR DATA	2ND CYCLE ADDR DATA	3RD CYCLE ADDR DATA	4TH CYCLE ADDR DATA	5TH CYCLE ADDR DATA	6TH CYCLE ADDR DATA
Read/reset	1	XXXXhF0h					
	4	5555h AAh	2AAAh 55h	5555h F0h	RA RD		
Algorithm selection	4	5555h AAh	2AAAh 55h	5555h 90h	RA RD		
Byte program	4	5555h AAh	2AAAh 55h	5555h A0h	PA PD		
Chip erase	6	5555h AAh	2AAAh 55h	5555h 80h	5555h AAh	2AAAh 55h	5555h 10h
Sector erase	6	5555h AAh	2AAAh 55h	5555h 80h	5555h AAh	2AAAh 55h	SA 30h
Sector erase-suspend		XXXXh B0h	Erase-suspend valid during sector-erase operation				
Sector erase-resume		XXXXh 30h	Erase-resume valid only after erase-suspend				

LEGEND:
RA = Address of the location to be read
PA = Address of the location to be programmed
SA = Address of the sector to be erased
Address A18, A17, A16 select 1 of 8 sectors
RD = Data to be read at selected address location
PD = Data to be programmed at selected address location
† Address pins A18, A17, A16, A15 = V_{IL} or V_{IH} for all bus cycle addresses except for program address (PA), sector address (SA), and read address (RA).

read/reset command

The read or reset mode is activated by writing either of the two read/reset command sequences into the command register. The device remains in this mode until one of the other valid command sequences is input into the command register. Memory data is available in the read mode and can be read with standard microprocessor read-cycle timing.

On power up, the device defaults to the read/reset mode. A read/reset command sequence is not required and memory data is available.

algorithm-selection command

The algorithm-selection command allows access to a binary code that matches the device with the proper programming and erase-command operations. After writing the three-bus-cycle command sequence, the first byte of the algorithm selection code (97h) can be read from address XX00h. The second byte of the code (94h) can be read from address XX01h (see Table 2). This mode remains in effect until another valid command sequence is written to the device.

byte-program command

Byte programming is a four-bus-cycle command sequence. The first three bus cycles put the device into the program-setup state. The fourth bus cycle loads the address location and the data to be programmed into the device. The addresses are latched on the falling edge of $\overline{W}$ and the data is latched on the rising edge of $\overline{W}$ in the fourth bus cycle. The rising edge of $\overline{W}$ starts the byte-program operation. The embedded byte-programming function automatically provides needed voltage and timing to program and verify the cell margin. Any further commands written to the device during the program operation are ignored.

Programming can be performed at any address location in any order. When erased, all bits are in a logic 1 state. Logic 0s are programmed into the device. Attempting to program logic 1 into a bit that was previously programmed to a logic 0 causes the internal pulse counter to exceed the pulse count limit. This sets the exceed timing limit indicator (DQ5) to a logic-high state. Only an erase operation can change bits from logic 0s to logic 1s. Figure 3 shows a flowchart of the typical device programming operation.

byte-program command (continued)

The status of the device during the automatic programming operation can be monitored for completion using the data-polling feature or the toggle-bit feature. See the "operation status" section for a full description.

chip-erase command

Chip-erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase-setup state. The next two bus cycles unlock the erase mode. The sixth bus cycle loads the chip-erase command. This command sequence is required to ensure that the memory contents are not erased accidentally. The rising edge of $\overline{W}$ starts the chip-erase operation. Any further commands written to the device during the chip-erase operation are ignored.

The embedded chip-erase function automatically provides voltage and timing needed to program and verify all the memory cells prior to electrical erase. It then erases and verifies the cell margin automatically. The user is not required to program the memory cells prior to erase. The status of the device during the automatic chip-erase operation can be monitored for completion using the data-polling feature or the toggle-bit feature. See the operation status section for a full description. Figure 6 shows a flowchart for the typical chip-erase device operation.

sector-erase command

Sector erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase setup state. The next two bus cycles unlock the erase mode. The sixth bus cycle loads the sector-erase command and the sector-address location to be erased. Any address location within the desired sector may be used. The addresses are latched on the falling edge of $\overline{W}$ and the sector-erase command (30h) is latched on the rising edge of $\overline{W}$ in the sixth bus cycle. After a delay of 100 μs from the rising edge of $\overline{W}$, the sector-erase operation begins on the selected sector(s).

Additional sectors can be selected to be erased concurrently during the sector-erase command sequence. For each additional sector to be selected for erase, another bus cycle is issued. The bus cycle loads the next sector-address location and the sector-erase command. The time between the end of the previous bus cycle and the start of the next bus cycle must be less than 100 μs; otherwise, the new sector location is not loaded. A time delay of 100 μs from the rising edge of the last $\overline{W}$ starts the sector-erase operation. If there is a falling edge of $\overline{W}$ within the 100-μs time delay, the timer is reset.

One to eight sector-address locations can be loaded in any order. The state of the delay timer can be monitored using the sector-erase delay indicator (DQ3). If DQ3 is logic-low, the time delay has not expired. See the "operation status" section for a description.

Any command other than erase suspend (B0h) or sector erase (30h) written to the device during the sector-erase operation causes the device to exit the sector-erase mode. The contents of the sector(s) selected for erase are not valid. To complete the sector-erase operation, re-issue the sector-erase command sequence.

The embedded sector-erase function automatically provides needed voltage and timing to program and to verify all of the memory cells prior to electrical erase and then erases and verifies the cell margin automatically. Programming the memory cells prior to erase is not required. The status of the device during the automatic sector-erase operation can be monitored for completion by using the data-polling feature or the toggle-bit feature. See the operation status section for a full description. Figure 8 shows a flowchart for the typical sector-erase device operation.

erase-suspend command

The erase-suspend command (B0h) allows interruption of a sector-erase operation in order to read data from unaltered sectors of the device. Erase-suspend is a one-bus-cycle command. The addresses can be V_{IL} or V_{IH} and the erase-suspend command (B0h) is latched on the rising edge of $\overline{W}$. Once the sector-erase operation is in progress, the erase-suspend command requests the internal write-state machine to halt operation at

erase-suspend command (continued)

predetermined breakpoints. The erase-suspend command is valid only during the sector-erase operation and is invalid during the byte programming and chip-erase operations. The sector-erase delay timer expires immediately if the erase-suspend command is issued while the delay is active.

After erase-suspend is issued, the device takes between 0.1 μs and 15 μs to suspend the operation. The toggle bit must be monitored to determine when the suspend has been executed. When the toggle bit stops toggling, data can be read from sectors that are not selected for erase. See the “operation status” section for a full description. Reading from a sector selected for erase can result in invalid data.

Once the sector-erase operation is suspended, further writes of the erase-suspend command are ignored. Any command other than erase suspend (B0h) or erase resume (30h) written to the device during the erase suspend mode causes the device to exit the suspend mode. To complete the sector-erase operation, re-issue the sector-erase command sequence.

erase-resume command

The erase-resume command (30h) restarts a suspended sector-erase operation from where it was halted to completion. Erase resume is a one-bus-cycle command. The addresses can be V_{IL} or V_{IH} and the erase-resume command (30h) is latched on the rising edge of $\overline{W}$. When an erase-suspend/erase-resume command combination is written, the internal pulse counter (exceed timing limit) is reset. The erase-resume command is valid only in the erase-suspend state. After the erase-resume command is executed, the device returns to the valid sector-erase state and further writes of the erase-resume command are ignored. After the device has resumed the sector-erase operation, another erase-suspend command can be issued to the device.

operation status

status-bit definitions

During operation of the automatic embedded program and erase functions, the status of the device can be determined by reading the data state of designated outputs. The data-polling bit (DQ7) and toggle-bit (DQ6) require multiple successive reads to observe a change in the state of the designated output. Table 4 defines the values of the status flags.

Table 4. Operation Status Flags†

Device Operation‡	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Byte programming in progress	$\overline{D}$	T	0	X	0	X	X	X
Byte programming exceed time limit	$\overline{D}$	T	1	X	0	X	X	X
Byte programming complete	D	D	D	D	D	D	D	D
Sector-/chip-erase in progress	0	T	0	X	1	X	X	X
Sector-/chip-erase exceed time limit	0	T	1	X	1	X	X	X
Sector-/chip-erase complete	1	1	1	1	1	1	1	1

† T= toggle, D= data, X=data undefined
‡ DQ4, DQ2, DQ1, DQ0 are reserved for future use.

data-polling DQ7

The data-polling status function outputs the complement of the data latched into the DQ7 data register while the write-state machine is engaged in a program or erase operation. Data bit DQ7 changing from complement to true indicates the end of an operation. Data-polling is available only during the byte-programming, chip-erase, sector-erase, and sector-erase timing delay. Data-polling is valid after the rising edge of $\overline{W}$ in the last bus cycle of the command sequence loaded into the command register. Figure 10 shows a flowchart for data-polling.

data-polling DQ7 (continued)

During a byte-program operation, reading DQ7 outputs the complement of the DQ7 data to be programmed at the selected address location. Upon completion, reading DQ7 outputs the true DQ7 data loaded into the program data register. During the erase operations, reading DQ7 outputs a 0. Upon completion, reading DQ7 outputs a 1. Also, data-polling must be performed at a sector address that is within a sector being erased; otherwise, the status is invalid. When using data-polling, the address should remain stable throughout the operation.

During a data-polling read, while $\overline{G}$ is low, data bit DQ7 may change asynchronously. Depending on the read timing, the system can read valid data on DQ7, while other DQ pins are still invalid. A subsequent read of the device is valid. See Figure 11 for the data-polling timing diagram.

toggle-bit DQ6

The toggle-bit status function outputs data on DQ6 that toggles between 1 and 0 while the write-state machine is engaged in a program or erase operation. When toggle-bit DQ6 stops toggling after two consecutive reads to the same address, the operation is complete. The toggle-bit is only available during the byte programming, chip erase, sector erase, and sector-erase timing delay. Toggle-bit data is valid after the rising edge of $\overline{W}$ in the last bus cycle of the command sequence loaded into the command register. Figure 12 shows a flowchart for the toggle-bit status read algorithm. Depending on the read timing, DQ6 can stop toggling while other DQ pins are still invalid. A subsequent read of the device is valid. See Figure 13 for the toggle-bit timing diagram.

exceed time limit DQ5

The program and erase operations use an internal pulse counter to limit the number of pulses applied. If the pulse count limit is exceeded, DQ5 is set to a 1 data state. This indicates that the program or erase operation has failed. DQ7 will not change from complemented data to true data and DQ6 will not stop toggling when read. To continue operation, the device must be reset.

This condition occurs when attempting to program a logic 1 state into a bit that has been programmed previously to a logic 0. Only an erase operation can change bits from 0 to 1. After reset, the device is functional and can be erased and reprogrammed.

sector-load-timer DQ3

The sector-load-timer status bit, DQ3, is used to determine whether the time to load additional sector addresses has expired. After completion of a sector erase command sequence, DQ3 remains at a logic low for 80 µs. This indicates that another sector-erase command sequence can be issued. If DQ3 is at a logic high, it indicates that the delay has expired and attempts to issue additional sector-erase commands are ignored. See the sector-erase command section for a description.

The data-polling bit and toggle bit are valid during the 100-µs time delay and can be used to determine if a valid sector-erase command has been issued. To ensure additional sector-erase commands have been accepted, the status of DQ3 should be read before and after each additional sector-erase command. If DQ3 is at a logic low on both reads, then the additional sector-erase command was accepted.

data protection

hardware-sector protection feature

This feature disables both programming and erase operations on any combination of one to eight sectors. Commands to program or erase a protected sector do not change the data contained in the sector. The data polling and toggle bit operate for 2 µs to 100 µs and then return to valid data. This feature is enabled using high-voltage V_{ID} (11.5 V to 12.5 V) on address pin A9 and control pin $\overline{G}$ and V_{IL} on control pin $\overline{E}$. Figure 14 shows a flow chart for the sector-protect operation.

hardware-sector protection feature (continued)

The device is delivered with all sectors unprotected. The sector-unprotect mode is available to unprotect protected sectors. Figure 16 is a flow chart for the unprotect operation.

sector-protect operation

The sector-protect mode is activated when $\overline{W}$ = V_{IH}, $\overline{E}$= V_{IL} and address pin A9 and control pin $\overline{G}$ are forced to V_{ID}. The sector-select address pins A18, A17, and A16 are used to select the sector to be protected. Address pins A0–A15 and I/O pins DQ0–DQ7 must be stable and can be V_{IL} or V_{IH}. Once the addresses are stable, $\overline{W}$ is pulsed low for 100 µs. The operation begins on the falling edge of $\overline{W}$ and terminates on the rising edge of $\overline{W}$. Figure 15 shows a timing diagram for the sector-protect operation.

sector-protect verify

Verification of sector-protection is activated when $\overline{W}$ = V_{IH}, $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and address pin A9 = V_{ID}. Address pins A0 and A6 are set to V_{IL}, and A1 is set to V_{IH}. The sector-address pins A18, A17, and A16 select the sector to be verified. The other addresses can be V_{IH} or V_{IL}. If the sector selected is protected, the DQs output 01h. If the sector selected is not protected, the DQs output 00h.

Sector-protection can also be verified using the algorithm-selection command. After issuing the three bus-cycle command sequence, the sector-protection status can be read on DQ0. Set address pins A0 = V_{IL}, A1 = V_{IH}, and A6 = V_{IL}. The sector address pins A18, A17, and A16 select the sector to be verified. The remaining addresses are set to V_{IL}. If the sector selected is protected, DQ0 outputs a 1 state. If the sector selected is not protected, DQ0 outputs a 0 state. This mode remains in effect until another valid command sequence is written to the device.

sector-unprotect

Prior to sector unprotection, all sectors should be protected using the sector-protect mode. The sector-unprotect mode is activated when $\overline{W}$ = V_{IH} and address pin A9 and control pins $\overline{G}$ and $\overline{E}$ are forced to V_{ID}. Address pins A6, A12, and A16 are set to V_{IH}. The sector select address pins A18, A17, and A16 can be V_{IL} or V_{IH}. All eight sectors are unprotected in parallel. Once the inputs are stable, $\overline{W}$ is pulsed low for 10 ms. The unprotect operation begins on the falling edge of $\overline{W}$ and terminates on the rising edge of $\overline{W}$. Figure 17 shows a timing diagram for sector unprotection.

sector-unprotect verify

Verification of the sector unprotection is activated when $\overline{W}$ = V_{IH}, $\overline{G}$ = V_{IL}, $\overline{E}$ =V_{IL} and address pin A9 = V_{ID}. Select the sector to be verified. Address pins A1 and A6 are set to V_{IH}, and A0 is set to V_{IL}. The other addresses can be V_{IH} or V_{IL}. If the sector selected is protected, the DQs output 01h. If the sector is not protected, the DQs output 00h. Sector unprotection can also be read using the algorithm-selection command.

low V_{CC} write lockout

During power-up and power-down, write operations are locked out for V_{CC} less than V_{LKO}. If $V_{CC} < V_{LKO}$, the command input is disabled and the device is reset to the read mode. On powerup if $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL}, and $\overline{G}$ = V_{IH}, the device does not accept commands on the rising edge of $\overline{W}$. The device automatically powers up in the read mode.

glitching

Pulses of less than 5 ns (typical) on $\overline{G}$, $\overline{W}$, or $\overline{E}$ will not issue a write cycle.

power supply considerations

Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Printed circuit traces to V_{CC} should be appropriate to handle the current demand and minimize inductance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 2) . . . . –0.6 V to 7 V
Input voltage range: All inputs except A9, $\overline{E}$, $\overline{G}$ (see Note 3) . . . . –0.6 V to V_{CC} + 1 V
A9, $\overline{E}$, $\overline{G}$ . . . . –0.6 V to 13.5 V
Output voltage range (see Note 4) . . . . –0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program, T_A
(L) . . . . 0°C to 70°C
(E) . . . . – 40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. All voltage values are with respect to GND.
3. The voltage on any input pin can undershoot to –2 V for periods less than 20 ns.
4. The voltage on any output pin can overshoot to 5 V for periods less than 20 ns.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	’29LF040 V_{CC} range	3	3.3	3.6	V
		’29VF040 V_{CC} range	2.7	3	3.6	
V_{IH}	High-level dc input voltage		2		V_{CC}+0.5	V
V_{IL}	Low-level dc input voltage		–0.5		0.8	V
V_{ID}	Algorithm selection and sector-protect input voltage		11.5		12.5	V
V_{LKO}	Low V_{CC} lock-out voltage		2			V
T_A	Operating free-air temperature during read/erase/program	L	0		70	°C
		E	–40		85	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL-input level	I_{OH} = – 2.5 mA	V_{CC} = V_{CC}MIN‡	2.4		V
		CMOS-input level	I_{OH} = – 100 µA	V_{CC} = V_{CC}MIN‡	V_{CC} – 0.4		
V_{OL}	Low-level output voltage	TTL-input level	I_{OL} = 5.8 mA	V_{CC} = V_{CC}MIN‡		0.45	V
		CMOS-input level	I_{OL} = 5.8 mA	V_{CC} = V_{CC}MIN‡		0.45	
I_I	Input current (leakage)		V_{IN} = GND to V_{CC},	V_{CC} = 3.6 V		±1	µA
I_O	Output current (leakage)		V_O = GND to V_{CC},	$\overline{E}$ = V_{IH}		±1	µA
I_{ID}	High-voltage current (standby)		A9 = 12.5 V			50	µA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{E}$ = V_{IH},	V_{CC} = 3.6 V		1	mA
		CMOS-input level	$\overline{E}$ = V_{CC} ± 0.5 V,	V_{CC} = 3.6 V		100	µA
I_{CC2}	V_{CC} supply current (see Note 5)		$\overline{E}$ = V_{IL},	$\overline{G}$ = V_{IH}		40	mA
I_{CC3}	V_{CC} supply current (see Notes 6 and 7)		$\overline{E}$ = V_{IL},	$\overline{G}$ = V_{IH}		60	mA

‡ See the recommended operating conditions table.

NOTES: 5. I_{CC} current in the read mode, switching at 6 MHz, I_{OUT} = 0 mA
6. I_{CC} current while erase or program operation is in progress
7. Not 100% tested

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_{i1}	Input capacitance (All inputs except A9, $\overline{E}$, $\overline{G}$) (See Note 7)	V_I = 0 V, f = 1 MHz		7.5	pF
C_{i2}	Input capacitance (A9, $\overline{E}$, $\overline{G}$) (See Note 7)	V_I = 0 V, f = 1 MHz		9	pF
C_o	Output capacitance (See Note 7)	V_O = 0 V, f = 1 MHz		12	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, read-only operation (see Figure 1)

PARAMETER		ALTERNATE SYMBOL	'29LF040-60		'29LF040-75		'29LF040-90		'29LF040-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Cycle time, read (see Note 7)	$t_{c(R)}$	60		75		90		100		ns
t_{AVQV}	Access time, address	$t_{a(A)}$		60		75		90		100	ns
t_{ELQV}	Access time, $\overline{E}$	$t_{a(E)}$		60		75		90		100	ns
t_{GLQV}	Access time, $\overline{G}$	$t_{a(G)}$		30		35		35		45	ns
t_{EHQZ}	Disable time, $\overline{E}$ to high impedance (see Note 7)	$t_{dis(E)}$		20		20		20		30	ns
t_{GHQZ}	Disable time, $\overline{G}$ to high impedance (see Note 7)	$t_{dis(G)}$		20		20		20		30	ns
t_{ELQX}	Enable time, $\overline{E}$ to low impedance (see Note 7)	$t_{en(E)}$	0		0		0		0		ns
t_{GLQX}	Enable time, $\overline{G}$ to low impedance (see Note 7)	$t_{en(G)}$	0		0		0		0		ns
t_{AXQX}	Hold time, output from address $\overline{E}$ or $\overline{G}$ change (see Note 7)	$t_{h(D)}$	0		0		0		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, read-only operation (see Figure 1) (continued)

PARAMETER		ALTERNATE SYMBOL	'29VF040-12		'29VF040-15		'29VF040-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Cycle time, read (see Note 7)	$t_{c(R)}$	120		150		200		ns
t_{AVQV}	Access time, address	$t_{a(A)}$		120		150		200	ns
t_{ELQV}	Access time, $\overline{E}$	$t_{a(E)}$		120		150		200	ns
t_{GLQV}	Access time, $\overline{G}$	$t_{a(G)}$		60		70		90	ns
t_{EHQZ}	Disable time, $\overline{E}$ to high impedance (see Note 7)	$t_{dis(E)}$		40		40		60	ns
t_{GHQZ}	Disable time, $\overline{G}$ to high impedance (see Note 7)	$t_{dis(G)}$		40		40		60	ns
t_{ELQX}	Enable time, $\overline{E}$ to low impedance (see Note 7)	$t_{en(E)}$	0		0		0		ns
t_{GLQX}	Enable time, $\overline{G}$ to low impedance (see Note 7)	$t_{en(G)}$	0		0		0		ns
t_{AXQX}	Hold time, output from address $\overline{E}$ or $\overline{G}$ change (see Note 7)	$t_{h(D)}$	0		0		0		ns

NOTE 7: Not 100% tested

timing requirements over recommended ranges of supply voltage and operating free-air temperature, controlled by $\overline{W}$

PARAMETER		ALTERNATE SYMBOL	'29LF040-60		'29LF040-75		'29LF040-90		'29LF040-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Cycle time, write (see Note 7)	$t_{c(W)}$	60		75		90		100		ns
t_{AVWL}	Setup time, address	$t_{su(A)}$	0		0		0		0		ns
t_{WLAX}	Hold time, address	$t_{h(A)}$	30		45		45		45		ns
t_{DVWH}	Setup time, data	$t_{su(D)}$	30		30		45		45		ns
t_{WHDX}	Hold time, data valid after $\overline{W}$ high	$t_{h(D)}$	0		0		0		0		ns
t_{ELWL}	Setup time, $\overline{E}$	$t_{su(E)}$	0		0		0		0		ns
t_{WHEH}	Hold time, $\overline{E}$	$t_{h(E)}$	0		0		0		0		ns
t_{WLWH1}	Pulse duration, $\overline{W}$ low	$t_{w(WL)}$	30		35		45		45		ns
t_{WHWL}	Pulse duration, $\overline{W}$ high	$t_{w(WH)}$	20		20		20		20		ns
t_{GHWL}	Recovery time, read before write	$t_{rec(R)}$	0		0		0		0		ns
t_{GHWH}	$\overline{G}$ setup time		0		0		0		0		ns
t_{WHGL1}	Hold time, $\overline{G}$ read		0		0		0		0		ns
t_{WHGL2}	Hold time, $\overline{G}$ toggle, data		10		10		10		10		ns
t_{VCEL}	Setup time, V_{CC} (see Note 7)		50		50		50		50		µs
t_{HVT}	Transition time, V_{ID} (see Notes 7, 8 and 9)		4		4		4		4		µs
t_{WLWH2}	Pulse duration, $\overline{W}$ low (see Note 8)		100		100		100		100		µs
t_{WLWH3}	Pulse duration, $\overline{W}$ low (see Note 9)		10		10		10		10		ms
t_{EHVWL}	Setup time, $\overline{E}$ V_{ID} to $\overline{W}$ (see Notes 8 and 9)		4		4		4		4		µs
t_{GHVWL}	Setup time, $\overline{G}$ V_{ID} to $\overline{W}$ (see Notes 7, 8, and 9)		4		4		4		4		µs
t_{WHWH1}	Cycle time, programming operation	$t_{c(W)PR}$	16		16		16		16		µs
t_{WHWH2}	Cycle time, sector-erase operation (see Note 10)	$t_{c(W)ER}$		30		30		30		30	s
t_{WHWH3}	Cycle time, chip-erase operation (see Note 11)			120		120		120		120	s

NOTES: 7. Not 100% tested
8. Sector protect
9. Sector-unprotect timing
10. Typical value for all speeds is 2 s.
11. Typical value for all speeds is 14 s.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, controlled by $\overline{W}$ (continued)

PARAMETER		ALTERNATE SYMBOL	'29VF040-12		'29VF040-15		'29VF040-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Cycle time, write (see Note 7)	$t_{c(W)}$	120		150		200		ns
t_{AVWL}	Setup time, address	$t_{su(A)}$	0		0		0		ns
t_{WLAX}	Hold time, address	$t_{h(A)}$	60		60		90		ns
t_{DVWH}	Setup time, data	$t_{su(D)}$	60		60		90		ns
t_{WHDX}	Hold time, data valid after $\overline{W}$ high	$t_{h(D)}$	0		0		0		ns
t_{ELWL}	Setup time, $\overline{E}$	$t_{su(E)}$	0		0		0		ns
t_{WHEH}	Hold time, $\overline{E}$	$t_{h(E)}$	0		0		0		ns
t_{WLWH1}	Pulse duration, $\overline{W}$ low	$t_{w(WL)}$	60		70		90		ns
t_{WHWL}	Pulse duration, $\overline{W}$ high	$t_{w(WH)}$	40		40		40		ns
t_{GHWH}	$\overline{G}$ setup time		0		0		0		ns
t_{GHWL}	Recovery time, read before write	$t_{rec(R)}$	0		0		0		ns
t_{WHGL1}	Hold time, $\overline{G}$ read		0		0		0		ns
t_{WHGL2}	Hold time, $\overline{G}$ toggle, data		20		20		20		ns
t_{VCEL}	Setup time, V_{CC} (see Note 7)		50		50		50		µs
t_{HVT}	Transition time, V_{ID} (see Notes 7, 8 and 9)		4		4		4		µs
t_{WLWH2}	Pulse duration, $\overline{W}$ low (see Note 8)		100		100		100		µs
t_{WLWH3}	Pulse duration, $\overline{W}$ low (see Note 9)		10		10		10		ms
t_{EHVWL}	Setup time, $\overline{E}$ V_{ID} to $\overline{W}$ (see Note 9)		4		4		4		µs
t_{GHVWL}	Setup time, $\overline{E}$ V_{ID} to $\overline{W}$ (see Notes 8 and 9)		4		4		4		µs
t_{WHWH1}	Cycle time, programming operation	$t_{c(W)PR}$	16		16		16		µs
t_{WHWH2}	Cycle time, sector-erase operation (see Note 10)	$t_{c(W)ER}$		30		30		30	s
t_{WHWH3}	Cycle time, chip-erase operation (see Note 11)			120		120		120	s

NOTES: 7. Not 100% tested
8. Sector protect
9. Sector-unprotect timing
10. Typical value for all speeds is 2 s.
11. Typical value for all speeds is 14 s.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, controlled by $\overline{E}$ (see Figure 1)

PARAMETER		ALTERNATE SYMBOL	'29LF040-60		'29LF040-75		'29LF040-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Cycle time, write (see Note 7)	$t_{c(W)}$	60		75		90		ns
t_{AVEL}	Setup time, address	$t_{su(A)}$	0		0		0		ns
t_{ELAX}	Hold time, address	$t_{h(A)}$	40		45		45		ns
t_{DVEH}	Setup time, data	$t_{su(D)}$	30		30		45		ns
t_{EHDX}	Hold time, data	$t_{h(D)}$	0		0		0		ns
t_{WLEL}	Setup time, $\overline{W}$	$t_{su(W)}$	0		0		0		ns
t_{EHWH}	Hold time, $\overline{W}$	$t_{h(W)}$	0		0		0		ns
t_{ELEH}	Pulse duration, $\overline{E}$ low	$t_{w(EL)}$	30		35		45		ns
t_{EHEL}	Pulse duration, $\overline{E}$ high	$t_{w(EH)}$	20		20		20		ns
t_{GHEL}	Recovery time, read before write	$t_{rec(R)}$	0		0		0		ns
t_{WHGL1}	Hold time, $\overline{G}$ read	$t_{h(C)}$	0		0		0		ns
t_{WHGL2}	Hold time, $\overline{G}$ toggle, data		10		10		10		ns
t_{EHEH1}	Cycle time, programming operation		16		16		16		µs
t_{WHWH2}	Cycle time, sector-erase operation (see Note 10)	$t_{c(W)ER}$		30		30		30	s
t_{WHWH3}	Cycle time, chip-erase operation (see Note 11)			120		120		120	s

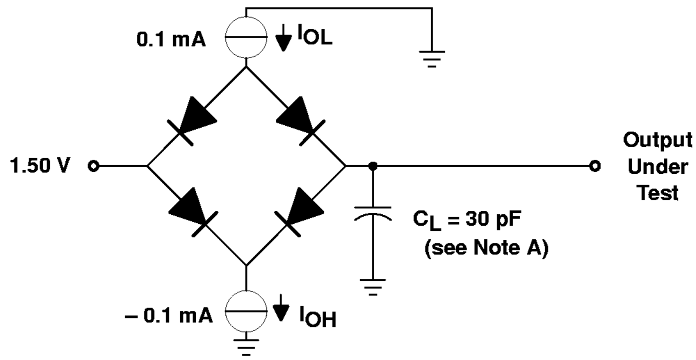
NOTES: 7. Not 100% tested
10. Typical value for all speeds is 2 s.
11. Typical value for all speeds is 14 s.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, controlled by $\overline{E}$ (see Figure 1) (continued)

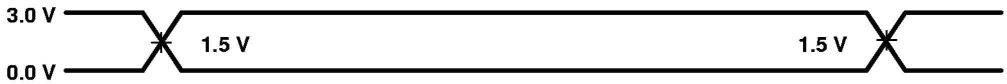
PARAMETER		ALTERNATE SYMBOL	'29LF040-10		'29VF040-12		'29VF040-15		'29VF040-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Cycle time, write (see Note 7)	$t_{c(W)}$	100		120		150		200		ns
t_{AVEL}	Setup time, address	$t_{su(A)}$	0		0		0		0		ns
t_{ELAX}	Hold time, address	$t_{h(A)}$	45		60		60		90		ns
t_{DVEH}	Setup time, data	$t_{su(D)}$	45		60		60		90		ns
t_{EHDX}	Hold time, data	$t_{h(D)}$	0		0		0		0		ns
t_{WLEL}	Setup time, $\overline{W}$	$t_{su(W)}$	0		0		0		0		ns
t_{EHWH}	Hold time, $\overline{W}$	$t_{h(W)}$	0		0		0		0		ns
t_{ELEH}	Pulse duration, $\overline{E}$ low	$t_{w(EL)}$	45		60		60		90		ns
t_{EHEL}	Pulse duration, $\overline{E}$ high	$t_{w(EH)}$	20		40		40		40		ns
t_{GHEL}	Recovery time, read before write	$t_{rec(R)}$	0		0		0		0		ns
t_{WHGL1}	Hold time, $\overline{G}$ read	$t_{h(C)}$	0		0		0		0		ns
t_{WHGL2}	Hold time, $\overline{G}$ toggle, data		10		20		20		20		ns
t_{EHEH1}	Cycle time, programming operation		16		16		16		16		µs
t_{WHWH2}	Cycle time, sector-erase operation (see Note 10)	$t_{c(W)ER}$		30		30		30		30	s
t_{WHWH3}	Cycle time, chip-erase operation (see Note 11)			120		120		120		120	s

NOTES: 7. Not 100% tested
10. Typical value for all speeds is 2 s.
11. Typical value for all speeds is 14 s.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.



NOTE B: The ac testing inputs are driven at 3 V for logic high and 0 V for logic low. Timing measurements are made at 1.5 V for logic high and 1.5 V for logic low on both inputs and outputs. Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} as closely as possible to the device pins.

Figure 1. AC Test Output Load Circuit

PARAMETER MEASUREMENT INFORMATION

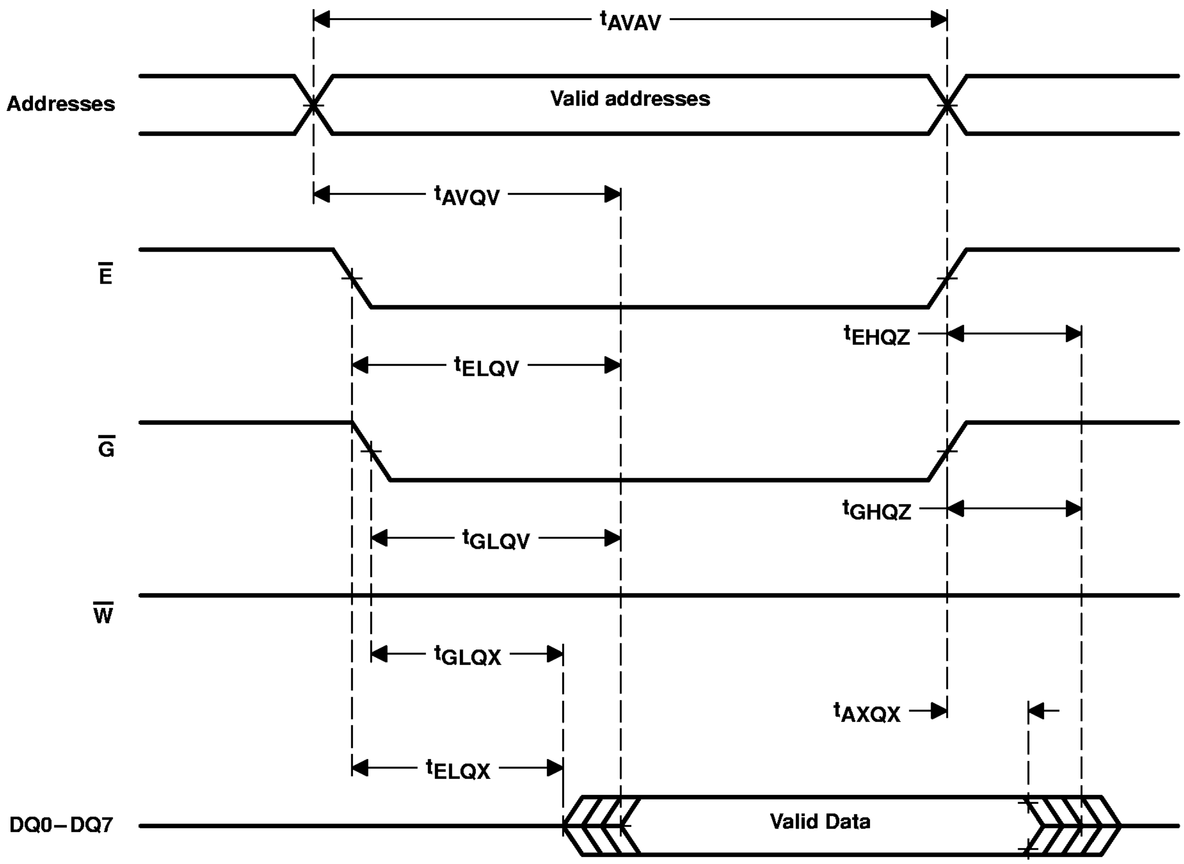


Figure 2. AC Waveform for Read Operation

PARAMETER MEASUREMENT INFORMATION

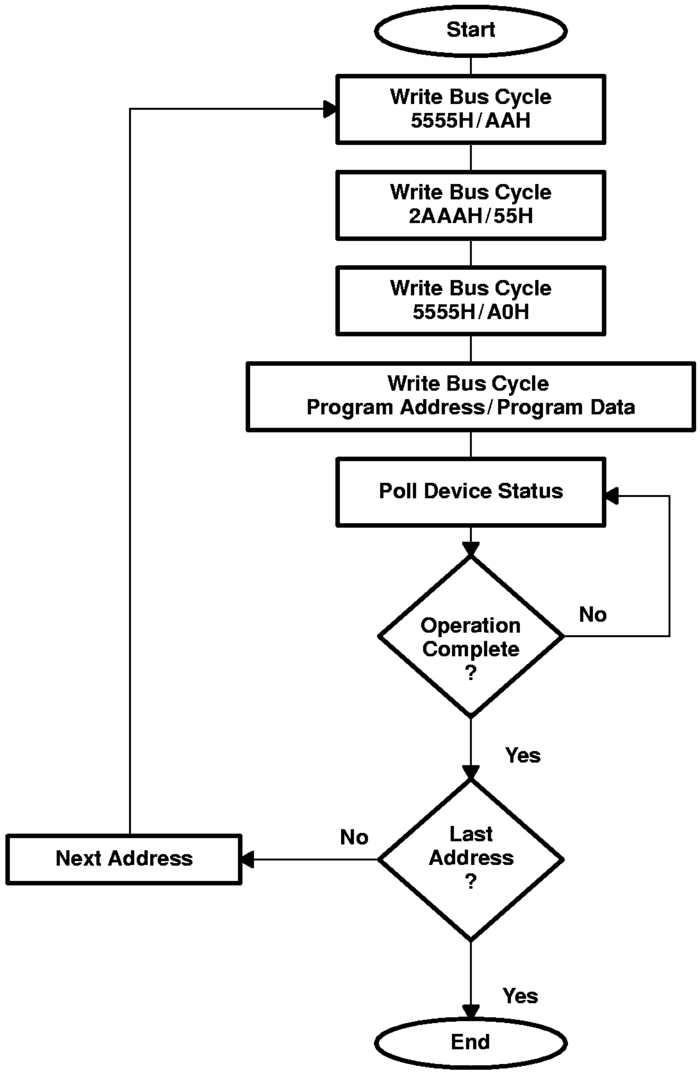
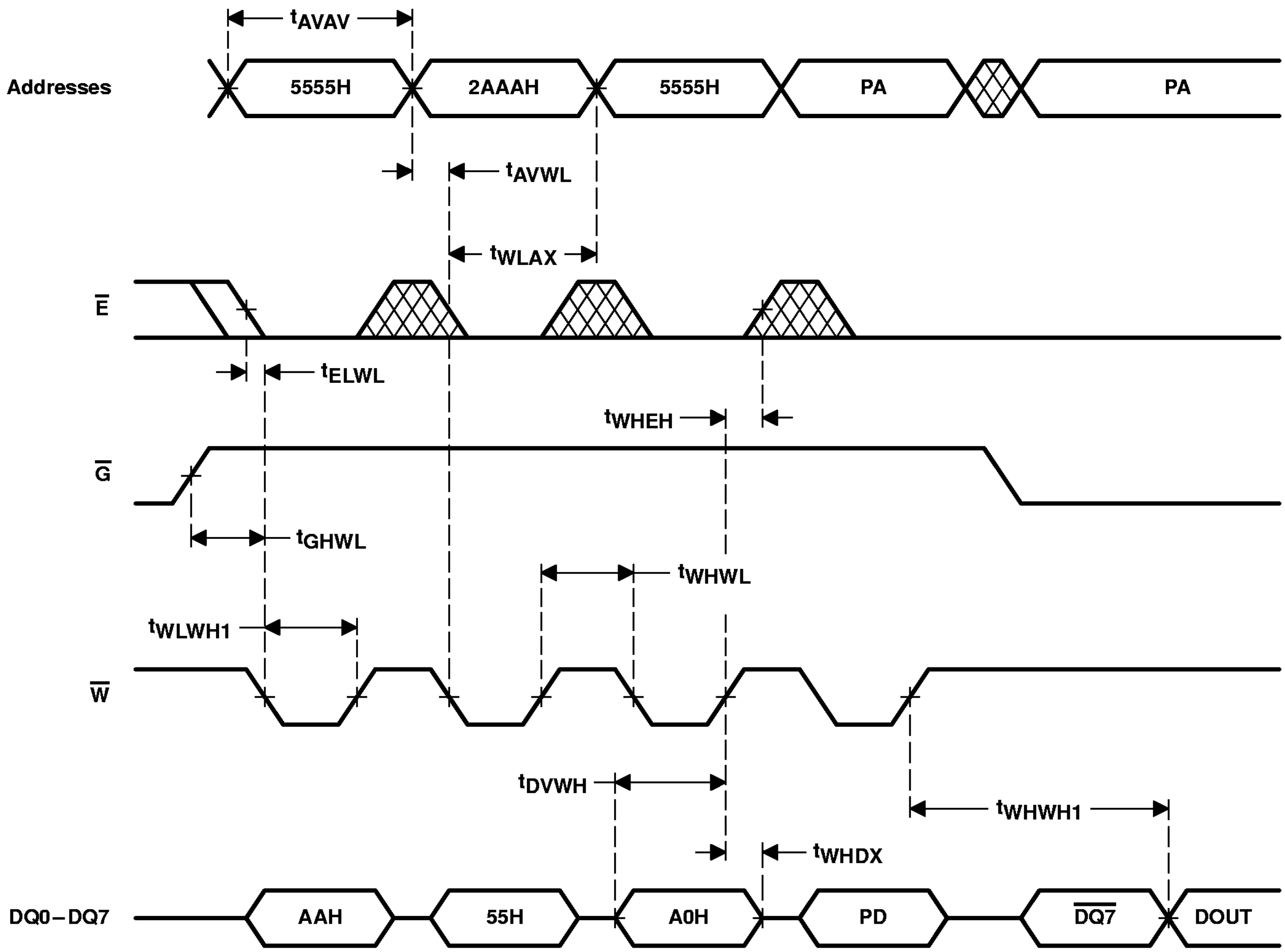


Figure 3. Byte-Program Algorithm

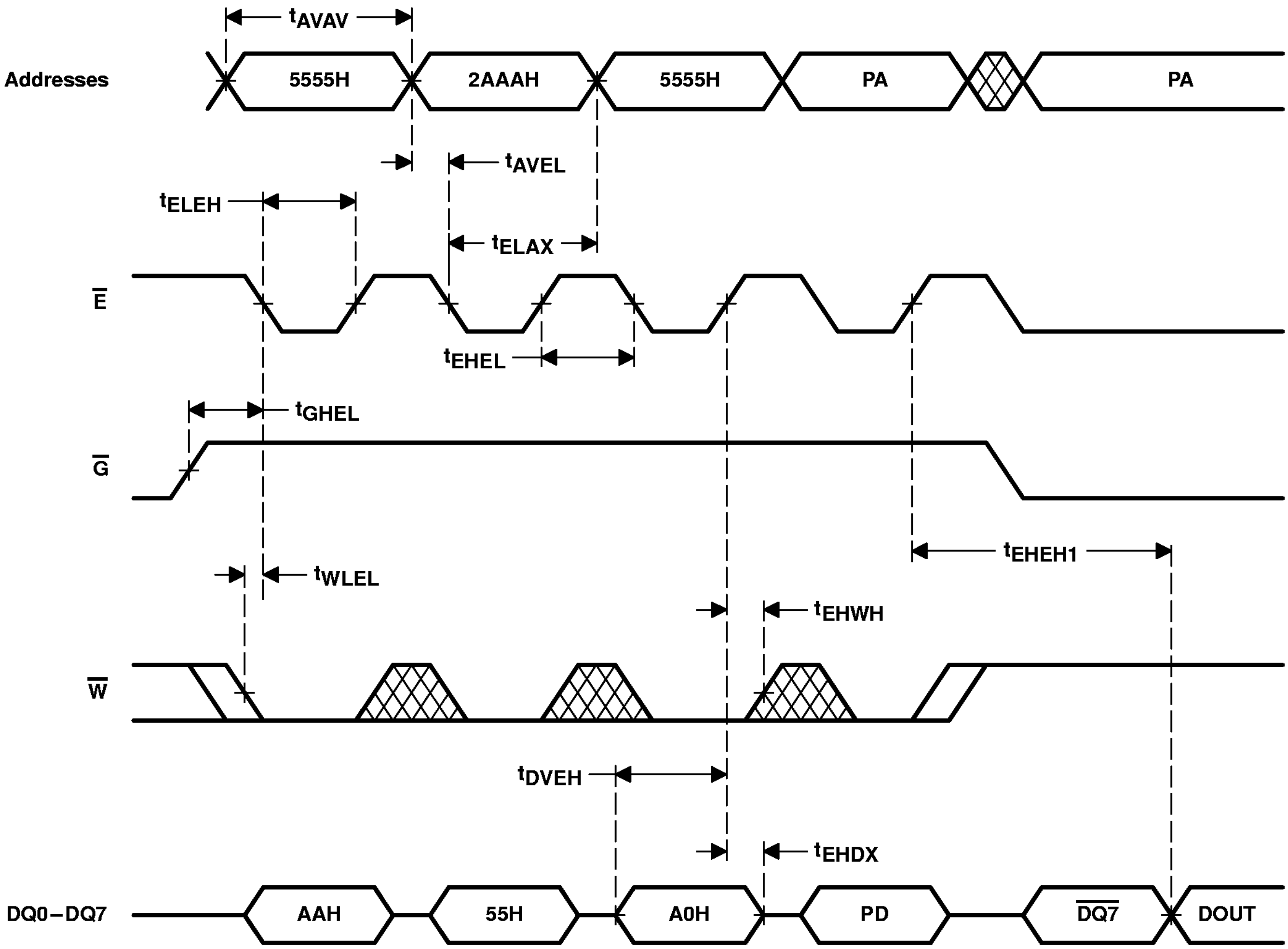
PARAMETER MEASUREMENT INFORMATION



NOTES: A. PA = Address to be programmed
B. PD = Data to be programmed
C. $\overline{DQ7}$ = Complement of data written to DQ7

Figure 4. AC Waveform for Byte-Program Operation

PARAMETER MEASUREMENT INFORMATION



NOTES: A. PA = Address to be programmed
B. PD = Data to be programmed
C. $\overline{DQ7}$ = Complement of data written to DQ7

Figure 5. Alternate $\overline{E}$-Controlled Write Operation

PARAMETER MEASUREMENT INFORMATION

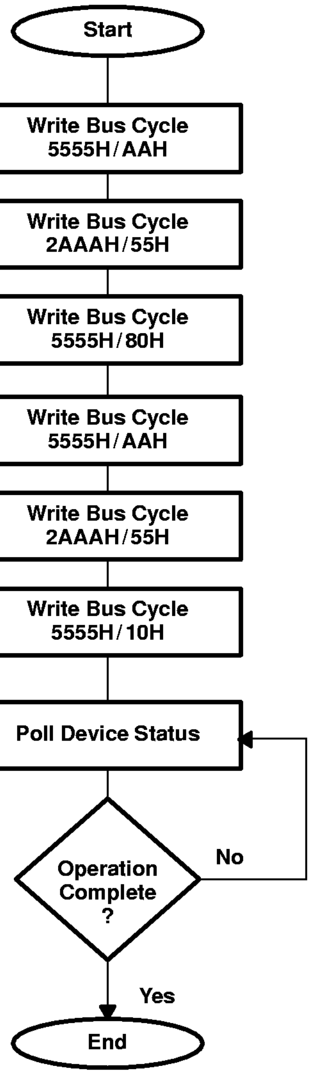
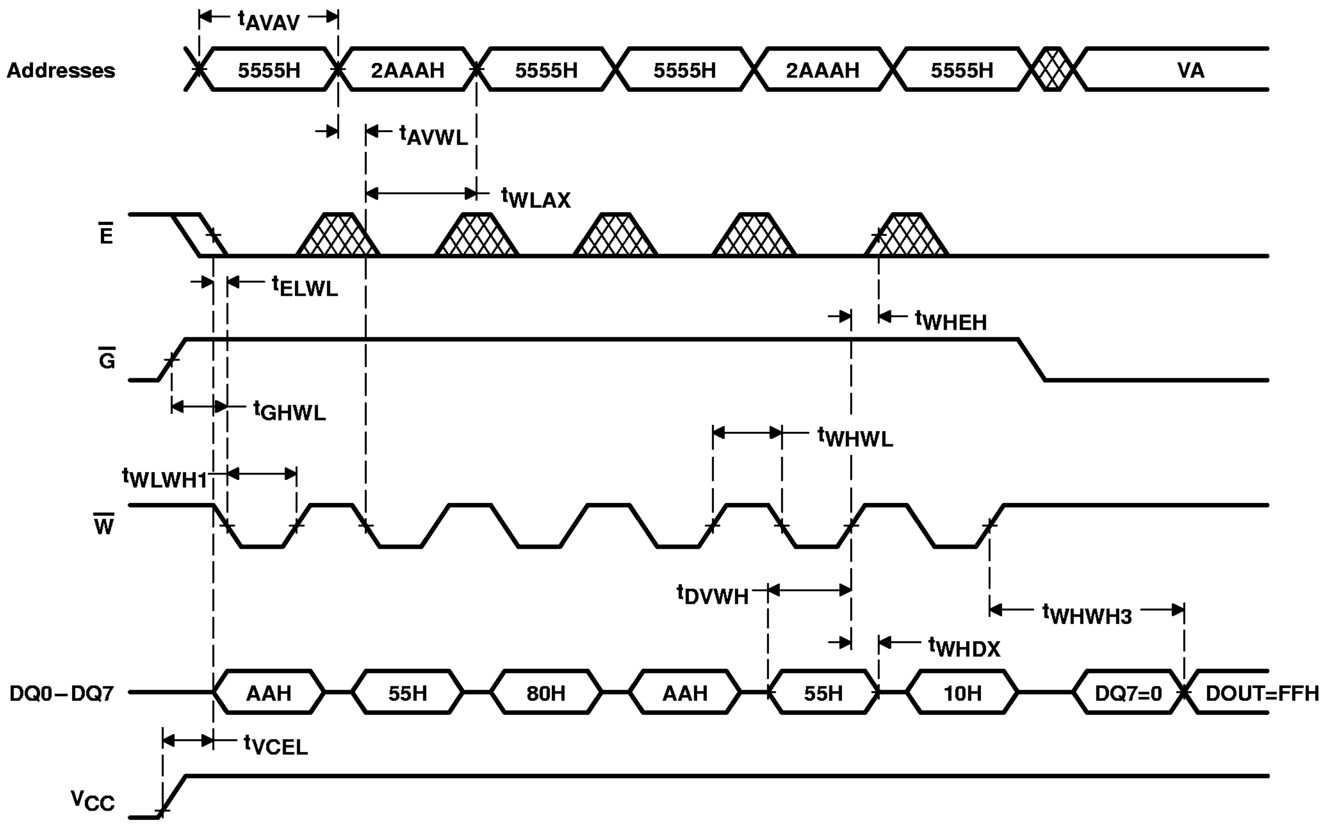


Figure 6. Chip-Erase Algorithm

PARAMETER MEASUREMENT INFORMATION



NOTE A: VA = any valid address.

Figure 7. AC Waveform for Chip-Erase Operation

PARAMETER MEASUREMENT INFORMATION

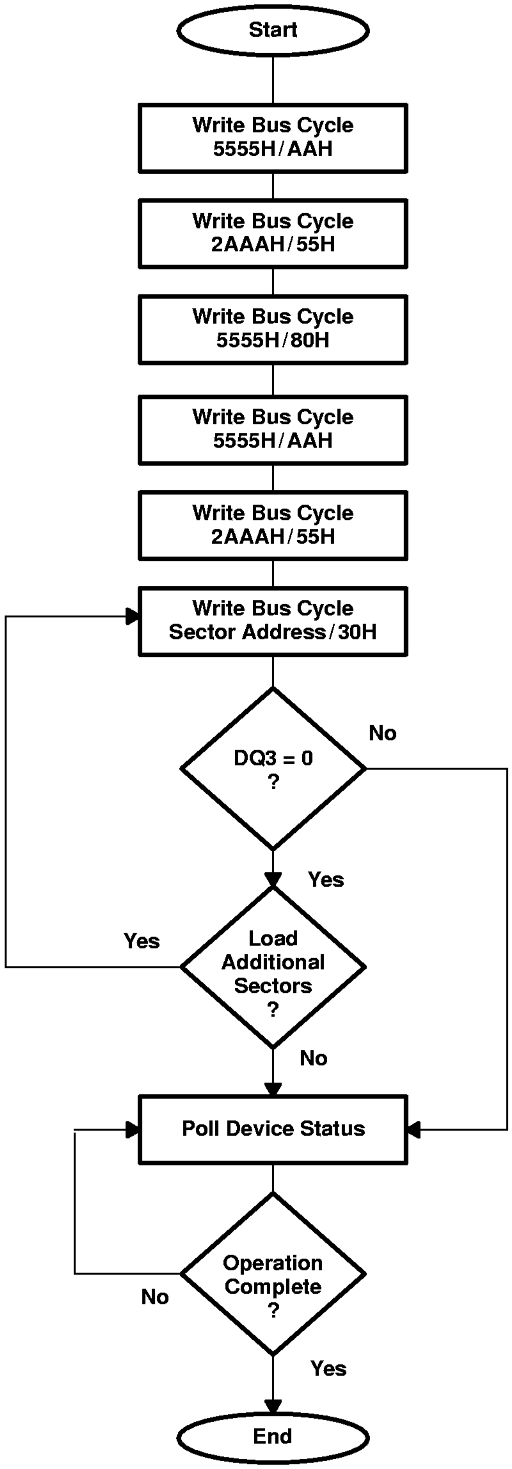
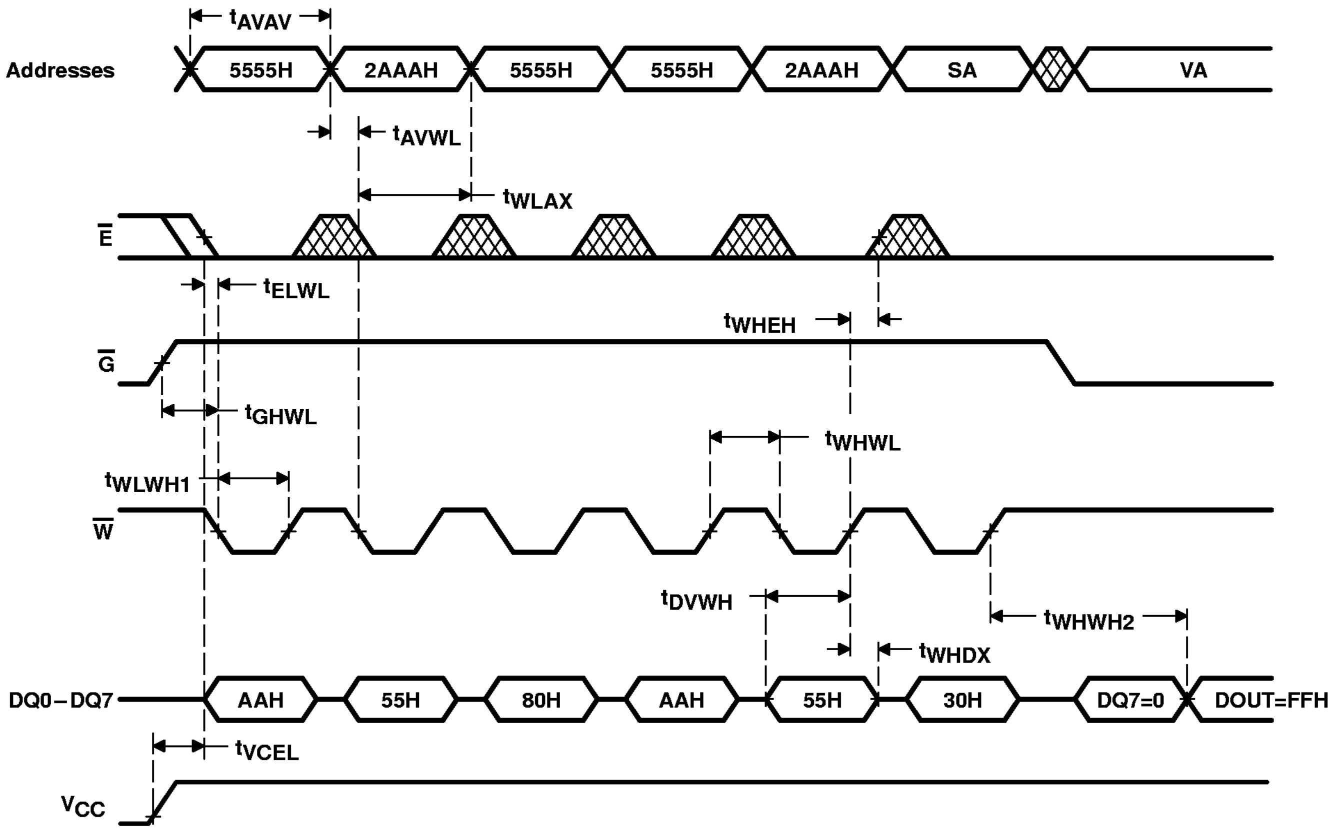


Figure 8. Sector-Erase Algorithm

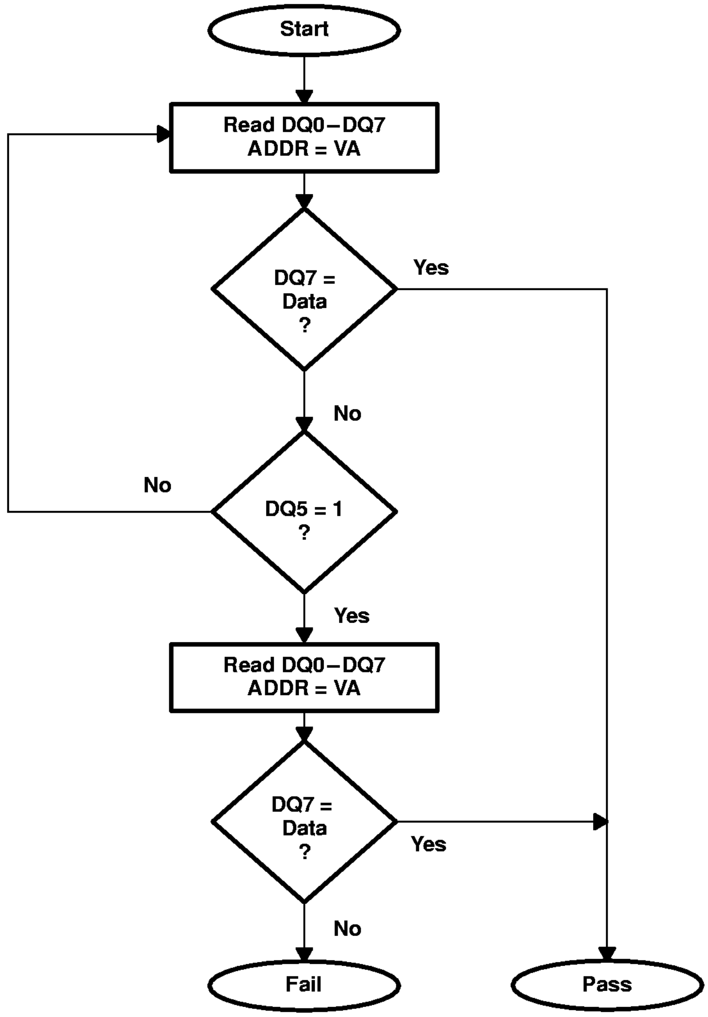
PARAMETER MEASUREMENT INFORMATION



NOTE A: SA = Sector address to be erased.

Figure 9. AC Waveform for Sector-Erase Operation

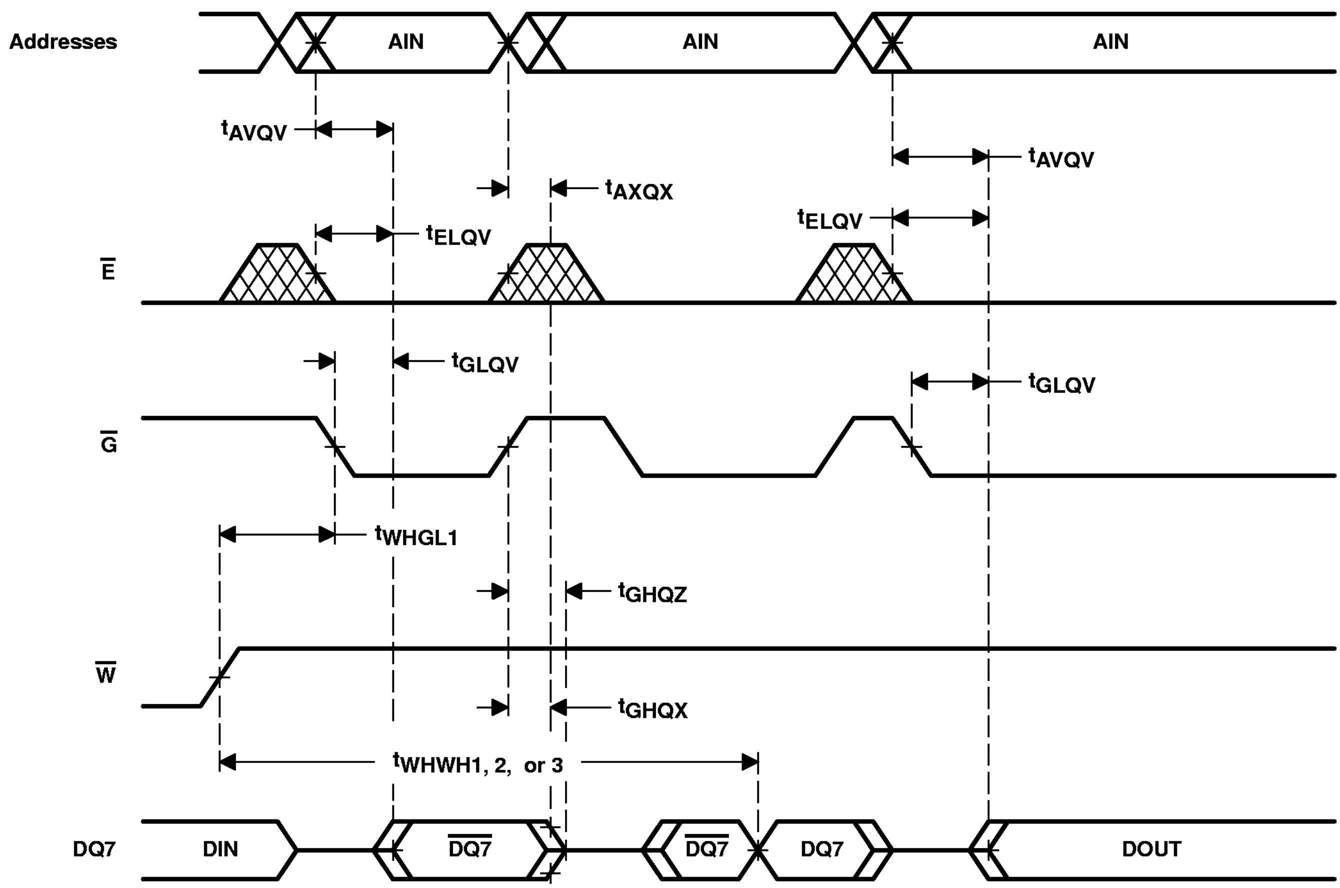
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Polling status bits DQ7 and DQ5 can change asynchronously. Read DQ7 after DQ5 changes states.
B. VA = Program address for byte programming
= Selected sector address for sector erase
= Any valid address for chip erase

Figure 10. Data-Polling Algorithm

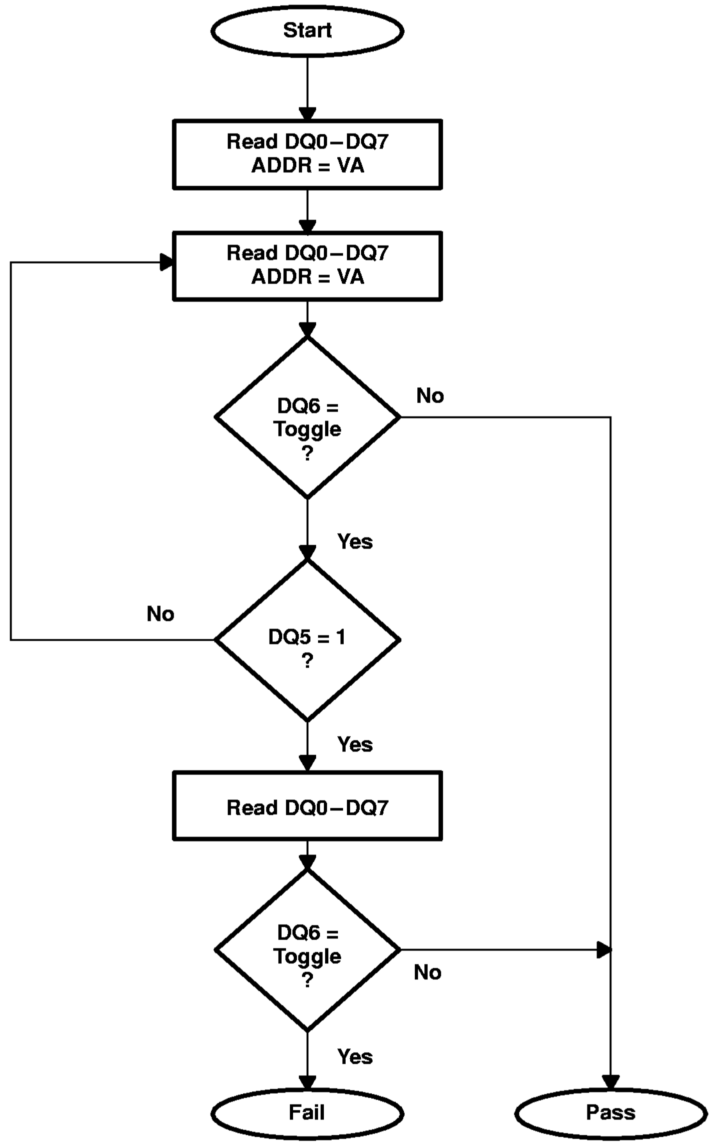
PARAMETER MEASUREMENT INFORMATION



NOTES: A. DIN = Last command data written to the device
B. $\overline{DQ7}$ = Complement of data written to DQ7
C. DOUT = Valid data output
D. AIN = Valid address for byte-program, sectorr-erase, or chip-erase operation

Figure 11. AC Waveform for Data-Polling Operation

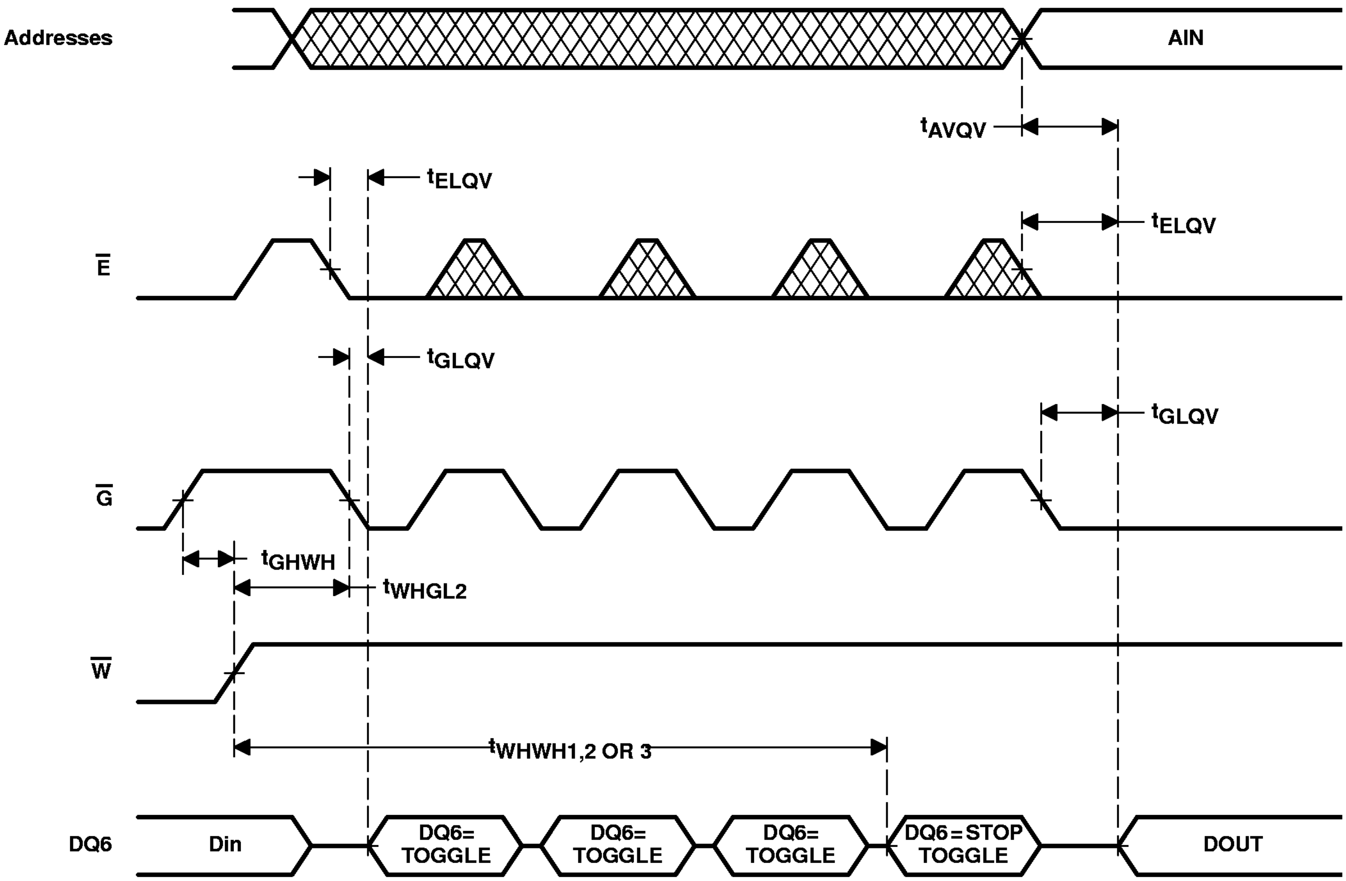
PARAMETER MEASUREMENT INFORMATION



NOTE A: Polling status bits DQ6 and DQ5 can change asynchronously.
Read DQ6 after DQ5 changes states.

Figure 12. Toggle-Bit Algorithm

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DIN = Last command data written to the device
B. DQ6 = Toggle bit output
C. DOUT = Valid data output
D. AIN = Valid address for byte-program, sector-erase, or chip-erase operation

Figure 13. AC Waveform for Toggle-Bit Operation

PARAMETER MEASUREMENT INFORMATION

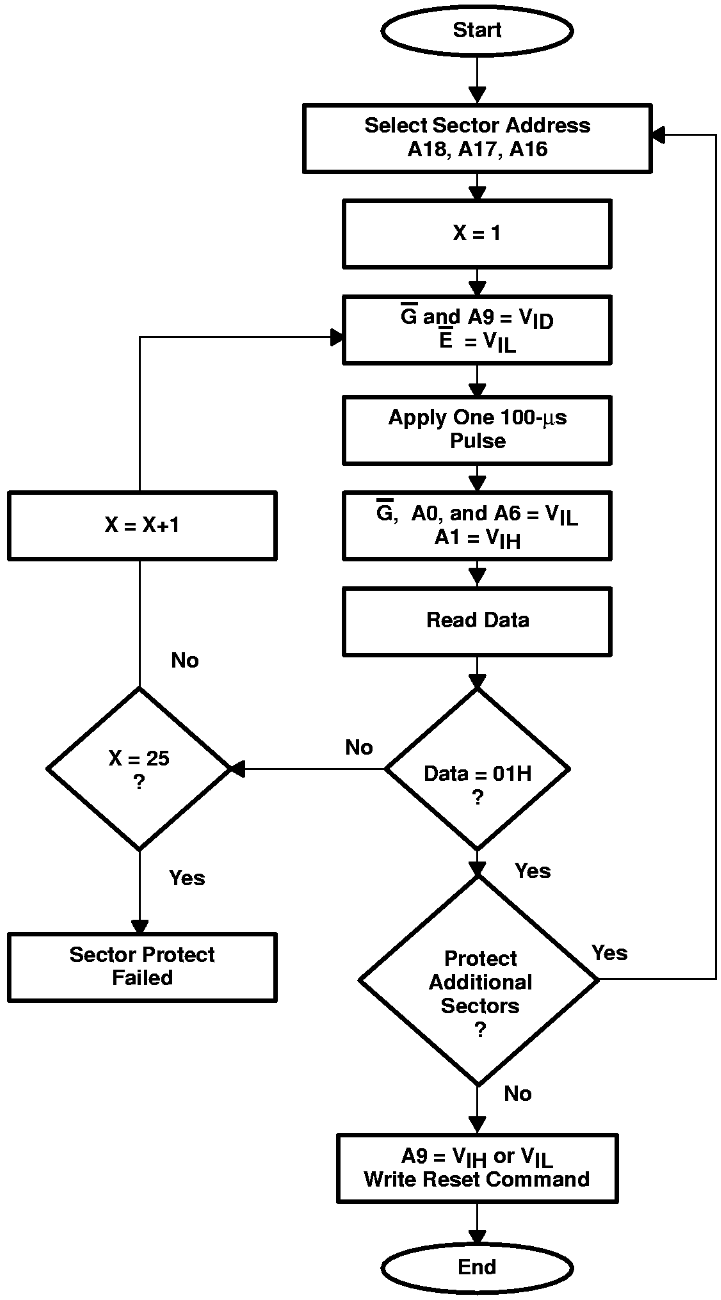
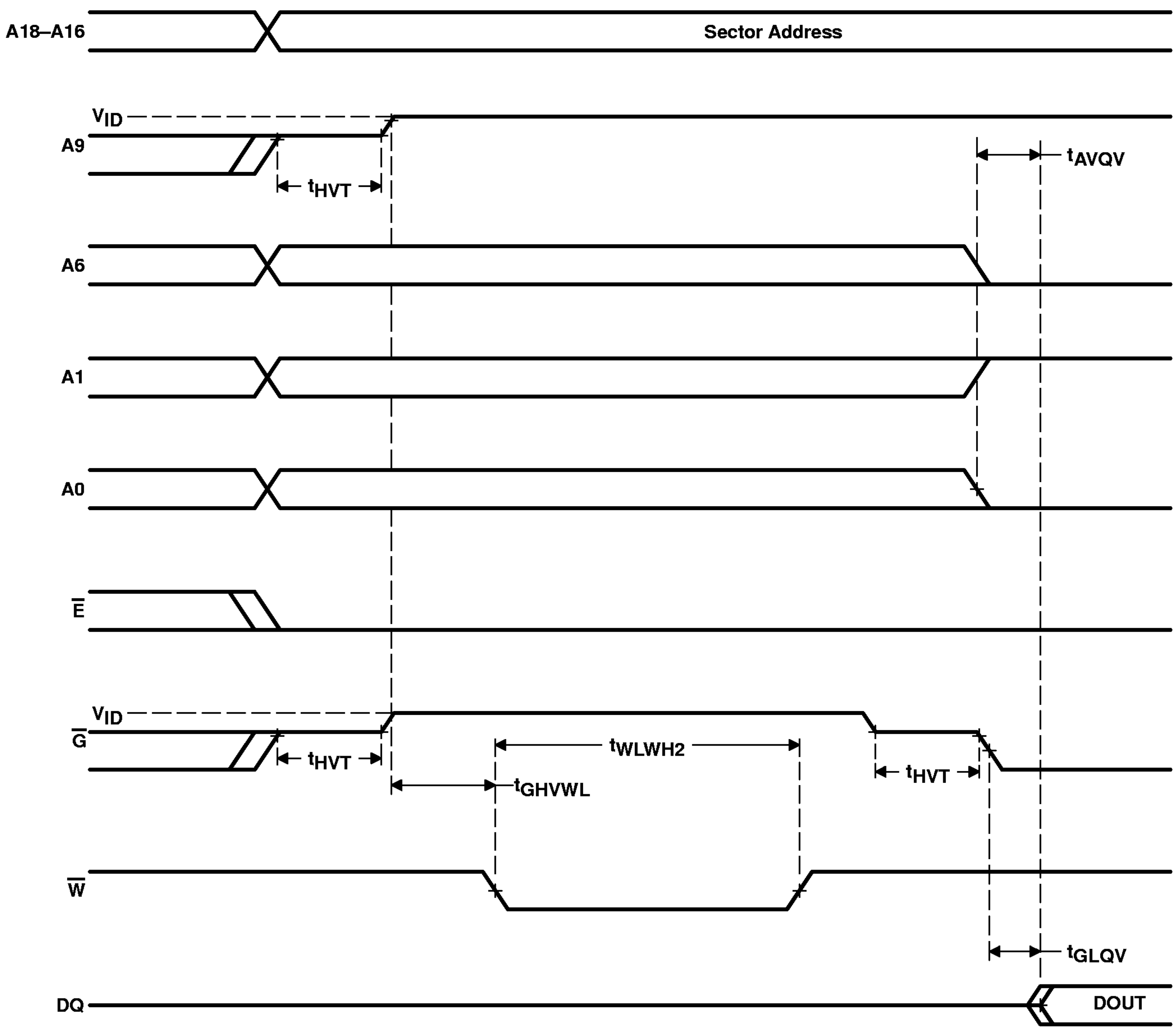


Figure 14. Sector-Protect Algorithm

PARAMETER MEASUREMENT INFORMATION



NOTE A: DOUT = 00H if selected sector is not protected,
01H if the sector is protected

Figure 15. AC Waveform for Sector-Protect Operation

PARAMETER MEASUREMENT INFORMATION

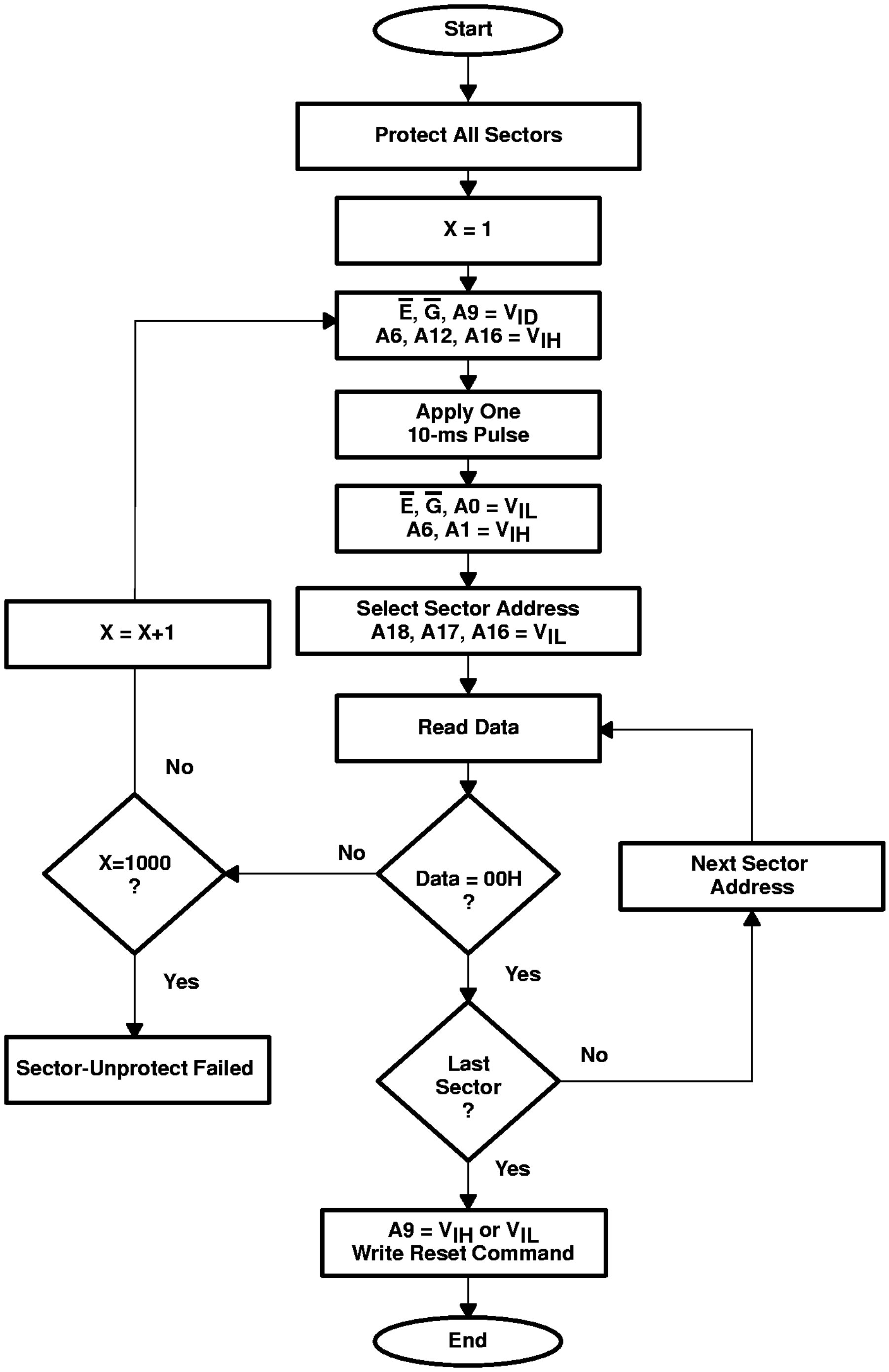
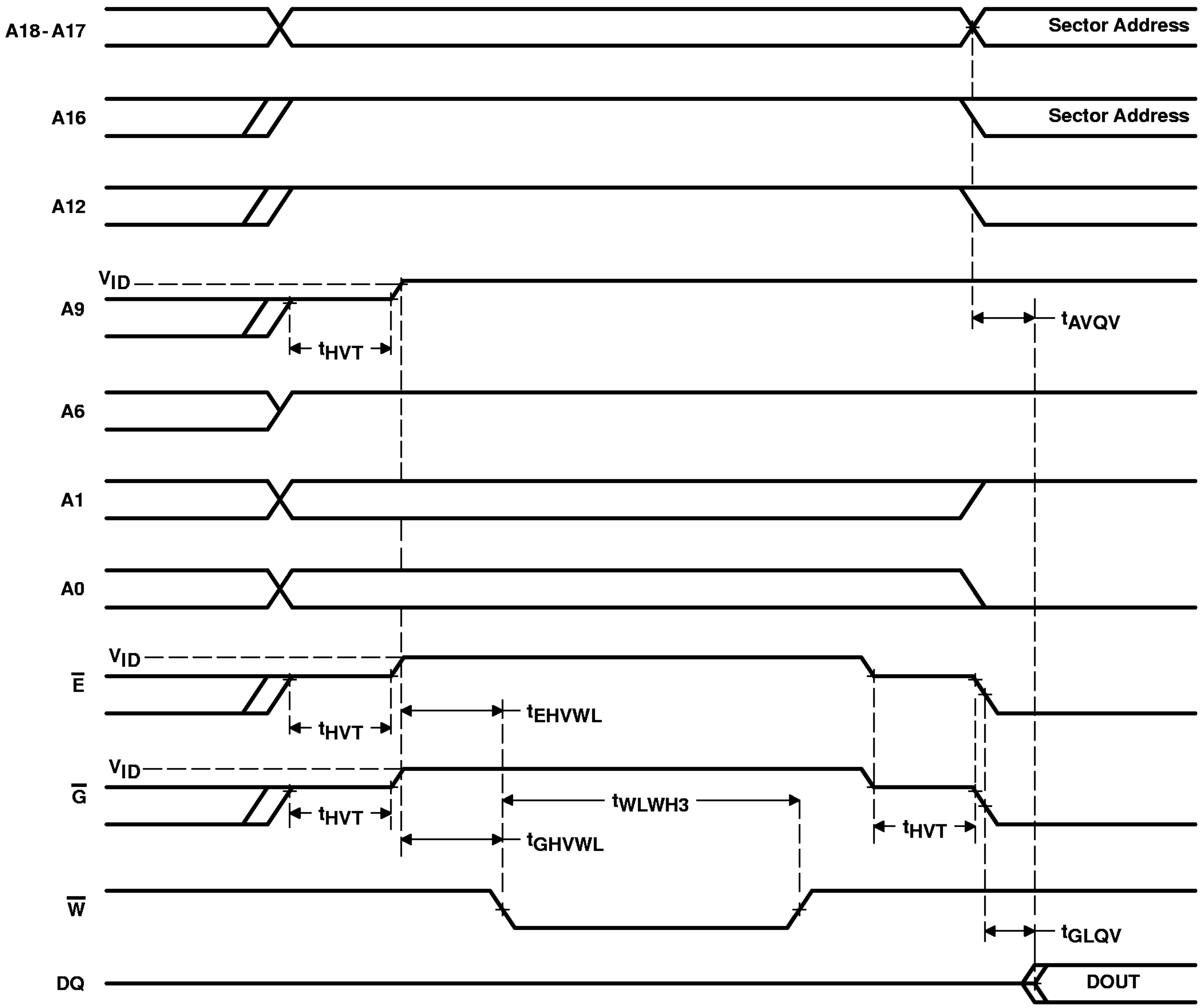


Figure 16. Sector-Unprotect Algorithm

PARAMETER MEASUREMENT INFORMATION

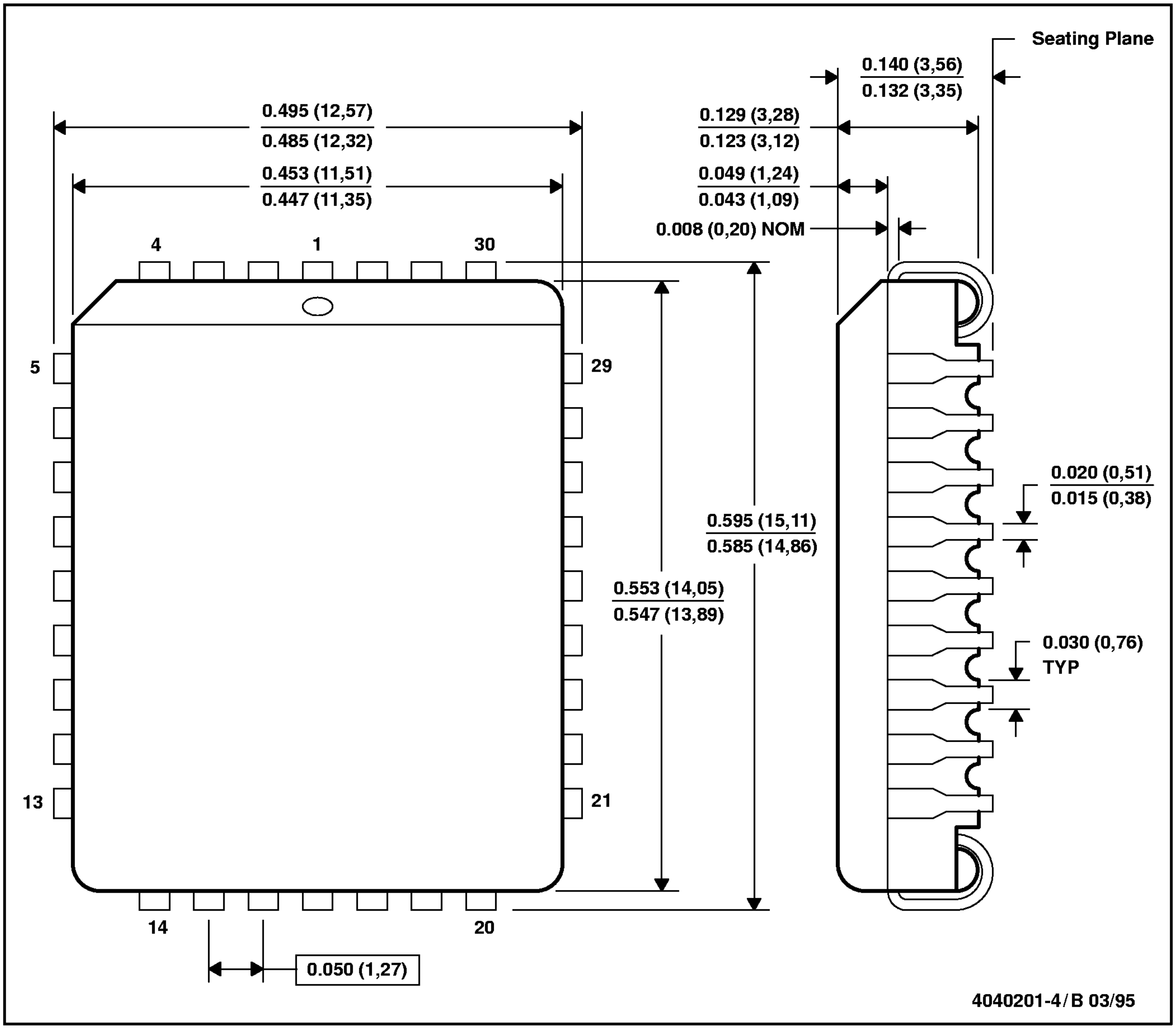


NOTE A: DOUT = 00H if selected sector is not protected,
01H if the sector is protected

Figure 17. AC Waveform for Sector-Unprotect Operation

MECHANICAL DATA

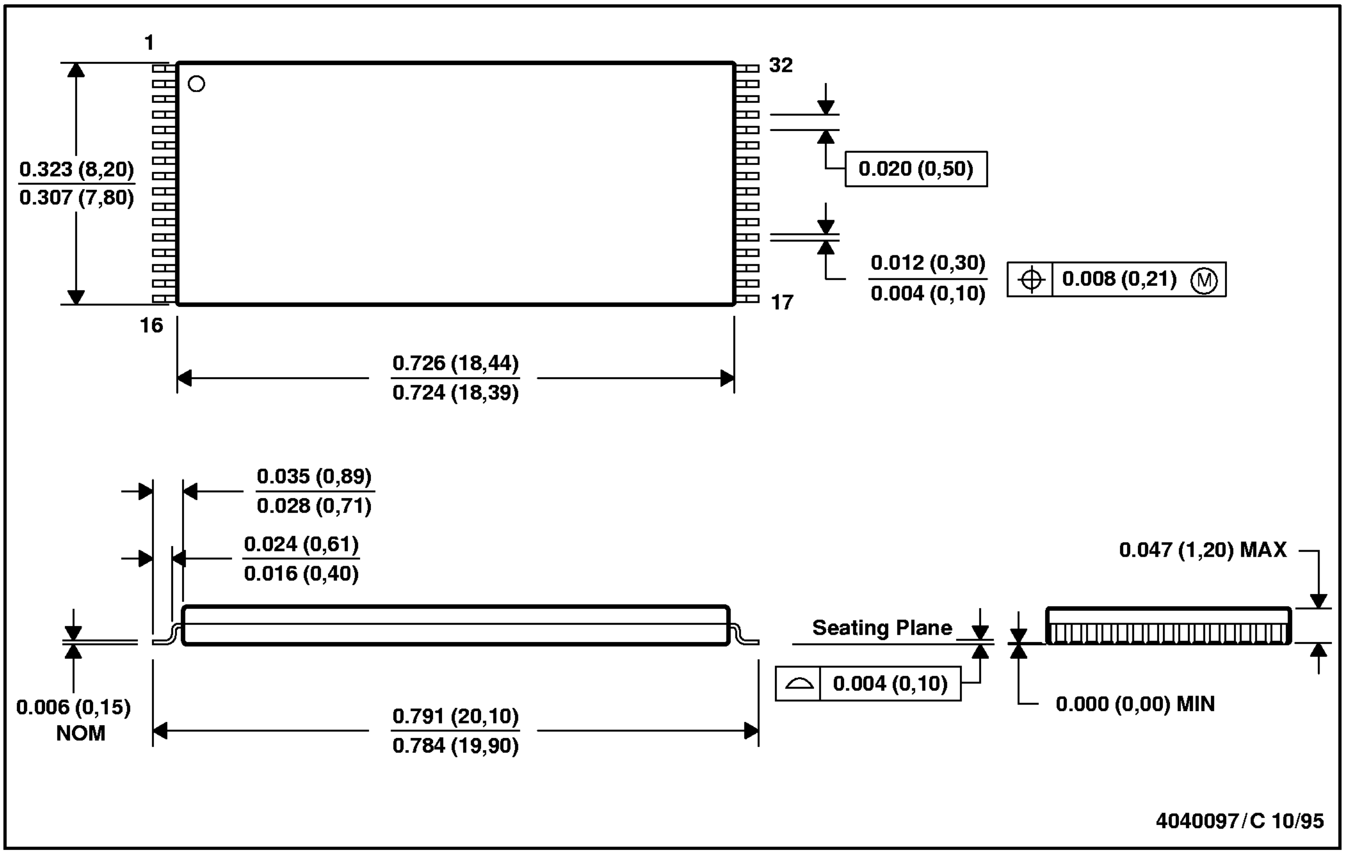
FM (R-PQCC-J32) **PLASTIC J-LEADED CHIP CARRIER**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

MECHANICAL DATA

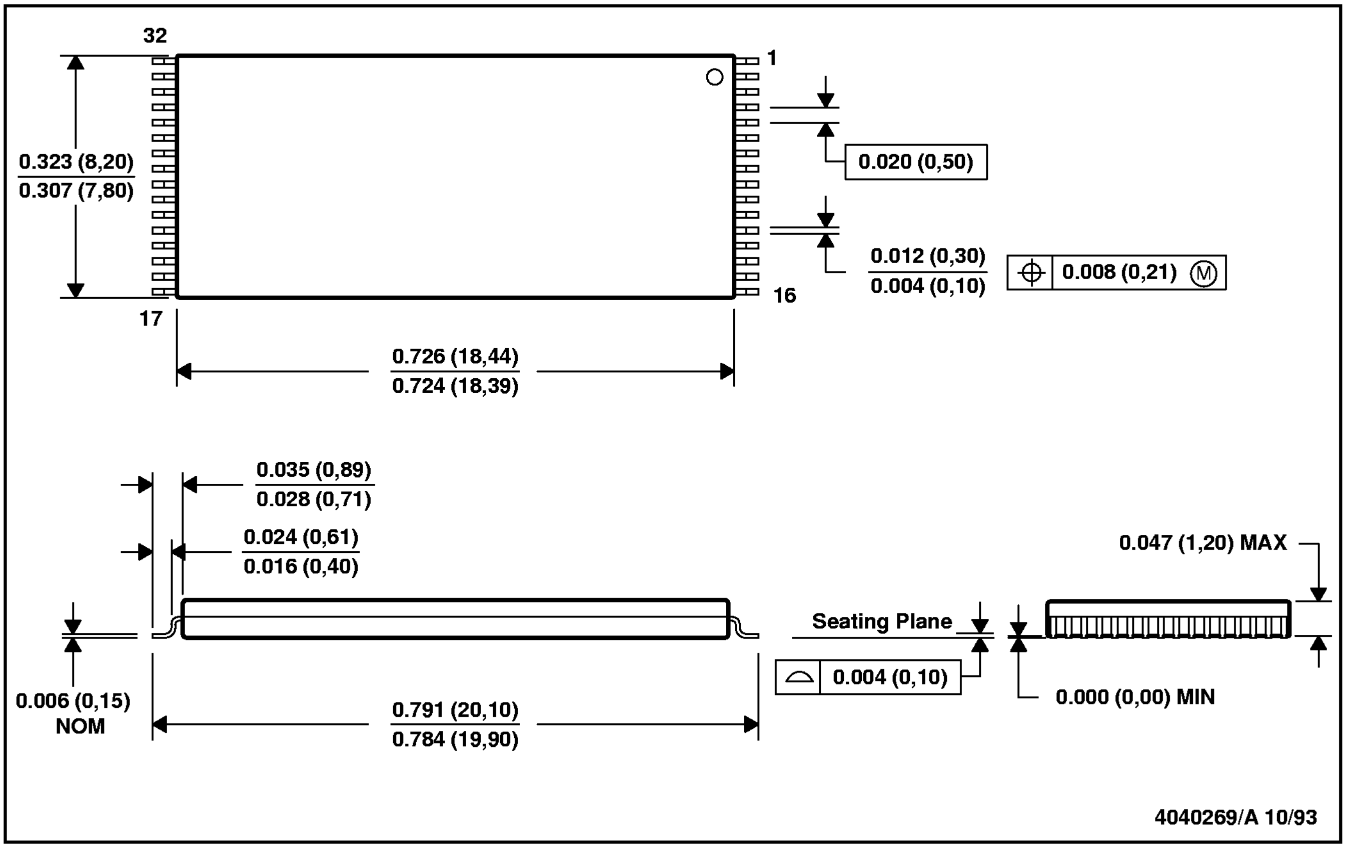
DD (R-PDSO-G32) **THIN SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

MECHANICAL DATA

DU (R-PDSO-G32) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is a reverse pin configuration to the DD package.