MOTOROLA

MC74AC398
MC74ACT398
MC74AC399
MC74ACT399

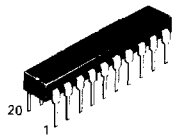
Product Preview

Quad 2-Port Register

QUAD 2-PORT REGISTER

The MC74AC398/74ACT398 and MC74AC399/74ACT399 are the logical equivalents of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flop on the rising edge of the clock. The MC74AC399/74ACT399 is the 16-pin version of the MC74AC398/74ACT398, with only the Q outputs of the flip-flops available.

- Select Inputs from Two Data Sources
- Fully Positive Edge-Triggered Operation
- Both True and Complement Outputs — MC74AC398/74ACT398
- Outputs Source/Sink 24 mA
- 'ACT398 and 'ACT399 Have TTL Compatible Inputs



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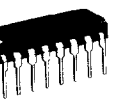
CASE 738-03
PLASTIC

N SUFFIX
CASE 648-08
PLASTIC



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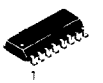

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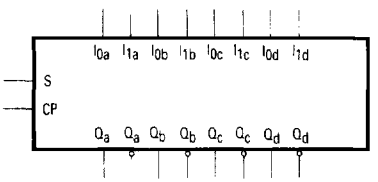
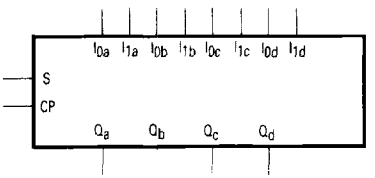
LOGIC SYMBOL

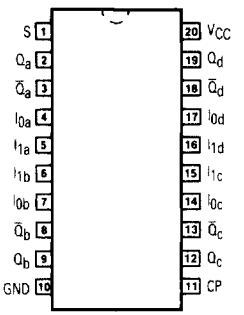
MC74AC398/74ACT398



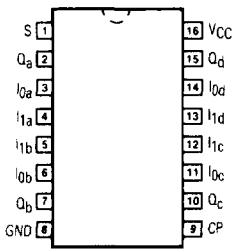
MC74AC399/74ACT399



MC74AC398/74ACT398



MC74AC399/74ACT399



PIN NAMES

S	Common Select Input
CP	Clock Pulse
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
Q_a–Q_d	Register True Outputs
$\overline{Q}_a$–$\overline{Q}_d$	Register Complementary Outputs (MC74AC398/74ACT398)

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FUNCTIONAL DESCRIPTION

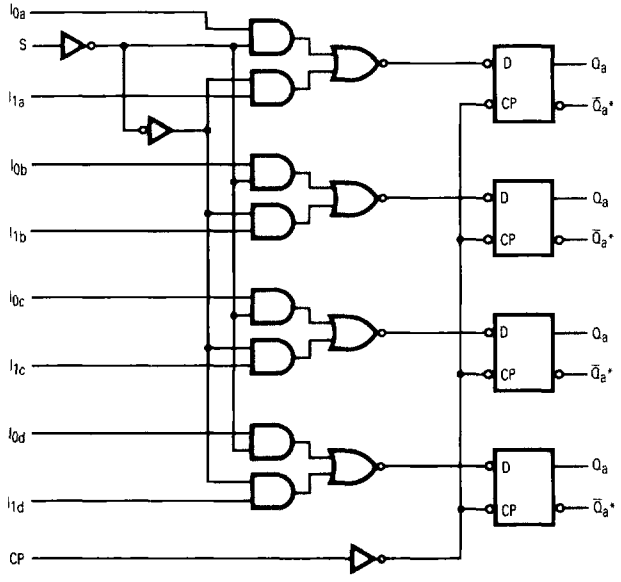
The MC74AC398/74ACT398 and MC74AC399/74ACT399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The MC74AC398/74ACT398 has both Q and $\overline{Q}$ outputs.

FUNCTION TABLE

Inputs				Outputs	
S	I_0	I_1	CP	Q	$\overline{Q}$*
L	L	X	⎍	L	H
L	H	X	⎍	H	L
H	X	L	⎍	L	H
H	X	H	⎍	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⎍ = LOW-to-HIGH Clock Transition
* = MC74AC398/74ACT398 only

LOGIC DIAGRAM



*MC74AC398/74ACT398

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT398/399)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		180 160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or $\overline{Q}$	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or $\overline{Q}$	3.3 5.0		8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW I_n to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW I_n to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('398)	3.3 5.0	4.5 3.0			ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('399)	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW S to CP	3.3 5.0	−1.5 −1.0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Input Clock Frequency	5.0		160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}$	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}$	5.0		6.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW I_n to CP	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW I_n to CP	5.0	0			ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('398)	5.0	3.0			ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('399)	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW S to CP	5.0	1.0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	5.5			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

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