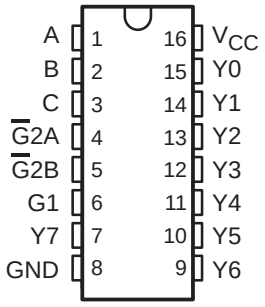
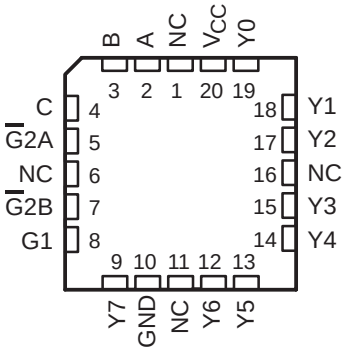
- **Inputs Are TTL-Voltage Compatible**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT138 . . . J OR W PACKAGE
SN74HCT138 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'HCT138 are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

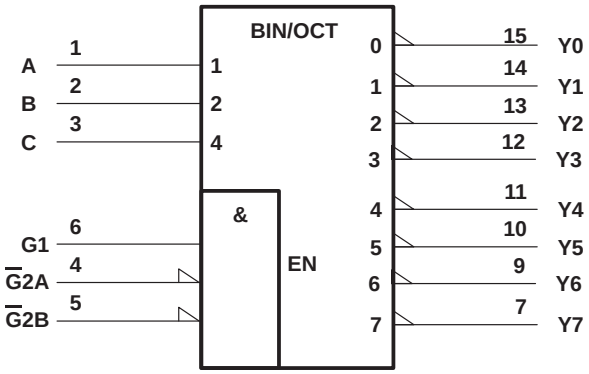
The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low ($\overline{G}$) and one active-high (G) enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

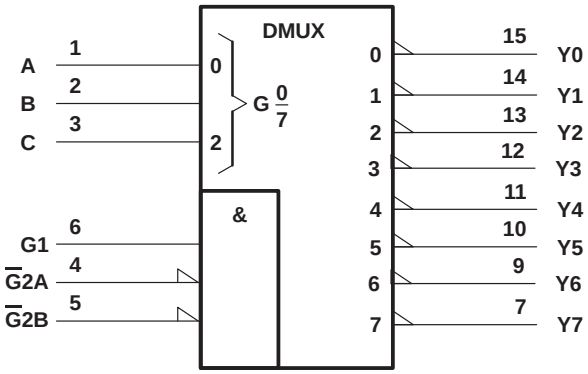
The SN54HCT138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT138 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

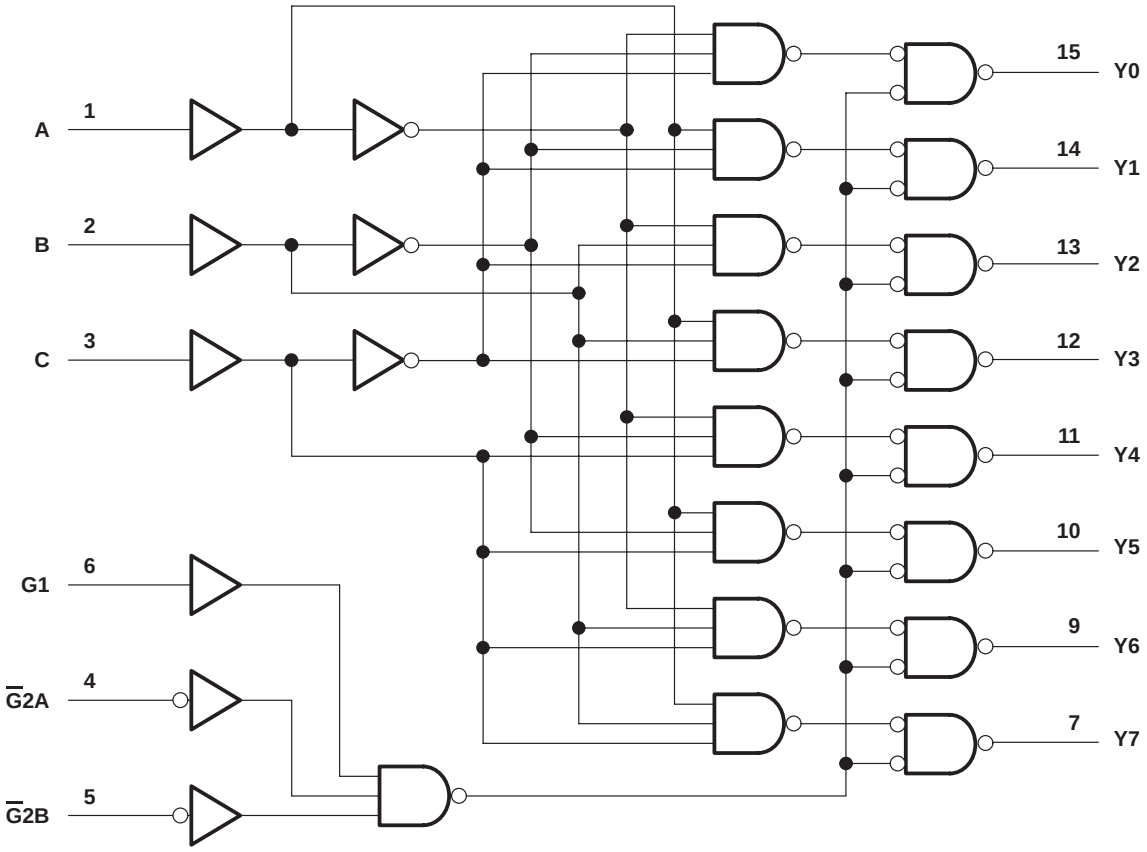
logic symbols (alternatives)†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HCT138			SN74HCT138			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT138		SN74HCT138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V			±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

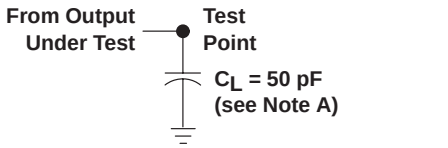
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT138		SN74HCT138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Any Y	4.5 V		23	36		54		45	ns
			5.5 V		17	32		49		34	
	Enable	Any Y	4.5 V		22	33		50		42	
			5.5 V		18	30		45		38	
t_t		Y	4.5 V		12	15		22		19	ns
			5.5 V		11	14		20		17	

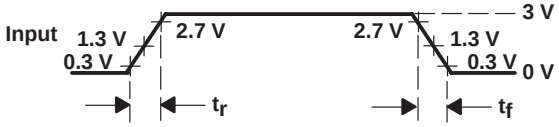
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	85	pF

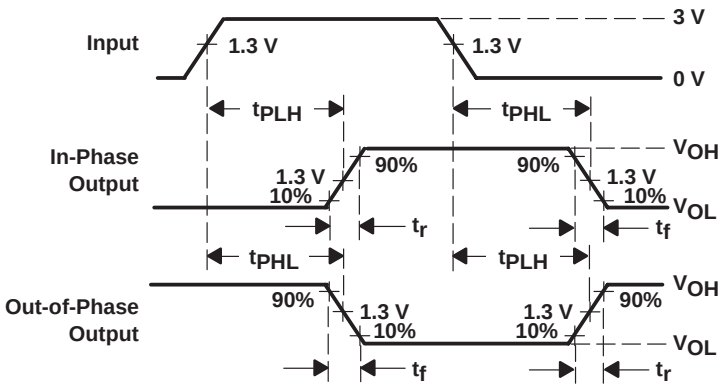
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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SN74HCT138, 3-Line To 8-Line Decoders/Demultiplexers

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54HCT138	SN74HCT138
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	CMOS	CMOS
Output Drive (mA)		-4/4
Output	2S	2S
From	3	3
To	8	8

FEATURES

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- Inputs Are TTL-Voltage Compatible
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- Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception
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DESCRIPTION

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TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74hct138.pdf (95 KB,Rev.C) (Updated: 05/01/1997)

APPLICATION NOTES

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View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- SN54/74HCT CMOS Logic Family Applications and Restrictions (SCLA011 - Updated: 05/01/1996)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74HCT138D	SOP (D)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HCT138N	PDIP (N)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HCT138PWR	TSSOP (PW)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74HCT138D	ACTIVE	SOP (D) | 16	-40 TO 85	View Contents	1KU | 0.22	40	N/A*	2000 | 03 Oct	2 WKS	Avnet | AMERICA	>1k	BUY NOW
								280 | 09 Oct		DigiKey | AMERICA	>1k	BUY NOW
								2000 | 22 Oct				
SN74HCT138DR	ACTIVE	SOP (D) | 16	-40 TO 85	View Contents	1KU | 0.22	2500	N/A*		6 WKS	Avnet | AMERICA	>1k	BUY NOW
SN74HCT138N	ACTIVE	PDIP (N) | 16	-40 TO 85	View Contents	1KU | 0.22	25	N/A*	>10k | 07 Oct	3 WKS	Avnet | AMERICA	>1k	BUY NOW
								2000 | 28 Oct				
SN74HCT138N3	OBSOLETE	PDIP (N) | 16	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74HCT138NSR	ACTIVE	SOP (NS) | 16		View Contents	1KU | 0.25	2000	N/A*		6 WKS			
SN74HCT138PWLE	OBSOLETE	TSSOP (PW) | 16	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74HCT138PWR	ACTIVE	TSSOP (PW) | 16	-40 TO 85	View Contents	1KU | 0.22	2000	N/A*	2000 | 19 Sep	2 WKS			

Table Data Updated on: 9/26/2002
