

Document Title

256Kx36 & 512Kx18-Bit Flow Through NtRAM™

Revision History

| <u>Rev. No.</u> | <u>History</u> | <u>Draft Date</u> | <u>Remark</u> |
|------------------------|--|--------------------------|----------------------|
| 0.0 | 1. Initial document. | April. 09. 1998 | Preliminary |
| 0.1 | Modify from $\overline{\text{ADV}}$ to ADV at timing. Add the Trade Mark(NtRAM™) | June. 02. 1998 | Preliminary |
| 0.2 | 1. Changed tCD from 8.0ns to 8.5ns at -8 2. Changed tCYC from 13.0ns to 12.0ns at -10 3. Changed DC condition at Icc and parameters Icc ; from 240mA to 260mA at -10, ISB1 ; from 10mA to 30mA, ISB2 ; from 10mA to 30mA. | Sep. 09. 1998 | Preliminary |

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



256Kx36 & 512Kx18-Bit Flow Through NtRAM™

FEATURES

- 3.3V ±5% Power Supply.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 100-TQFP-1420A Package.

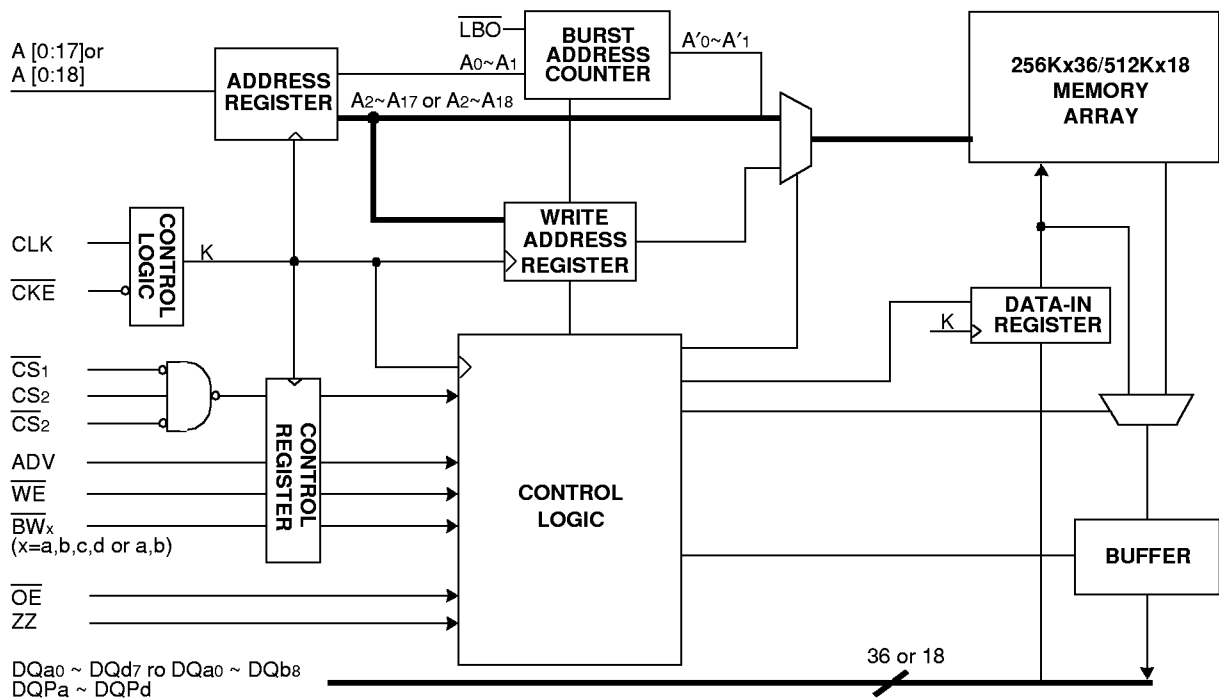
GENERAL DESCRIPTION

The KM736V847 and KM718V947 are 9,437,184-bit Synchronous Static SRAMs. The NtRAM™, or No Turnaround Random Access Memory utilizes all bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low". Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. For read cycles, Flow-Through SRAM allows output data to simply flow freely from the memory array. The KM736V847 and KM718V947 are implemented with SAMSUNG's high performance CMOS technology and is available in 100pin TQFP packages. Multiple power and ground pins minimize ground bounce.

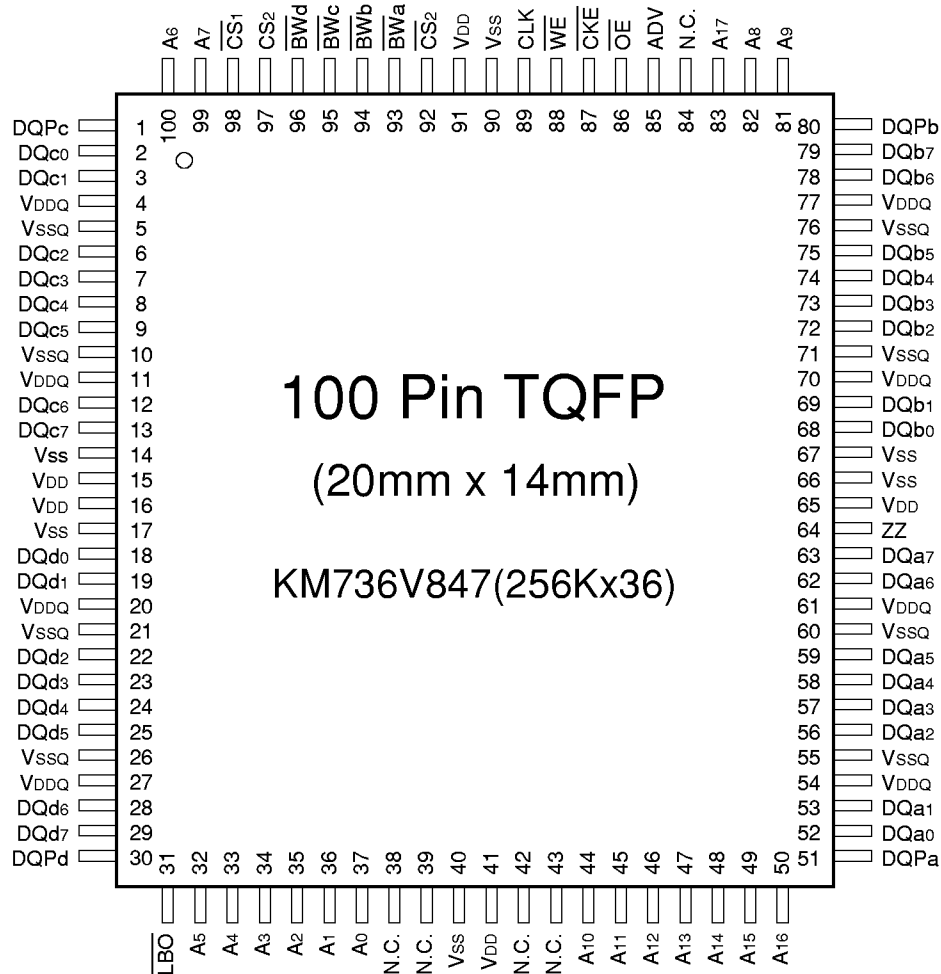
FAST ACCESS TIMES

| Parameter | Symbol | -8 | -9 | -10 | Unit |
|---------------------------|------------------|-----|-----|------|------|
| Cycle Time | t _{CYC} | 10 | 12 | 12 | ns |
| Clock Access Time | t _{CD} | 8.5 | 9.0 | 10.0 | ns |
| Output Enable Access Time | t _{OE} | 3.5 | 3.5 | 3.5 | ns |

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



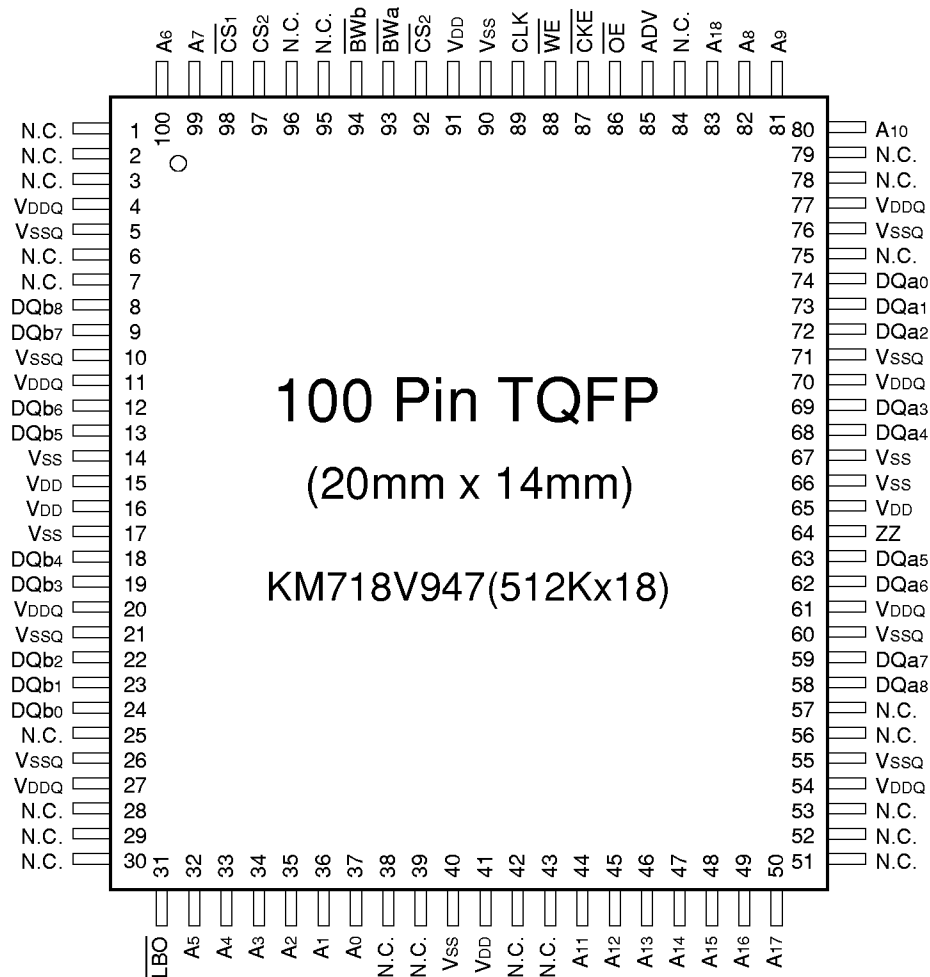
PIN NAME

| SYMBOL | PIN NAME | TQFP PIN NO. | SYMBOL | PIN NAME | TQFP PIN NO. |
|----------|--------------------------|--|---------|-----------------------------|-------------------------|
| A0 - A17 | Address Inputs | 32,33,34,35,36,37, 44,45,46,47,48,49, 50,81,82,83,99,100 | VDD | Power Supply(+3.3V) | 15,16,41,65,91 |
| | | | VSS | Ground | 14,17,40,66,67,90 |
| | | | N.C. | No Connect | 38,39,42,43,84 |
| ADV | Address Advance/Load | 85 | | | |
| WE | Read/Write Control Input | 88 | DQa0~a7 | Data Inputs/Outputs | 52,53,56,57,58,59,62,63 |
| CLK | Clock | 89 | DQb0~b7 | | 68,69,72,73,74,75,78,79 |
| CKE | Clock Enable | 87 | DQc0~c7 | | 2,3,6,7,8,9,12,13 |
| CS1 | Chip Select | 98 | DQd0~d7 | | 18,19,22,23,24,25,28,29 |
| CS2 | Chip Select | 97 | DQPa~Pd | | 51,80,1,30 |
| CS2 | Chip Select | 92 | | | |
| BWx | Byte Write Inputs | 93,94,95,96 | VDDQ | Output Power Supply (+3.3V) | 4,11,20,27,54,61,70,77 |
| OE | Output Enable | 86 | VSSQ | Output Ground | 5,10,21,26,55,60,71,76 |
| ZZ | Power Sleep Mode | 64 | | | |
| LBO | Burst Mode Control | 31 | | | |

NOTE : 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.
2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.



PIN CONFIGURATION(TOP VIEW)



PIN NAME

| SYMBOL | PIN NAME | TQFP PIN NO. | SYMBOL | PIN NAME | TQFP PIN NO. |
|----------|--------------------------|---|---------|-----------------------------|--|
| A0 - A18 | Address Inputs | 32,33,34,35,36,37, 44,45,46,47,48,49,50, 80,81,82,83,99,100 | VDD | Power Supply(+3.3V) | 15,16,41,65,91 |
| | | | VSS | Ground | 14,17,40,66,67,90 |
| | | | N.C. | No Connect | 1,2,3,6,7,25,28,29,30, 38,39,42,43,51,52,53, 56,57,75,78,79,84,95,96 |
| ADV | Address Advance/Load | 85 | | | |
| WE | Read/Write Control Input | 88 | DQa0~a8 | Data Inputs/Outputs | 8,9,12,13,18,19,22,23,24 |
| CLK | Clock | 89 | DQb0~b8 | | 58,59,62,63,68,69,72,73, 74 |
| CKE | Clock Enable | 87 | | | |
| CS1 | Chip Select | 98 | VDDQ | Output Power Supply (+3.3V) | 4,11,20,27,54,61,70,77 |
| CS2 | Chip Select | 97 | VSSQ | Output Ground | 5,10,21,26,55,60,71,76 |
| CS2 | Chip Select | 92 | | | |
| BWx | Byte Write Inputs | 93,94 | | | |
| OE | Output Enable | 86 | | | |
| ZZ | Power Sleep Mode | 64 | | | |
| LBO | Burst Mode Control | 31 | | | |

NOTE : 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.
2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.



FUNCTION DESCRIPTION

The KM736V847 and KM718V947 are NtRAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of \overline{OE} , \overline{LBO} and \overline{ZZ}) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable(\overline{CKE}) pin allows the operation of the chip to be suspended as long as necessary. All synchronous inputs are ignored when \overline{CKE} is high and the internal device registers will hold their previous values.

When \overline{CKE} is active asserted, ADV is disasserted and all three chip enables($\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_2}$) are asserted, NtRAM™ latches external address and initiates a cycle.

Output Enable(\overline{OE}) can be used to disable the output at any given time.

Read operation is initiated when the following conditions are satisfied at the rising edge of clock, \overline{CKE} is asserted Low, all three chip enables($\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_2}$) are active, the write enable input signals \overline{WE} is deasserted high, and ADV is asserted Low. The address presented to the address inputs are latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data a propagate to the output buffers. After the first clock of read access the output buffers are controlled by \overline{OE} and the internal control logic. \overline{OE} must be driven Low in order for the device to drive out the requested data.

Write operation occurs when \overline{WE} is sampled Low at the rising edge of clock. $\overline{BW}[d:a]$ can be used for byte write operation. The Flow Through NtRAM™ uses a late write cycle to utilize 100% of the bandwidth.

At the first rising edge of clock, \overline{WE} and address are registered, and the data associated with that address is required one cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the \overline{LBO} pin. When this pin is Low, linear burst sequence is selected.

And this pin is High, interleaved burst sequence is selected.

During normal operation, \overline{ZZ} must be pulled LOW. When \overline{ZZ} is pulled HIGH, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When \overline{ZZ} returns to LOW, the SRAM normally operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, \overline{LBO} =High)

| \overline{LBO} PIN | HIGH | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | | A ₁ | A ₀ | A ₁ | A ₀ | A ₁ | A ₀ | A ₁ | A ₀ |
| | First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | ↓ | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| | ↓ | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| | Fourth Address | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

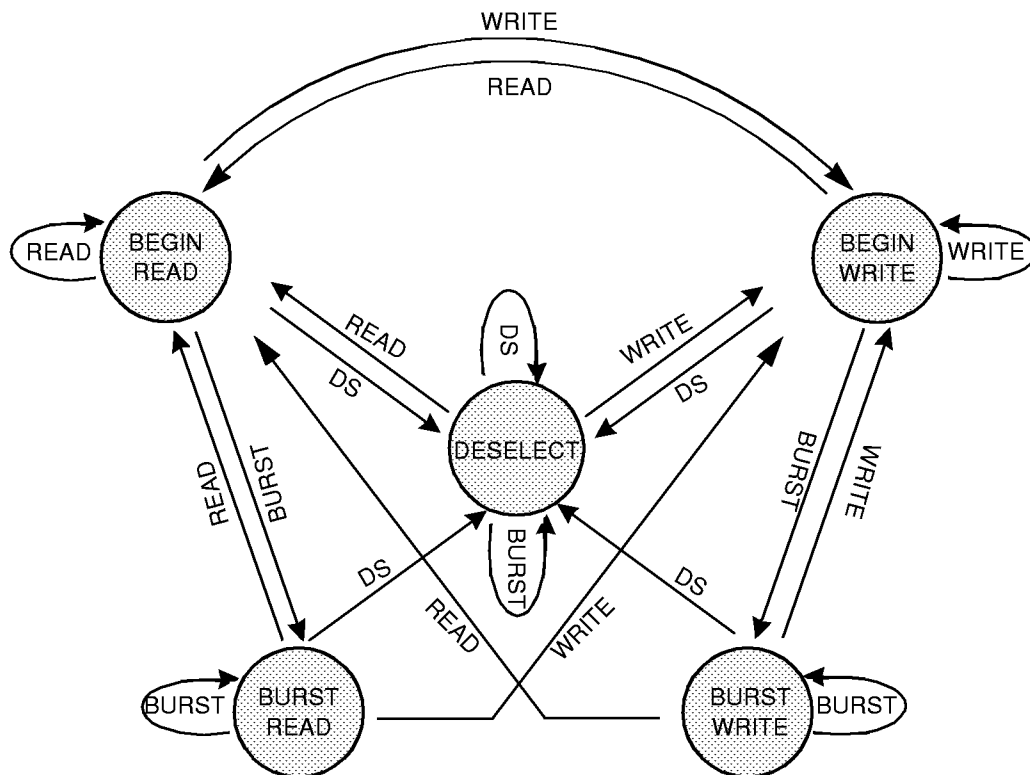
(Linear Burst, \overline{LBO} =Low)

| \overline{LBO} PIN | LOW | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | | A ₁ | A ₀ | A ₁ | A ₀ | A ₁ | A ₀ | A ₁ | A ₀ |
| | First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | ↓ | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| | ↓ | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| | Fourth Address | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

NOTE : 1. \overline{LBO} pin must be tied to High or Low, and Floating State must not be allowed.



STATE DIAGRAM FOR NtRAM™



| COMMAND | ACTION |
|---------|--|
| DS | DESELECT |
| READ | BEGIN READ |
| WRITE | BEGIN WRITE |
| BURST | BEGIN READ BEGIN WRITE CONTINUE DESELECT |

NOTE

1. An IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because $\overline{\text{CKE}}$ HIGH only blocks the clock (CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock (CLK)

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

| \overline{CS}_1 | \overline{CS}_2 | \overline{CS}_2 | ADV | \overline{WE} | \overline{BW}_x | \overline{OE} | \overline{CKE} | CLK | Address Accessed | Operation |
|-------------------|-------------------|-------------------|-----|-----------------|-------------------|-----------------|------------------|-----|------------------|----------------------------|
| H | X | X | L | X | X | X | L | ↑ | N/A | Not Selected |
| X | L | X | L | X | X | X | L | ↑ | N/A | Not Selected |
| X | X | H | L | X | X | X | L | ↑ | N/A | Not Selected |
| X | X | X | H | X | X | X | L | ↑ | N/A | Not Selected Continue |
| L | H | L | L | H | X | L | L | ↑ | External Address | Begin Burst Read Cycle |
| X | X | X | H | X | X | L | L | ↑ | Next Address | Continue Burst Read Cycle |
| L | H | L | L | H | X | H | L | ↑ | External Address | NOP/Dummy Read |
| X | X | X | H | X | X | H | L | ↑ | Next Address | Dummy Read |
| L | H | L | L | L | L | X | L | ↑ | External Address | Begin Burst Write Cycle |
| X | X | X | H | X | L | X | L | ↑ | Next Address | Continue Burst Write Cycle |
| L | H | L | L | L | H | X | L | ↑ | N/A | NOP/Write Abort |
| X | X | X | H | X | H | X | L | ↑ | Next Address | Write Abort |
| X | X | X | X | X | X | X | H | ↑ | Current Address | Ignore Clock |

- NOTE :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by (↑).
 3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
 4. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
 5. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE(x36)

| \overline{WE} | \overline{BW}_a | \overline{BW}_b | \overline{BW}_c | \overline{BW}_d | Operation |
|-----------------|-------------------|-------------------|-------------------|-------------------|-----------------|
| H | X | X | X | X | READ |
| L | L | H | H | H | WRITE BYTE a |
| L | H | L | H | H | WRITE BYTE b |
| L | H | H | L | H | WRITE BYTE c |
| L | H | H | H | L | WRITE BYTE d |
| L | L | L | L | L | WRITE ALL BYTES |
| L | H | H | H | H | WRITE ABORT/NOP |

WRITE TRUTH TABLE(x18)

| \overline{WE} | \overline{BW}_a | \overline{BW}_b | Operation |
|-----------------|-------------------|-------------------|-----------------|
| H | X | X | READ |
| L | L | H | WRITE BYTE a |
| L | H | L | WRITE BYTE b |
| L | L | L | WRITE ALL BYTES |
| L | H | H | WRITE ABORT/NOP |

- NOTE :** 1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

| Operation | ZZ | \overline{OE} | I/O Status |
|------------|----|-----------------|-------------|
| Sleep Mode | H | X | High-Z |
| Read | L | L | DQ |
| | L | H | High-Z |
| Write | L | X | Din, High-Z |
| Deselected | L | X | High-Z |

NOTE

1. X means "Don't Care".
2. For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
3. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
4. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

| Parameter | Symbol | Rating | Unit |
|--|--------|-------------|------|
| Voltage on VDD Supply Relative to VSS | VDD | -0.3 to 4.6 | V |
| Voltage on Any Other Pin Relative to VSS | VIN | -0.3 to 4.6 | V |
| Power Dissipation | Pd | 1.4 | W |
| Storage Temperature | TSTG | -65 to 150 | °C |
| Operating Temperature | TOPR | 0 to 70 | °C |
| Storage Temperature Range Under Bias | TBIAS | -10 to 85 | °C |

*NOTE : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS(0°C ≤ TA ≤ 70°C)

| Parameter | Symbol | Min | Typ. | Max | Unit |
|----------------|--------|-------|------|-------|------|
| Supply Voltage | VDD | 3.135 | 3.3 | 3.465 | V |
| | VDDQ | 3.135 | 3.3 | 3.465 | V |
| Ground | VSS | 0 | 0 | 0 | V |

*NOTE : VDD and VDDQ must be supplied with identical voltage levels.

CAPACITANCE*(TA=25°C, f=1MHz)

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|--------------------|--------|----------------|-----|-----|------|
| Input Capacitance | CIN | VIN=0V | - | 6 | pF |
| Output Capacitance | COUT | VOUT=0V | - | 8 | pF |

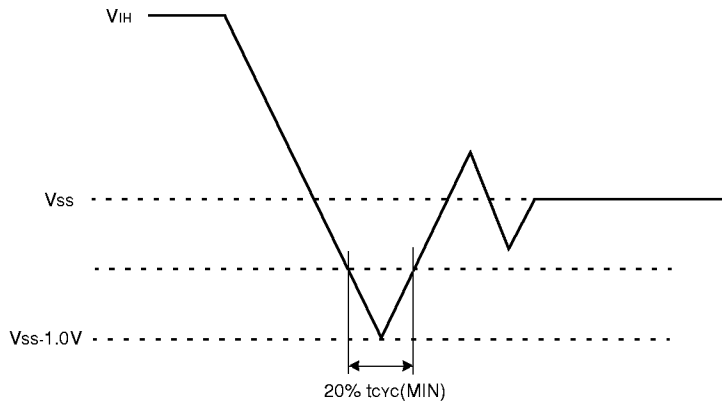
*NOTE : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=3.3V \pm 5\%$ $T_A=0^\circ C$ to $+70^\circ C$)

| Parameter | Symbol | Test Conditions | Min | Max | Unit | Notes | |
|----------------------------------|--|--|-------|------------------------|---------|-------|-----|
| Input Leakage Current(except ZZ) | IIL | $V_{DD}=\text{Max}$; $V_{IN}=V_{SS}$ to V_{DD} | -2 | +2 | μA | | |
| Output Leakage Current | IOL | Output Disabled, | -2 | +2 | μA | | |
| Operating Current | I _{CC} | Device Selected, I _{OUT} =0mA, ZZ≤V _{IL} , Cycle Time ≥ t _{CYC} Min | -8 | - | 300 | mA | 1,2 |
| | | | -9 | - | 260 | | |
| | | | -10 | - | 240 | | |
| Standby Current | I _{SB} | Device deselected, I _{OUT} =0mA, ZZ≤V _{IL} , f=Max, All Inputs≤0.2V or ≥ V _{DD} -0.2V | -8 | - | 60 | mA | |
| | | | -9 | - | 50 | | |
| | | | -10 | - | 40 | | |
| | I _{SB1} | Device deselected, I _{OUT} =0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V _{DD} -0.2V or 0.2V) | - | - | 30 | mA | |
| I _{SB2} | Device deselected, I _{OUT} =0mA, ZZ≥V _{DD} -0.2V, f=Max, All Inputs≤V _{IL} or ≥V _{IH} | - | - | 30 | mA | | |
| Output Low Voltage | V _{OL} | I _{OL} =8.0mA | - | 0.4 | V | | |
| Output High Voltage | V _{OH} | I _{OH} =-4.0mA | 2.4 | - | V | | |
| Input Low Voltage | V _{IL} | | -0.3* | 0.8 | V | | |
| Input High Voltage | V _{IH} | | 2.0 | V _{DD} +0.3** | V | 3 | |

NOTES;

1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DD}+0.3V.



TEST CONDITIONS

(T_A=0 to 70°C, V_{DD}=3.3V±5% unless otherwise specified)

| Parameter | Value |
|---|------------|
| Input Pulse Level | 0 to 3.0V |
| Input Rise and Fall Time(Measured at 20% and 80%) | 2ns |
| Input and Output Timing Reference Levels | 1.5v |
| Output Load | See Fig. 1 |



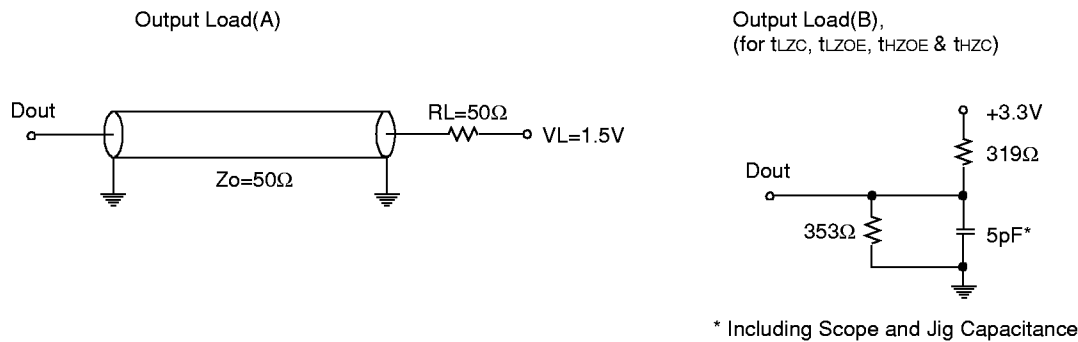


Fig. 1

AC TIMING CHARACTERISTICS
(VDD=3.3V±5%, TA=0 to 70°C)

| Parameter | Symbol | -8 | | -9 | | -10 | | Unit |
|---|-------------------|-----|-----|-----|-----|-----|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| Cycle Time | t _{CYC} | 10 | - | 12 | - | 12 | - | ns |
| Clock Access Time | t _{CD} | - | 8.5 | - | 9.0 | - | 10 | ns |
| Output Enable to Data Valid | t _{OE} | - | 3.5 | - | 3.5 | - | 3.5 | ns |
| Clock High to Output Low-Z | t _{lZC} | 2.5 | - | 2.5 | - | 2.5 | - | ns |
| Output Hold from Clock High | t _{OH} | 2.5 | - | 2.5 | - | 2.5 | - | ns |
| Output Enable Low to Output Low-Z | t _{lZOE} | 0 | - | 0 | - | 0 | - | ns |
| Output Enable High to Output High-Z | t _{hZOE} | - | 3.5 | - | 3.5 | - | 4.0 | ns |
| Clock High to Output High-Z | t _{hZC} | - | 5.0 | - | 5.0 | - | 6.0 | ns |
| Clock High Pulse Width | t _{CH} | 3.0 | - | 3.0 | - | 3.0 | - | ns |
| Clock Low Pulse Width | t _{CL} | 3.0 | - | 3.0 | - | 3.0 | - | ns |
| Address Setup to Clock High | t _{AS} | 2.0 | - | 2.0 | - | 2.0 | - | ns |
| CKE Setup to Clock High | t _{CES} | 2.0 | - | 2.0 | - | 2.0 | - | ns |
| Data Setup to Clock High | t _{DS} | 2.0 | - | 2.0 | - | 2.0 | - | ns |
| Write Setup to Clock High (\overline{WE} , \overline{BWE}) | t _{WS} | 2.0 | - | 2.0 | - | 2.0 | - | ns |
| Address Advance Setup to Clock High | t _{ADVS} | 2.0 | - | 2.0 | - | 2.0 | - | ns |
| Chip Select Setup to Clock High | t _{CSS} | 2.0 | - | 2.0 | - | 2.0 | - | ns |
| Address Hold from Clock High | t _{AH} | 0.5 | - | 0.5 | - | 0.5 | - | ns |
| CKE Hold from Clock High | t _{CEH} | 0.5 | - | 0.5 | - | 0.5 | - | ns |
| Data Hold from Clock High | t _{DH} | 0.5 | - | 0.5 | - | 0.5 | - | ns |
| Write Hold from Clock High (\overline{WE} , \overline{BWE}) | t _{WH} | 0.5 | - | 0.5 | - | 0.5 | - | ns |
| Address Advance Hold from Clock High | t _{ADVH} | 0.5 | - | 0.5 | - | 0.5 | - | ns |
| Chip Select Hold from Clock High | t _{CSH} | 0.5 | - | 0.5 | - | 0.5 | - | ns |
| ZZ High to Power Down | t _{PDS} | 2 | - | 2 | - | 2 | - | cycle |
| ZZ Low to Power Up | t _{PUS} | 2 | - | 2 | - | 2 | - | cycle |

- NOTE :**
1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and \overline{CS} is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
 3. A write cycle is defined by \overline{WE} low having been registered into the device at ADV Low, A Read cycle is defined by \overline{WE} High with ADV Low, Both cases must meet setup and hold times.
 4. To avoid bus contention, At a given voltage and temperature t_{clz} is more than t_{hzc}.
The soecs as shown do not imply bus contention because t_{clz} is a Min. parameter that is worst case at totally different test conditions (0°C,3.465V) than t_{hzc}, which is a Max. parameter(worst case at 70°C,3.135V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
 5. ADV must not be asserted for at least 2Clocks after leaving ZZ state.



SLEEP MODE

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z

The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

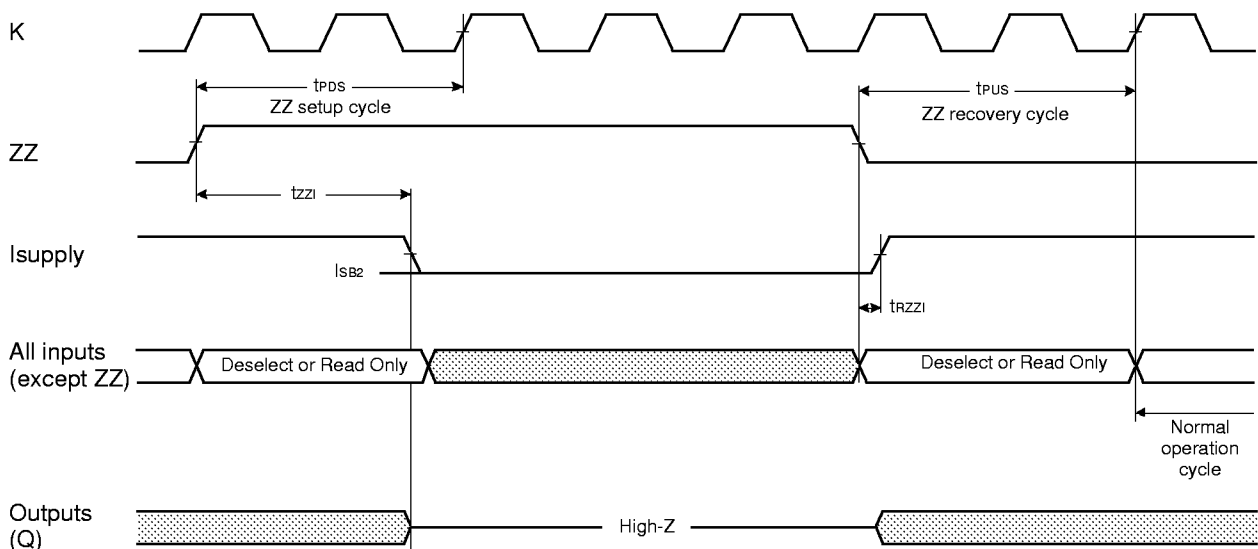
When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SLEEP MODE during t_{PUS} , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

SLEEP MODE ELECTRICAL CHARACTERISTICS

($V_{DD}, V_{DDQ}=2.5V \pm 5\%$)

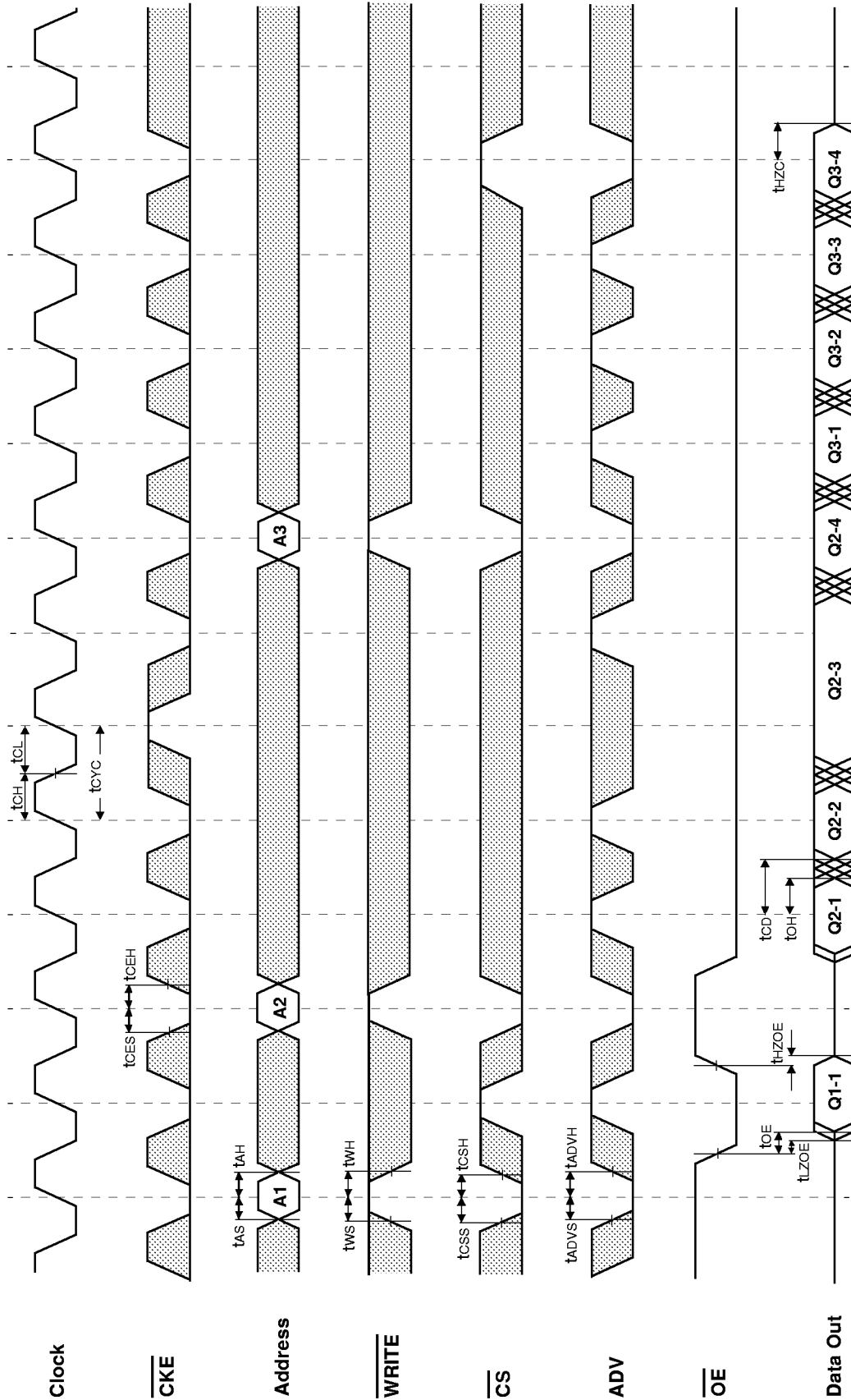
| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|-----------------------------------|------------------|------------|-----|-----|-------|
| Current during SLEEP MODE | $ZZ \geq V_{IH}$ | I_{SB2} | | 10 | mA |
| ZZ active to input ignored | | t_{PDS} | 2 | | cycle |
| ZZ inactive to input sampled | | t_{PUS} | 2 | | cycle |
| ZZ active to SLEEP current | | t_{ZZI} | | 2 | cycle |
| ZZ inactive to exit SLEEP current | | t_{RZZI} | 0 | | |

SLEEP MODE WAVEFORM



☒ DON'T CARE

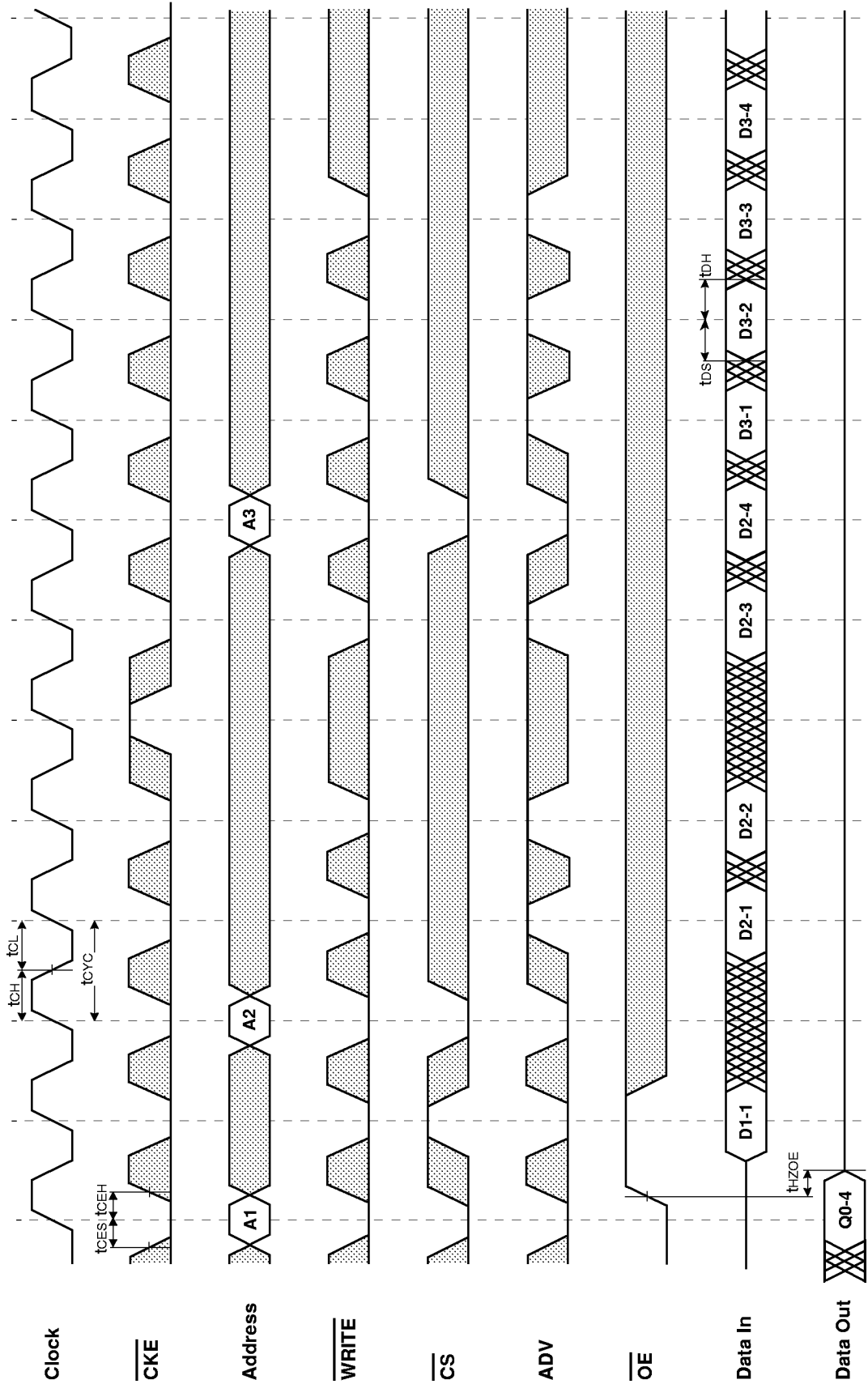
TIMING WAVEFORM OF READ CYCLE



☐ Don't Care
☒ Undefined

NOTES: $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS1}} = \text{L}$, $\overline{\text{CS2}} = \text{H}$ and $\overline{\text{CS2}} = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS1}} = \text{H}$, or $\overline{\text{CS1}} = \text{L}$ and $\overline{\text{CS2}} = \text{H}$, or $\overline{\text{CS1}} = \text{L}$, and $\overline{\text{CS2}} = \text{L}$

TIMING WAVEFORM OF WRTE CYCLE

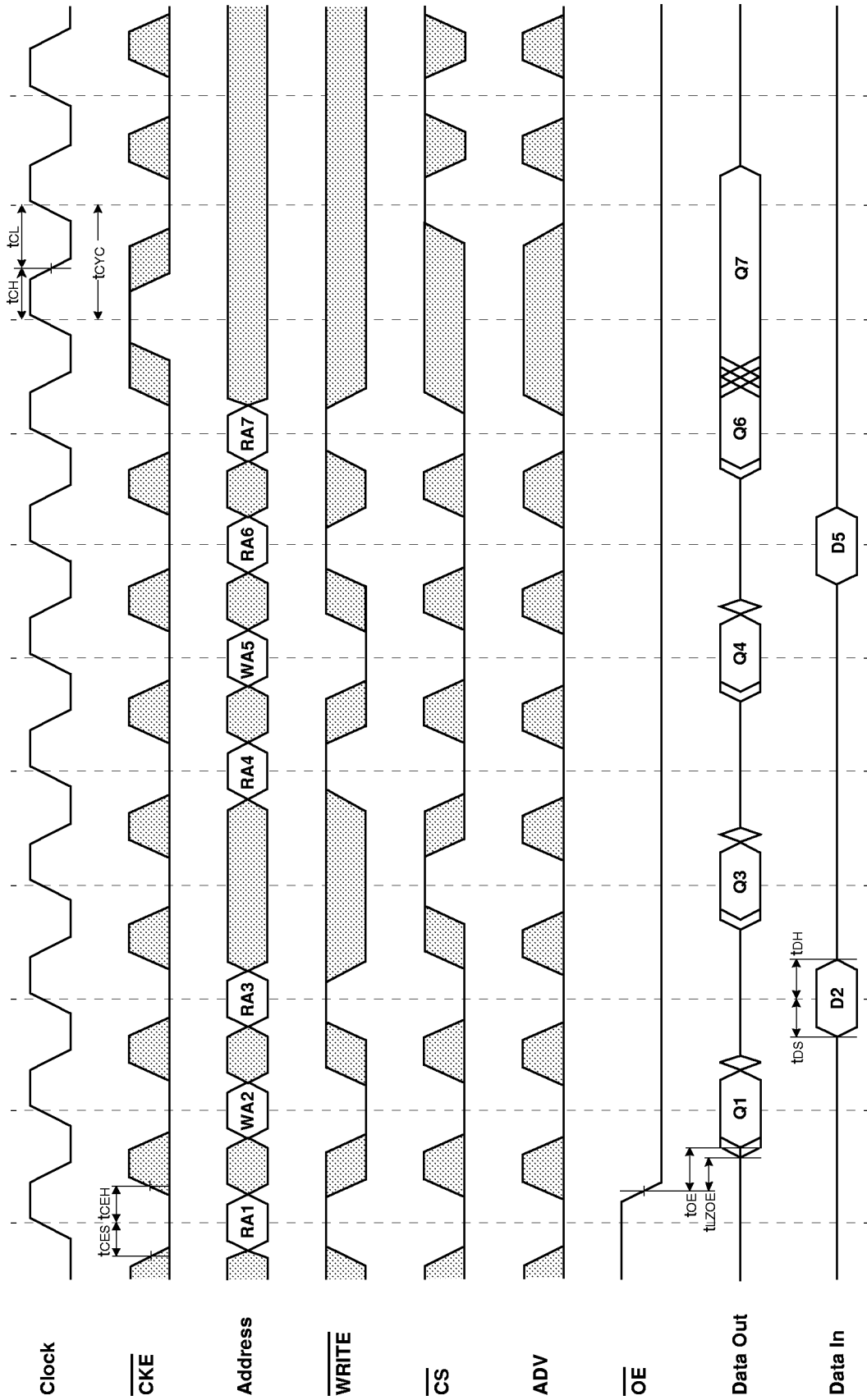


☐ Don't Care
⊠ Undefined

NOTES: $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS1} = L$, $\overline{CS2} = H$ and $\overline{CS2} = L$
 $\overline{CS} = H$ means $\overline{CS1} = H$, or $\overline{CS1} = L$ and $\overline{CS2} = H$, or $\overline{CS1} = L$, and $\overline{CS2} = L$



TIMING WAVEFORM OF SINGLE READ/WRITE

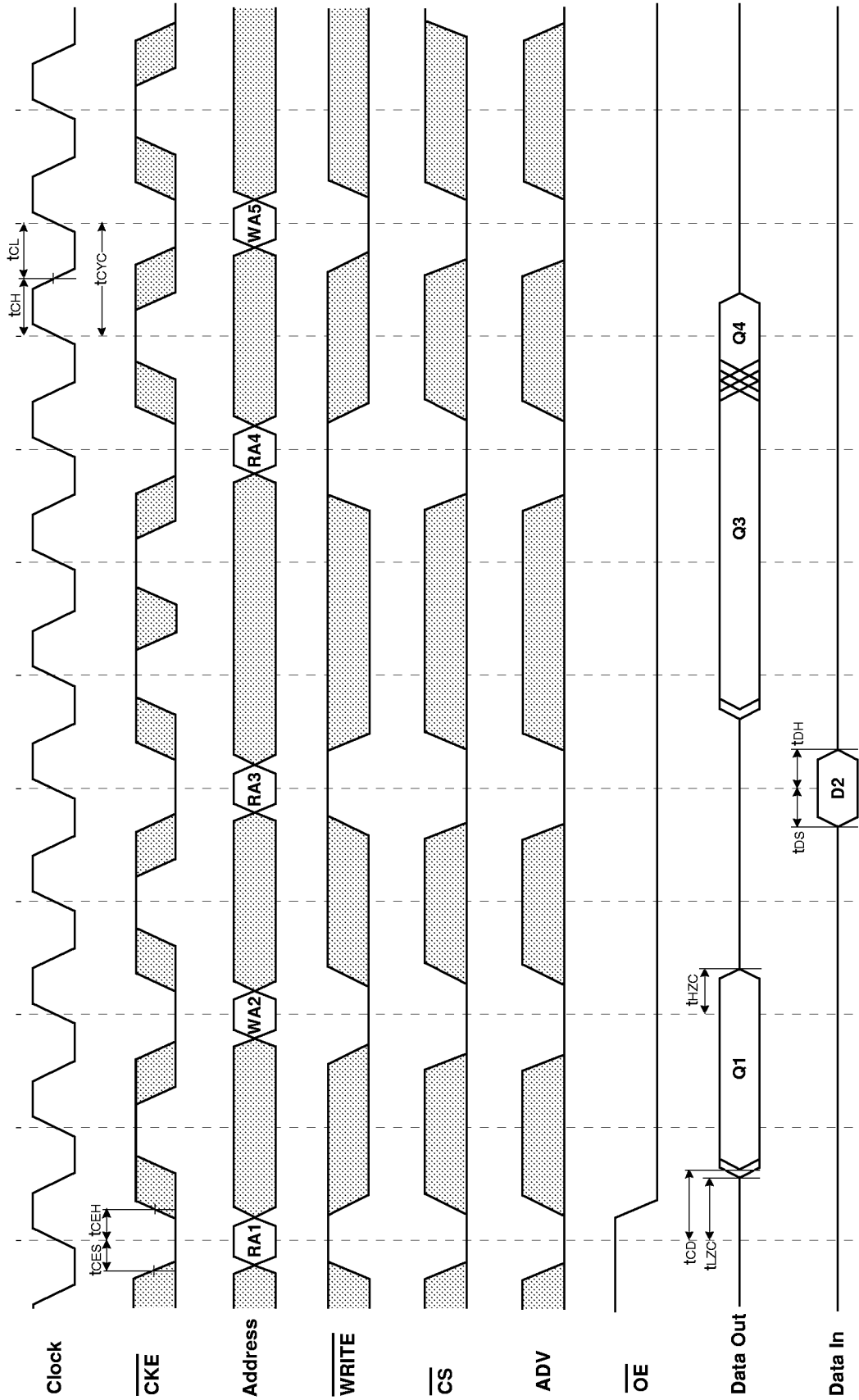


☐ Don't Care
☒ Undefined

NOTES: $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS1}} = \text{L}$, $\overline{\text{CS2}} = \text{H}$ and $\overline{\text{CS2}} = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS1}} = \text{H}$, or $\overline{\text{CS1}} = \text{L}$ and $\overline{\text{CS2}} = \text{H}$, or $\overline{\text{CS1}} = \text{L}$, and $\overline{\text{CS2}} = \text{L}$



TIMING WAVEFORM OF CKE OPERATION

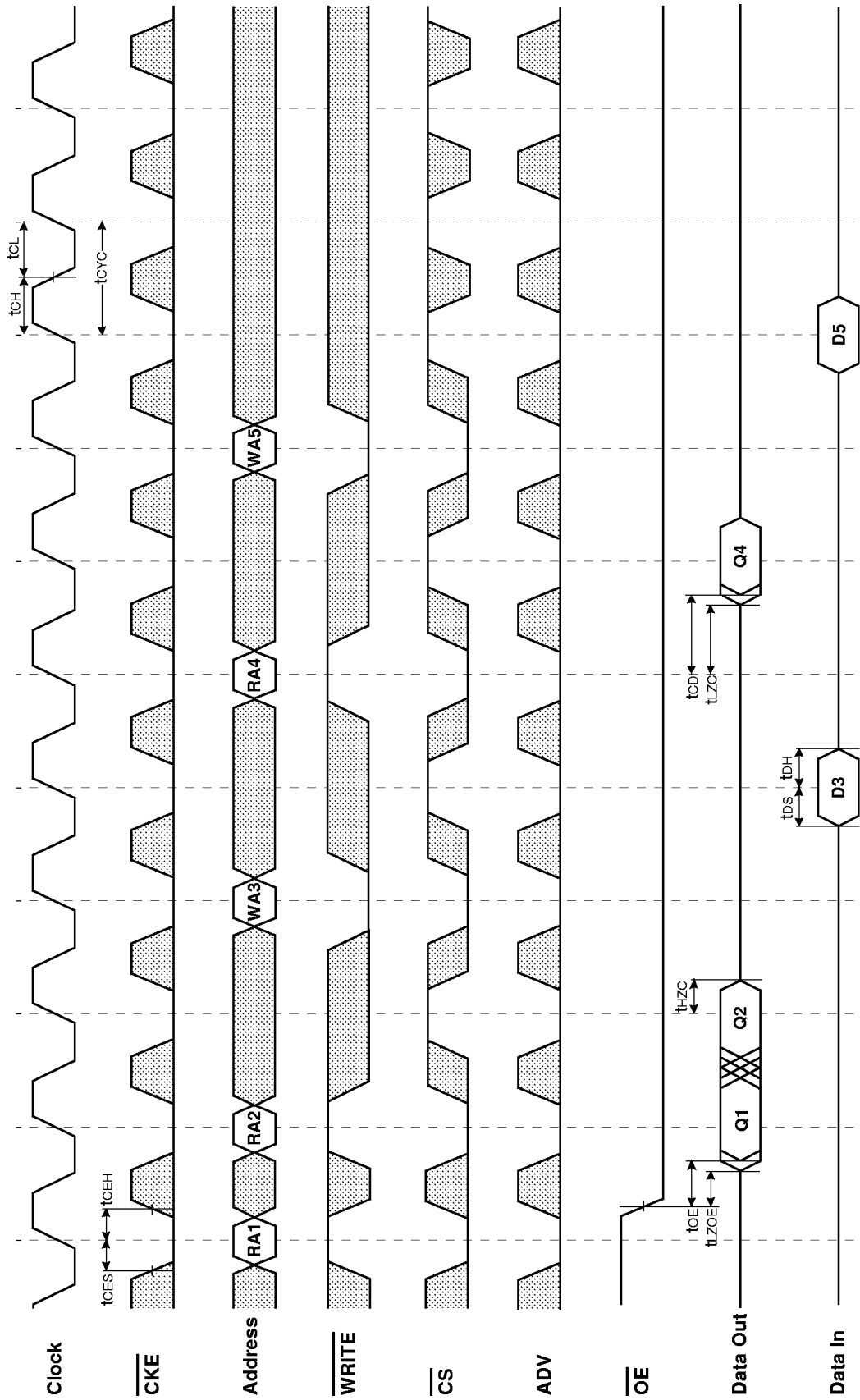


☐ Don't Care
☒ Undefined

NOTES : $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS1} = L$, $\overline{CS2} = H$ and $\overline{CS2} = L$
 $\overline{CS} = H$ means $\overline{CS1} = H$, or $\overline{CS1} = L$ and $\overline{CS2} = H$, or $\overline{CS1} = L$, and $\overline{CS2} = L$



TIMING WAVEFORM OF CS OPERATION



☐ Don't Care
☒ Undefined

NOTES: $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS1} = L$, $\overline{CS2} = H$ and $\overline{CS2} = L$
 $\overline{CS} = H$ means $\overline{CS1} = H$, or $\overline{CS1} = L$ and $\overline{CS2} = H$, or $\overline{CS1} = L$, and $\overline{CS2} = L$



PACKAGE DIMENSIONS

