MOTOROLA

Hex "D" Master-Slave Flip-Flop

ELECTRICALLY TESTED PER:
JM 38510/06103

The 10576 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

- 630 mW Max/Pkg (No Load)
- f_{toggle} = 150 MHz (typ)
- t_r, t_f = 2.0 ns typ (20% - 80%)

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PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω to V_{TT}
Q_1	3	7	4	51 Ω to V_{TT}
Q_2	4	8	5	51 Ω to V_{TT}
D0	5	9	7	GND
D_1	6	10	8	GND
D_2	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Clock	9	13	12	CP1
D_3	10	14	13	GND
D_4	11	15	14	GND
D_5	12	16	15	GND
Q_3	13	1	17	51 Ω to V_{TT}
Q_4	14	2	18	51 Ω to V_{TT}
Q_5	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

TRUTH TABLE

C	D	Q_{n+1}
L	∅	Q_n
* H	L	L
* H	H	H

∅ = Don't Care
* A clock H is a clock transition from a Low to a High state

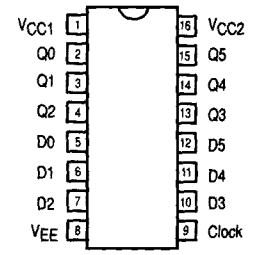
Military 10576

AVAILABLE AS

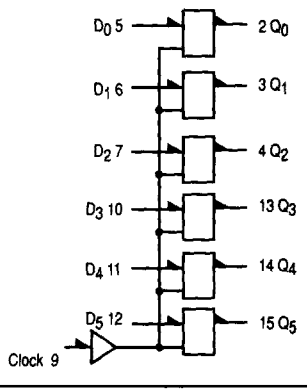
1) JAN: JM 38510/06103
2) SMD: N/A
3) 883: 10576/BXAJC
X = CASE OUTLINE AS FOLLOWS:

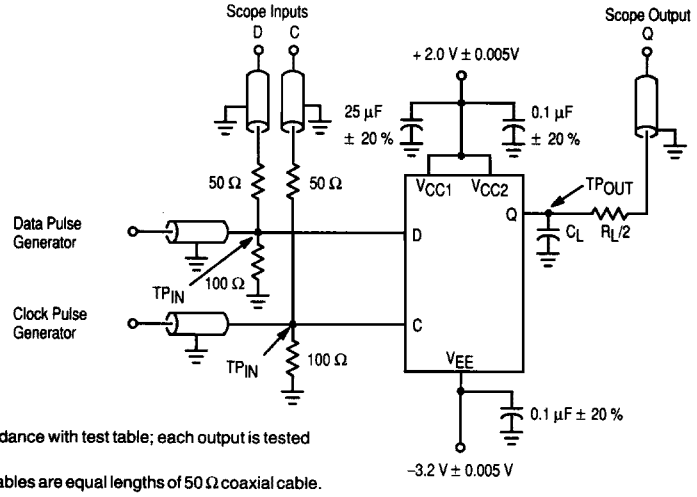
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM

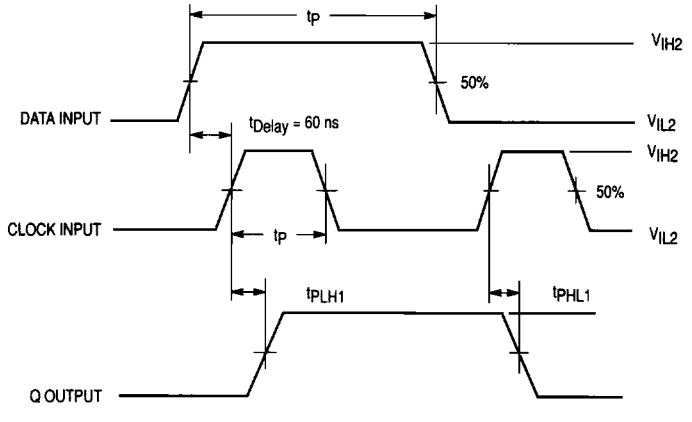




NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.25 inch (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Output not under test connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Scope input = 50 Ω to ground.
7. C_L (test jig) ≤ 5.0 pF.
8. Z_{OUT} = 50 Ω.

Figure 1. Synchronous Switching Test Circuit



NOTES

1. Note that observed pulse amplitude is attenuated by one half.
2. $t_{P(data)}$ = 150 ns.
3. $t_{P(clock)}$ = 40 ns.
4. PRR = 1.0 MHz.
5. $t_{THL} = t_{TLH}$ = 2.0 ns (20% to 80%).

Figure 2. Synchronous Switching Test Circuit Waveforms

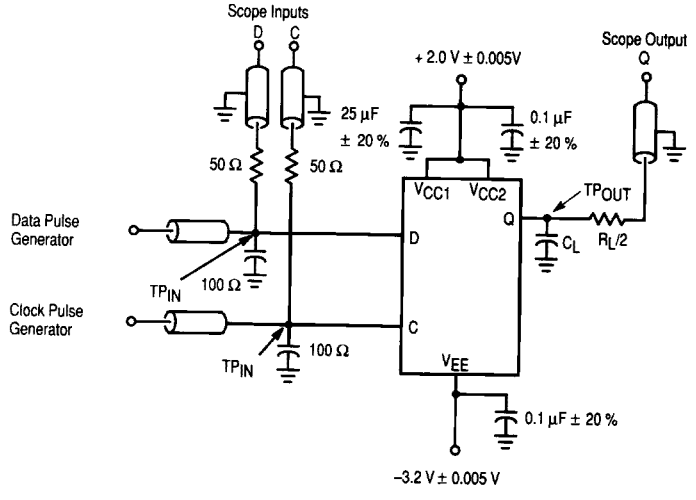


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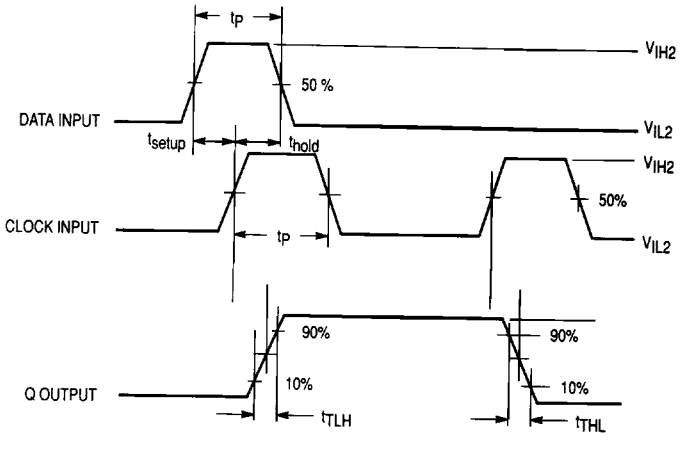
Figure 3. Setup and Hold Test Circuit



NOTES

1. Note that observed pulse amplitude is attenuated by one half.
2. $t_{P(data)}$ = 40 ns.
3. $t_{P(clock)}$ = 40 ns.
4. PRR = 1.0 MHz.
5. $t_{THL} = t_{TLH}$ = 2.0 ns (20% to 80%).

Figure 4. t_{SETUP} and t_{HOLD} Waveforms

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QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{ITH}	V_{ITL}	V_{IH1}	V_{IL1}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	Clk	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5 - 7, 10 - 12				9	8	16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V		5 - 7, 10 - 12				8	16	2 - 4, 13 - 15
V_{OTL}	Low Output Voltage		- 1.60		- 1.525		- 1.635	V	6, 7, 10 - 12	6, 7, 10 - 12	6, 7, 10 - 12	5 - 7, 10 - 12	9	8	16	2 - 4, 13 - 15
V_{OTH}	High Output Voltage	- 0.95		- 0.845		- 1.10		V	5 - 7, 10 - 12	5 - 7, 10 - 12		5 - 7, 10 - 12	9	8	16	2 - 4, 13 - 15
I_{IH1}	Input Current High		220		375		375	µA	5 - 7, 10 - 12					8	16	5 - 7, 10 - 12
I_{IH2}	Input Current High		310		527		527	µA	9					8	16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 10 - 12				8	16	5 - 7, 10 - 12
I_{EE}	Power Supply Drain Current	- 110		- 121		- 121		mA						8	16	8

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Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{ITH}	V_{ITL}	V_{IH1}	V_{IL1}	V_{EE}	V_{EEL}
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T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	4.0	1.0	4.5	1.0	4.3	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12
t_{THL}	Fall Time	1.1	4.0	1.0	4.5	1.0	4.3	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12
t_{PLH}	Propagation Delay	1.5	4.5	1.3	5.3	1.2	4.9	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12
t_{PLH}	Propagation Delay	1.5	4.5	1.3	5.3	1.2	4.9	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12
f_{Toggle}	Toggle Frequency	125		125		115		MHz	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12