DATA SHEET

M 65656

32 K × 8
ULTIMATE CMOS SRAM

FEATURES

- **ACCESS TIME**
  COMMERCIAL : 35(*), 40, 45, 55 NS
  INDUSTRIAL AND MILITARY :
  40(*), 45, 55 NS
- **VERY LOW POWER CONSUMPTION**
  ACTIVE : 50 mW (TYP)
  STANDBY : 0.5 µW (TYP)
  DATA RETENTION : 0.4 µW (TYP)

(*) Preliminary. Consult sales.

- **WIDE TEMPERATURE RANGE : – 55 TO + 125 °C**
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

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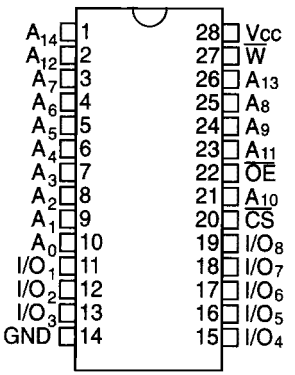
INTRODUCTION

The M 65656 is a very low power CMOS static RAM organized as 32768 × 8 bits. It is manufactured using the MHS high performance CMOS technology named SCMOS.
With this process, MHS is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments or embarked systems.
Using an array of six transistors (6T) memory cells, the M 65656 combines an extremely low standby supply current (Typical value = 0.1 µA) with a fast access time at 40 ns. The high stability of the 6T cell provides excellent protection against soft errors due to noise.
Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.
For military/space applications that demand superior levels of performance and reliability the M 65656 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

INTERFACE

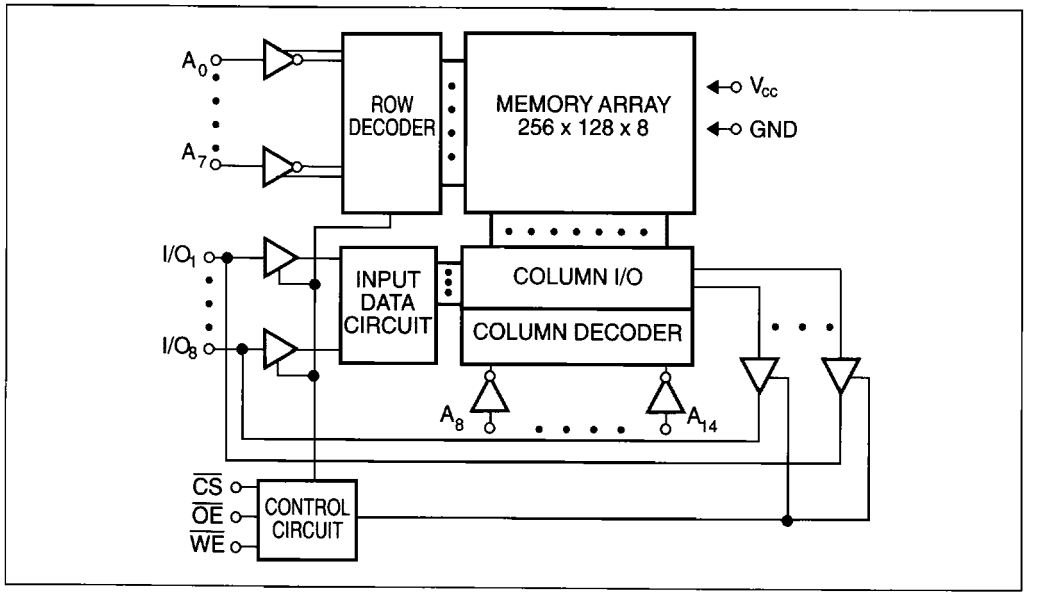
PIN CONFIGURATION

Side Brazed 600/300 mils 28 pins
SOIC/SOJ 300 mils 28 pins
CDIL 600 mils 28 pins
Multilayer Flat Pack 28 pins



(Top View)

BLOCK DIAGRAM



PIN NAMES

A_0-A_{14}	: Address inputs	$\overline{CS}$	: Chip-Select
I/O0-I/O7	: Input/Output	$\overline{W}$	: Write Enable
Vcc	: Power	$\overline{OE}$	: Output Enable
GND	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	$\overline{OE}$	INPUTS/ OUTPUTS	MODE
H	X	X	Z	Deselect/ POWER-DOWN
L	H	L	DATA OUT	Read
L	L	X	DATA IN	Write
L	H	H	Z	Output Disable

L = low, H = high, X = H or L, Z = high impedance.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.3 V to + 7.0 V
Input or Output voltage applied : (Gnd - 0.3 V) to (Vcc + 0.3 V)
Storage temperature : - 65 °C to + 150 °C
(Electro static discharge voltage > 1250 V (MIL STD 883, METHOD 3015)

OPERATING RANGE

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	V_{CC} = 5 V ± 10 %	– 55 °C to + 125 °C
Industrial	V_{CC} = 5 V ± 10 %	– 40 °C to 85 °C
Commercial	V_{CC} = 5 V ± 10 %	0 °C to 70 °C

DC OPERATING CONDITIONS

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc		Supply voltage	4.5	5.0	5.5	V
Gnd		Ground	0.0	0.0	0.0	V
VIL	(1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	(1)	input high voltage	2.2	–	Vcc + 0.3	V

Note : 1. VIH max = Vcc + 0.3 V, VIL min = – 0.3 V or – 1.0 pulse 50 ns.

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(2)	Input capacitance	–	–	8	pF
Cout	(2)	Output capacitance	–	–	8	pF

Notes : 2. TA = 25 °C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0	–	1.0	µA
IOZ	(3)	Output leakage current	– 1.0	–	1.0	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 4 mA, IOH = – 1.0 mA.

CONSUMPTION FOR COMMERCIAL SPECIFICATION

SYMBOL	PARAMETER	M 65656 L-35(*)	M 65656 V-35(*)	M 65656 L-40	M 65656 V-40	M 65656 L-45	M 65656 V-45	M 65656 L-55	M 65656 V-55	UNIT	VALUE
ICCSB (5)	Standby supply current	10	5	10	5	10	5	10	5	mA	max
ICCSB1 (6)	Standby supply current	75	5	75	5	75	5	75	5	µA	max
ICCOP (7)	Operating supply current	90	70	90	70	90	70	90	70	mA	max

CONSUMPTION FOR INDUSTRIAL SPECIFICATION

SYMBOL	PARAMETER	M 65656 L-40(*)	M 65656 V-40(*)	M 65656 L-45	M 65656 V-45	M 65656 L-55	M 65656 V-55	UNIT	VALUE
ICCSB (5)	Standby supply current	10	5	10	5	10	5	mA	max
ICCSB1 (6)	Standby supply current	100	10	100	10	100	10	µA	max
ICCOP (7)	Operating supply current	90	70	90	70	90	70	mA	max

CONSUMPTION FOR MILITARY SPECIFICATION

SYMBOL	PARAMETER	M 65656 L-40(*)	M 65656 V-40(*)	M 65656 L-45	M 65656 V-45	M 65656 L-55	M 65656 V-55	UNIT	VALUE
ICCSB (5)	Standby supply current	10	5	10	5	10	5	mA	max
ICCSB1 (6)	Standby supply current	500	100	500	100	500	100	µA	max
ICCOP (7)	Operating supply current	90	70	90	70	90	70	mA	max

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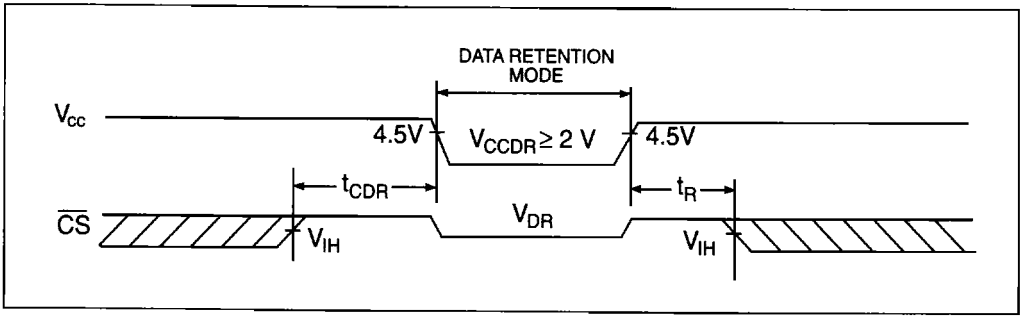
Notes : 5. $\overline{CS} \geq VIH$, $Vin \geq VIH$ or $Vin \leq VIL$.
6. $\overline{CS} \geq Vcc - 0.3$ V, Iout = 0 mA. $Vin \geq Vcc - 0.3$ V or $Vin \leq 0.3$ V.
7. Vcc max, Iout = 0 mA, Vin = Gnd/Vcc. Duty cycle 100 %, F = 5 MHz, derating = 10 mA/MHz.
(*) Preliminary. Please consult sales.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc – 0.2 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ must be kept between Vcc – 0.3 V and 70 % of Vcc during the power up and power down transitions.
4. The RAM can begIn operation > 45 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (8)	MAXIMUM			UNIT
VCCDR	Vcc for data retention	2.0	–	–			V
TCDR	Chip deselect to data retention time	0.0	–	–			ns
TR	Operation recovery time	TAVAV (9)	–	–			ns
ICCDR1 (10)	Data retention current			COM	IND	MIL	
	@ 2.0 V : M-65656 V	–	0.1	3	8	80	µA
	M-65656 L	–	0.1	60	80	300	µA
ICCDR2 (10)	Data retention current						
	@ 3.0 V : M-65656 V	–	0.3	4	9	90	µA
	M-65656 L	–	0.3	70	90	400	µA

Notes : 8. TA = 25°C.
9. TAVAV = Read cycle time.
10. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested at Vcc = 2 V.

AC PARAMETERS

AC CONDITIONS

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output load : See fig. 1a, 1b

WRITE CYCLE : COMMERCIAL SPECIFICATION (note 12)

SYMBOL	PARAMETER	M 65656 L/V–35(*)	M 65656 L/V–40	M 65656 L/V–45	M 65656 L/V–55	UNIT	VALUE
TAVAV	Write cycle time	35	40	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	30	30	35	40	ns	min
TDVWH	Data set-up time	20	22	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	30	30	35	40	ns	min
TWLQZ (11)	Write low to high Z	15	15	15	20	ns	max
TWLWH	Write pulse width	30	30	35	40	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (11)	Write high to low Z	0	0	0	0	ns	min

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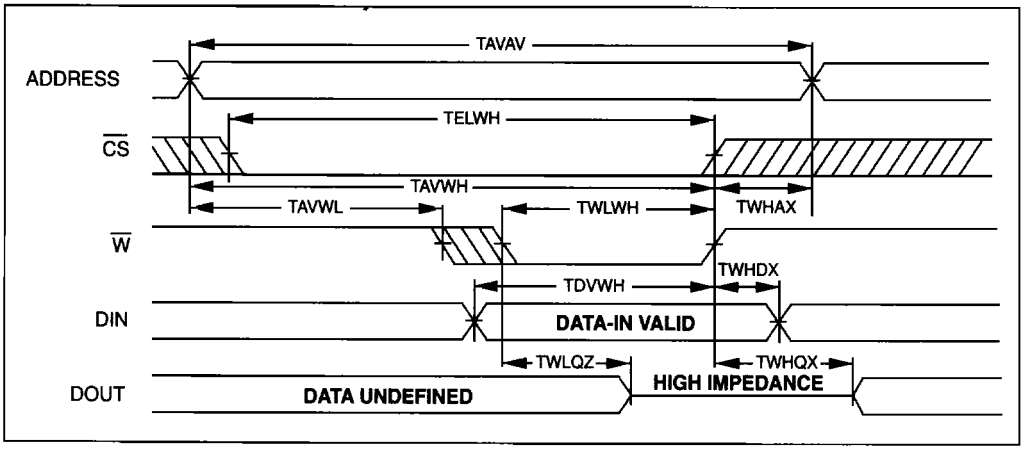
WRITE CYCLE : INDUSTRIAL AND MILITARY SPECIFICATION (note 12)

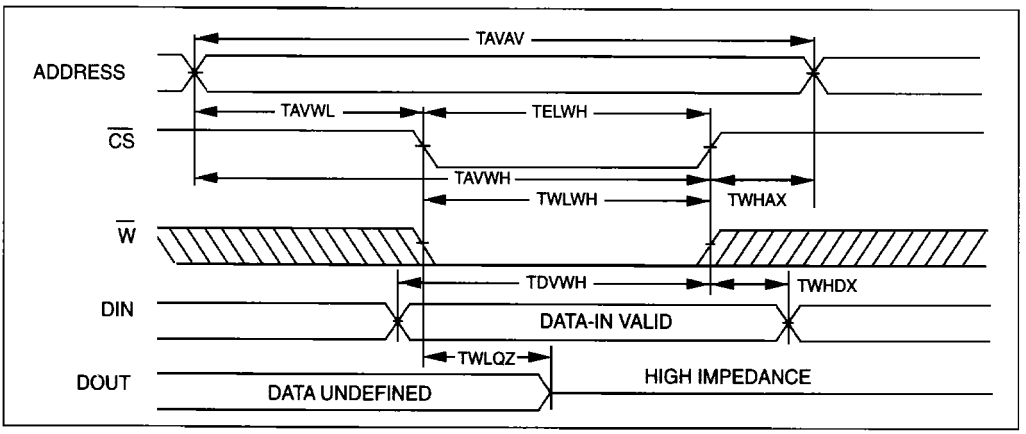
SYMBOL	PARAMETER	M 65656 L/V–40(*)	M 65656 L/V–45	M 65656 L/V–55	UNIT	VALUE
TAVAV	Read cycle time	40	45	55	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	30	35	40	ns	min
TDVWH	Data set-up time	22	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	30	35	40	ns	min
TWLQZ (11)	Write low to high Z	15	15	20	ns	min
TWLWH	Write pulse width	30	35	40	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (11)	Write high to low Z	0	0	0	ns	min

Notes : 11. Specified with CL = 5 pF (see figure 1b). Guaranteed. Not tested.
(*) Preliminary. Consult sales.

WRITE CYCLE 1 : $\overline{W}$ CONTROLLED (note 12)



WRITE CYCLE 2 : $\overline{CS}$ CONTROLLED (note 12)



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Note : 12. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$ = VIH.

AC TEST LOADS AND WAVEFORMS

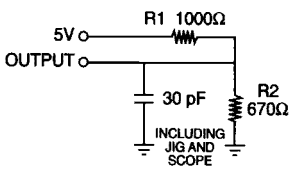


Figure 1 a

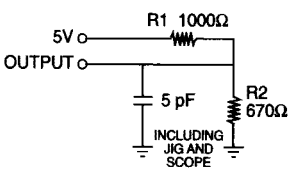


Figure 1 b

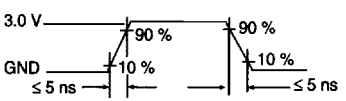
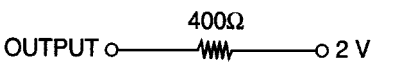


Figure 2

Equivalent to : THEVENIN EQUIVALENT



READ CYCLE : COMMERCIAL SPECIFICATION

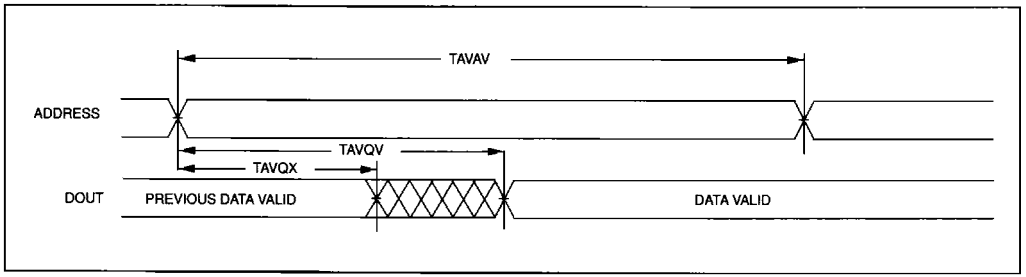
SYMBOL	PARAMETER	M 65656 L/V-35(*)	M 65656 L/V-40	M 65656 L/V-45	M 65656 L/V-55	UNIT	VALUE
TAVAV	Write cycle time	35	40	45	55	ns	min
TAVQV	Address access time	35	40	45	55	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	35	40	45	55	ns	max
TELQX (13)	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ (13)	$\overline{CS}$ high to high Z	20	20	20	20	ns	max
TGLQV	Output Enable access time	18	20	20	25	ns	max
TGLQX (13)	$\overline{OE}$ low to low Z	5	5	5	5	ns	min
TGHQZ (13)	$\overline{OE}$ high to high Z	15	15	15	20	ns	max

READ CYCLE : INDUSTRIAL AND MILITARY SPECIFICATION

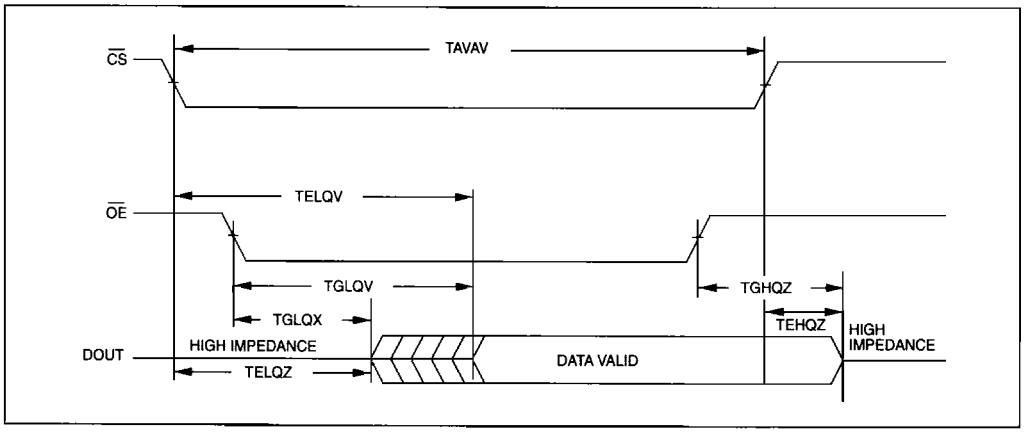
SYMBOL	PARAMETER	M 65656 L/V-40(*)	M 65656 L/V-45	M 65656 L/V-55	UNIT	VALUE
TAVAV	Read cycle time	40	45	55	ns	min
TAVQV	Address access time	40	45	55	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	40	45	55	ns	max
TELQX (13)	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ (13)	$\overline{CS}$ high to high Z	20	20	20	ns	max
TGLQV	Output Enable access time	20	20	25	ns	max
TGLQX (13)	$\overline{OE}$ low to low Z	5	5	5	ns	min
TGHQZ (13)	$\overline{OE}$ high to high Z	15	15	20	ns	max

Notes : 13. Specified with C_L = 5 pF (see figure 1b). Guaranteed but not tested.
(*) Preliminary. Consult sales.

READ CYCLE nb 1 (notes 14, 15)



READ CYCLE nb 2 (notes 14, 16)



Notes : 14. $\overline{W}$ is high for read cycle.
15. Device is continuously selected $\overline{CS}$ & $\overline{OE}$= VIL.
16. Address valid prior to or coincident with $\overline{CS}$ transition low.

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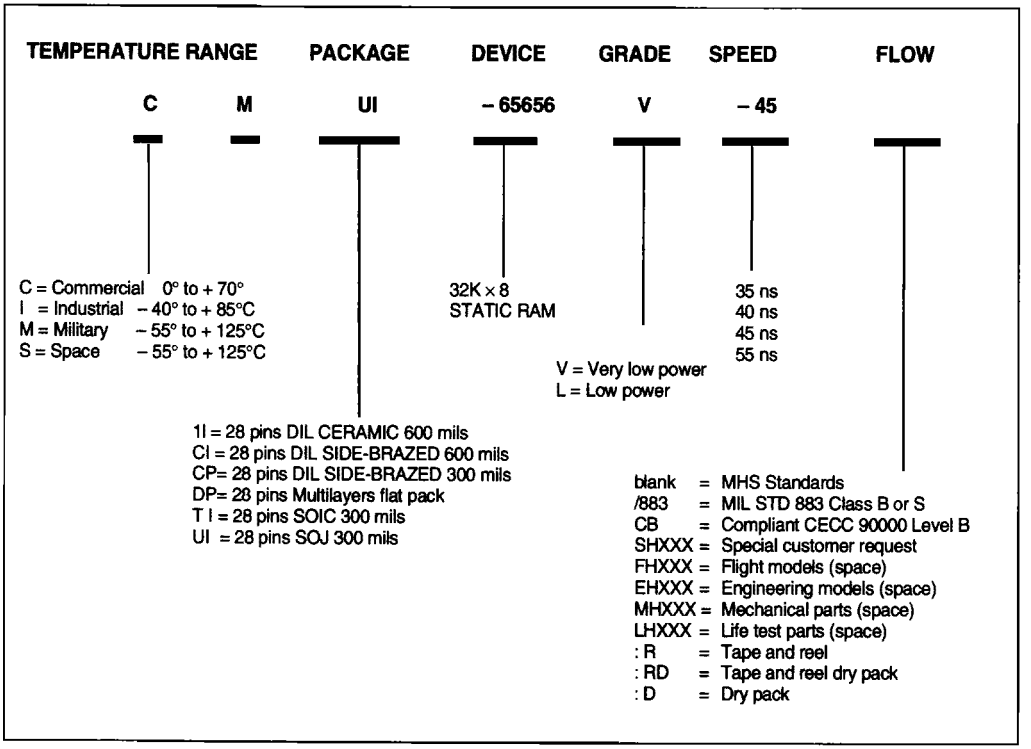
ORDERING INFORMATION



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