NPN SILICON RF POWER TRANSISTOR

DESCRIPTION:

The **ASI AVD400** is a silicon NPN power transistor, designed for high power and low duty cycle DME and IFF applications.

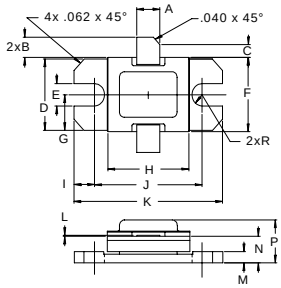
FEATURES:

- Internal Input/Output Matching Networks
- $\mathbf{P_G}$ = 6.5 dB at 400 W/1150 MHz
- ***Omnigold***™ Metalization System

MAXIMUM RATINGS

$\mathbf{I_C}$	22 A
$\mathbf{V_{CC}}$	55 V
$\mathbf{P_{DISS}}$	1458 W @ T_C = 25 °C
$\mathbf{T_J}$	-65 °C to +200 °C
$\mathbf{T_{STG}}$	-65 °C to +200 °C
$\mathbf{\theta_{JC}}$	0.12 °C/W

PACKAGE STYLE .400 2L FLG (A)



DIM	MINIMUM inches / mm	MAXIMUM inches / mm
A	.135 / 3.43	.145 / 3.68
B	.100 / 2.54	.120 / 3.05
C	.050 / 1.27	
D	.376 / 9.55	.396 / 10.06
E	.110 / 2.79	.130 / 3.30
F	.395 / 10.03	.407 / 10.34
G	.193 / 4.90	
H	.490 / 12.45	.510 / 12.95
I	.100 / 2.54	
J	.690 / 17.53	.710 / 18.03
K	.890 / 22.61	.910 / 23.11
L	.003 / 0.08	.006 / 0.18
M	.052 / 1.32	.072 / 1.83
N	.118 / 3.00	.131 / 3.33
P		.230 / 5.84

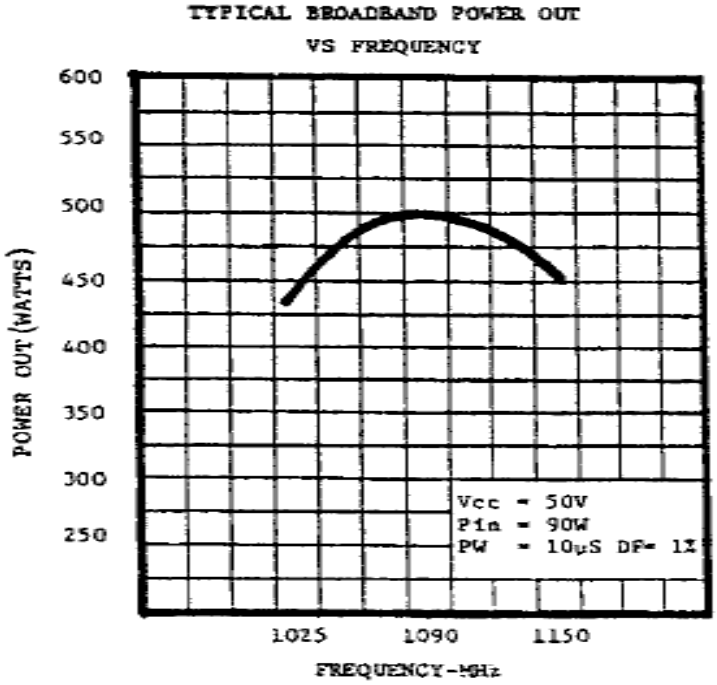
ORDER CODE: ASI10567

CHARACTERISTICS T_C = 25 °C

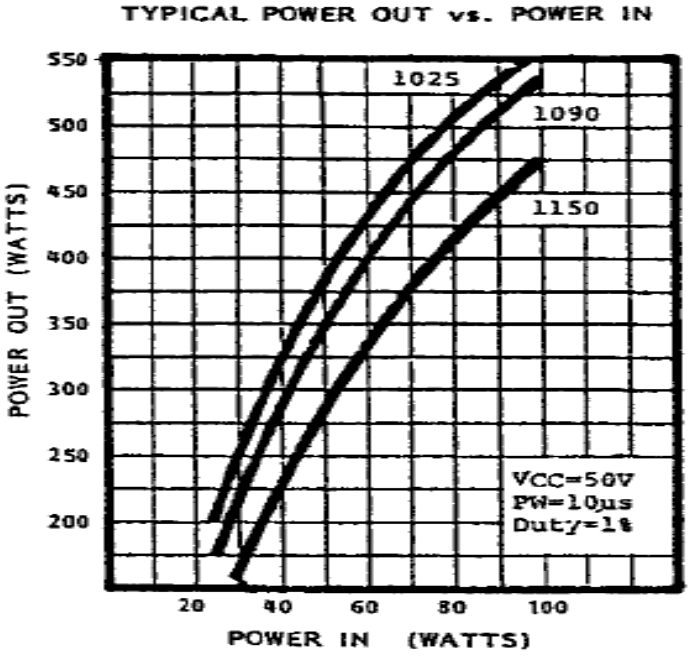
SYMBOL	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
$\mathbf{BV_{CBO}}$	I_C = 25 mA	65			**V**
$\mathbf{BV_{CES}}$	I_C = 50 mA	65			**V**
$\mathbf{BV_{EBO}}$	I_E = 10 mA	3.5			**V**
$\mathbf{I_{CES}}$	V_{CE} = 50 V			25	**mA**
$\mathbf{h_{FE}}$	V_{CE} = 5.0 V I_C = 0.25 A	10		200	**---**
$\mathbf{P_G}$ $\mathbf{\eta_C}$	V_{CC} = 50 V P_{OUT} = 400 W f = 1025 - 1150 MHz P_{IN} = 90 W	6.5 40			**dB** **%**

Pulse Width = 10 µsec, Duty Cycle = 1 %

POWER OUTPUT vs FREQUENCY



POWER OUTPUT vs POWER INPUT



IMPEDANCE DATA:

FREQ	$Z_{IN}(\Omega)$	$Z_{CL}(\Omega)$
1020 MHz	2.89 + j4.1	1.38 – j3.2
1090 MHz	2.32 + j3.4	1.33 – j2.8
1150 MHz	1.99 + j2.8	1.26 – j2.5

P_{IN} = 90 W
V_{CE} = 50 V