

# 512Kx8 Plastic Monolithic SRAM CMOS

## FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times of 17, 20, 25ns
  - Data Retention Function (LPA version)
  - Extended Temperature Testing
  - Data Retention Functionality Testing
- 36 lead JEDEC Approved Revolutionary Pinout
  - Plastic SOJ (Package 319)
- Single +5V ( $\pm 10\%$ ) Supply Operation

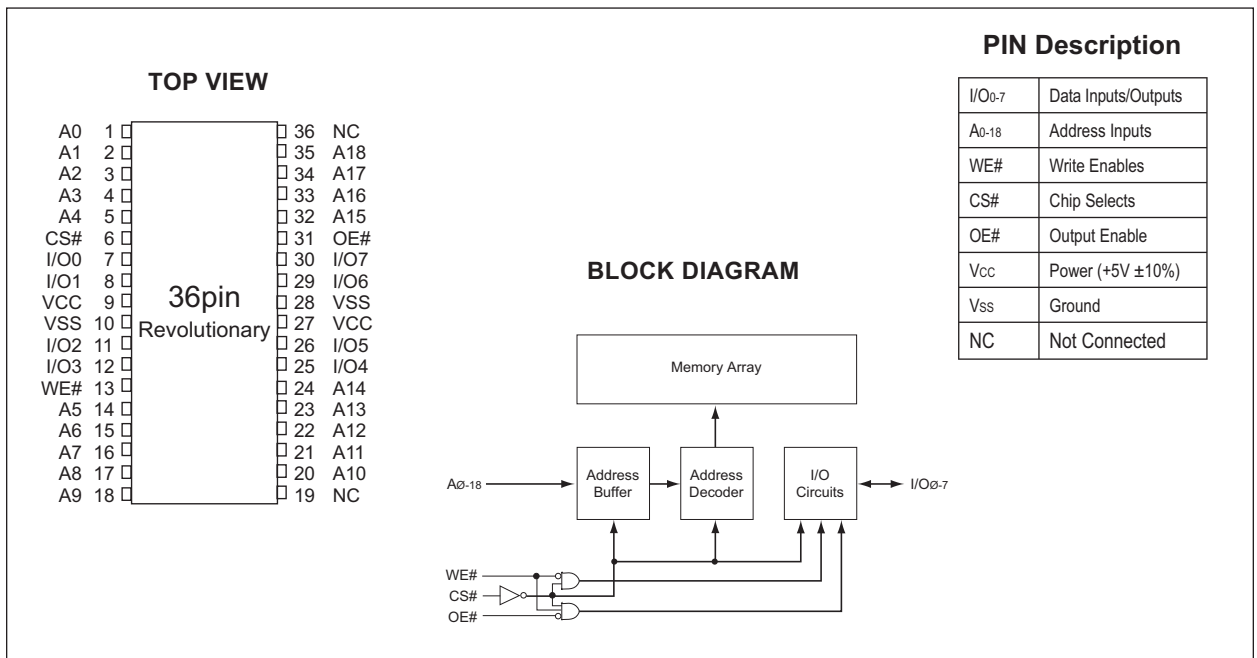
WEDC's ruggedized plastic 512Kx8 SRAM that allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

Extended temperature testing is performed with the test patterns developed for use on WEDC's fully compliant 512Kx8 SRAMs. WEDC fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial guarantee a device that operates reliably in the field at temperature extremes. Users of WEDC's ruggedized plastic benefit from WEDC's extensive experience in characterizing SRAMs for use in military systems.

WEDC ensures Low Power devices will retain data in Data Retention mode by characterizing the devices to determine the appropriate test conditions. This is crucial for systems operating at  $-40^{\circ}\text{C}$  or below and using dense memories such as 512Kx8s.

WEDC's ruggedized plastic SOJ is footprint compatible with WEDC's full military ceramic 36 pin SOJ.

**FIG. 1 – PIN CONFIGURATION**





**ABSOLUTE MAXIMUM RATINGS**

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature TA (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, TJ	175	°C

**NOTE:**

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAPACITANCE**

TA = +25°C

Parameter	Symbol	Condition	Max	Unit
Address Lines	CI	VIN = Vcc or Vss, f = 1.0MHz	6	pF
Data Lines	CO	VIN = Vcc or Vss, f = 1.0MHz	8	pF

These parameters are sampled, not 100% tested.

**DC CHARACTERISTICS**

Vcc = 5V, Vss = 0V, -55°C ≤ TA ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	ILI	Vcc = 5.5, VIN = Vss to Vcc		10	µA
Output Leakage Current	ILO	CS# = VIL, OE# = VIH, VOUT = Vss to Vcc		10	µA
Operating Supply Current	Icc	CS# = VIL, OE# = VIH, f = 5MHz, Vcc = 5.5		180	mA
Standby Current	Isb	CS# = VIH, OE# = VIH, f = 5MHz, Vcc = 5.5		15	mA
Output High Voltage	VOH	IOH = -4.0mA, Vcc = 4.5	2.4		V
Output Low Voltage	VOL	IOL = 8.0mA, Vcc = 4.5		0.4	V

NOTE: DC test conditions: VIL = 0.3V, VIH = Vcc - 0.3V

**AC TEST CONDITIONS**

**Figure 1**

**Figure 2**

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

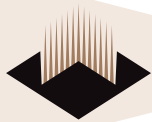
NOTE: For tEHOZ, tGHOZ and tWLOZ, CL = 5pF (Figure 2)

**TRUTH TABLE**

OE#	CS#	WE#	Mode	Output	Power
X	H	X	Standby	High Z	Icc2, Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	Data Out	Icc1
X	L	L	Write	Data In	Icc1

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	VIH	2.2	—	Vcc + 0.5	V
Input Low Voltage	VIL	-0.3	—	+0.8	V



## AC CHARACTERISTICS – READ CYCLE

$V_{CC} = 5.0V, V_{SS} = 0V, 0^{\circ}C \leq T_A \leq +70^{\circ}C$

Parameter	Symbol		17ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	17		20		25		ns
Address Access Time	t <sub>AVQV</sub>	t <sub>AA</sub>		17		20		25	ns
Chip Enable Access Time	t <sub>ELQV</sub>	t <sub>ACS</sub>		17		20		25	ns
Chip Enable to Output in Low Z (1)	t <sub>ELQX</sub>	t <sub>CLZ</sub>	3		3		3		ns
Chip Disable to Output in High Z (1)	t <sub>EHQZ</sub>	t <sub>CHZ</sub>	0	7	0	8	0	10	ns
Output Hold from Address Change	t <sub>AVQX</sub>	t <sub>OH</sub>	0		0		0		ns
Output Enable to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		8		10		12	ns
Output Enable to Output in Low Z (1)	t <sub>GLQX</sub>	t <sub>OLZ</sub>	0		0		0		ns
Output Disable to Output in High Z(1)	t <sub>GHQZ</sub>	t <sub>OHZ</sub>	0	7	0	8	0	10	ns

1. This parameter is guaranteed by design but not tested.

## AC CHARACTERISTICS – WRITE CYCLE

$V_{CC} = 5.0V, V_{SS} = 0V, 0^{\circ}C \leq T_A \leq +70^{\circ}C$

Parameter	Symbol		17ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	17		20		25		ns
Chip Enable to End of Write	t <sub>ELWH</sub>	t <sub>CW</sub>	14		15		17		ns
	t <sub>ELEH</sub>	t <sub>CW</sub>	14		15		17		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		0		0		ns
	t <sub>AVEL</sub>	t <sub>AS</sub>	0		0		0		ns
Address Valid to End of Write	t <sub>AVWH</sub>	t <sub>AW</sub>	14		15		17		ns
	t <sub>AVEH</sub>	t <sub>AW</sub>	14		15		17		ns
Write Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	14		15		17		ns
	t <sub>WLEH</sub>	t <sub>WP</sub>	14		15		17		ns
Write Recovery Time	t <sub>WHAX</sub>	t <sub>WR</sub>	0		0		0		ns
	t <sub>EHAX</sub>	t <sub>WR</sub>	0		0		0		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		0		0		ns
	t <sub>EHDX</sub>	t <sub>DH</sub>	0		0		0		ns
Write to Output in High Z (1)	t <sub>WLQZ</sub>	t <sub>WHZ</sub>	0	8	0	8	0	10	ns
Data to Write Time	t <sub>DVWH</sub>	t <sub>DW</sub>	8		10		12		ns
	t <sub>DVEH</sub>	t <sub>DW</sub>	8		10		12		ns
Output Active from End of Write (1)	t <sub>WHQX</sub>	t <sub>WLZ</sub>	0		0		0		ns

1. This parameter is guaranteed by design but not tested.



FIG. 2 – TIMING WAVEFORM — READ CYCLE

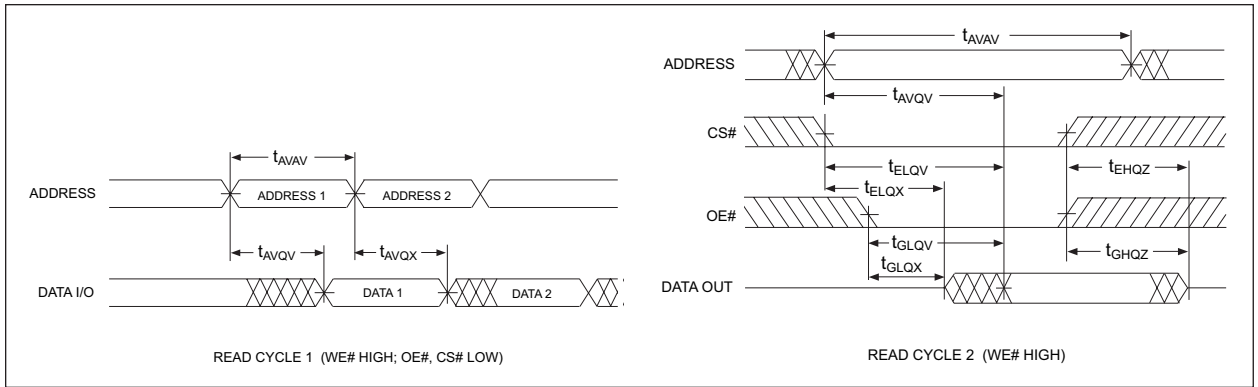


FIG. 3 – WRITE CYCLE — WE# CONTROLLED

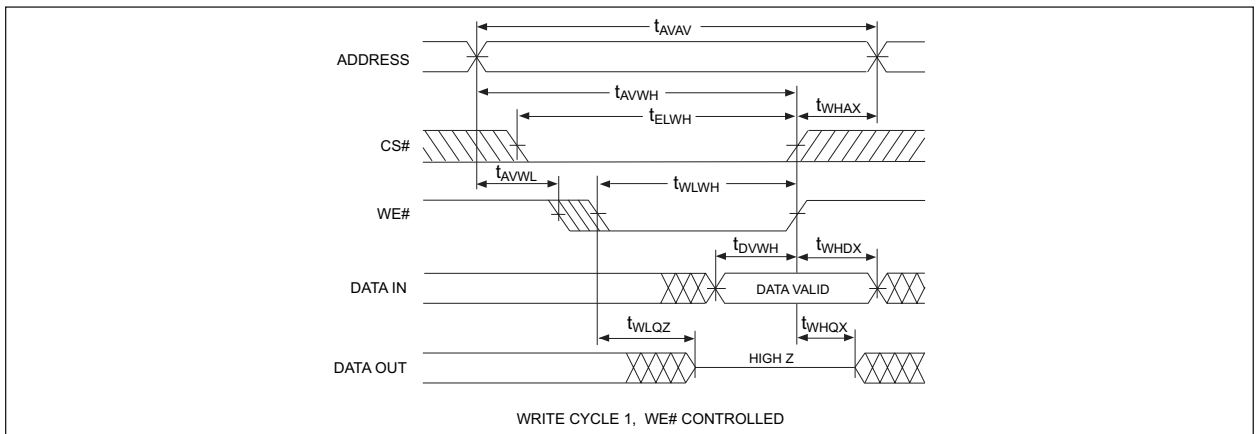
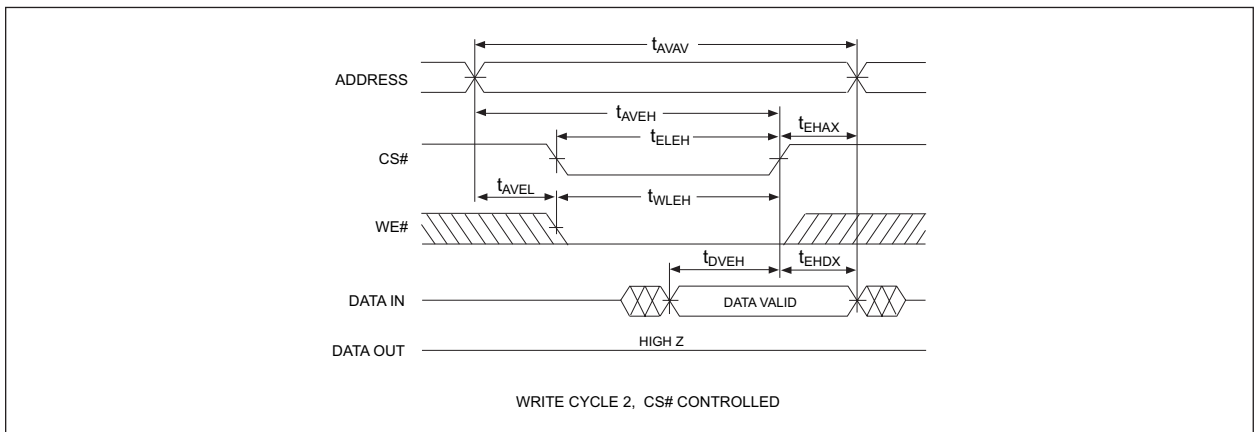


FIG. 4 – WRITE CYCLE — CS# CONTROLLED





**DATA RETENTION CHARACTERISTICS (EDI88512LPA ONLY)**

-55°C ≤ T<sub>A</sub> ≤ +125°C

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V <sub>DD</sub>	V <sub>DD</sub> = 2.0V	2	-	-	V
Data Retention Quiescent Current	I <sub>CCDR</sub>	CS# ≥ V <sub>DD</sub> - 0.2V	-	-	2	mA
Chip Disable to Data Retention Time	T <sub>CDR</sub>	V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V	0	-	-	ns
Operation Recovery Time	T <sub>R</sub>	or V <sub>IN</sub> ≤ 0.2V	T <sub>AVAV</sub>	-	-	ns

**FIG. 5 – DATA RETENTION - CS# CONTROLLED**

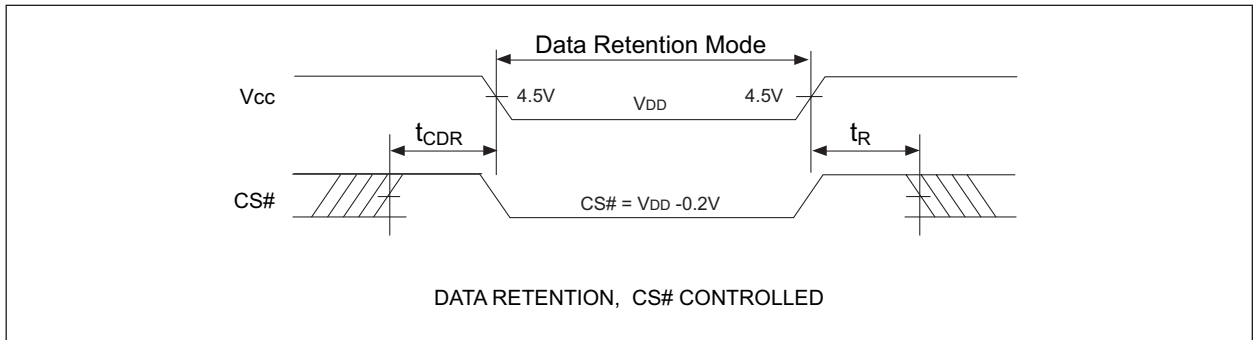
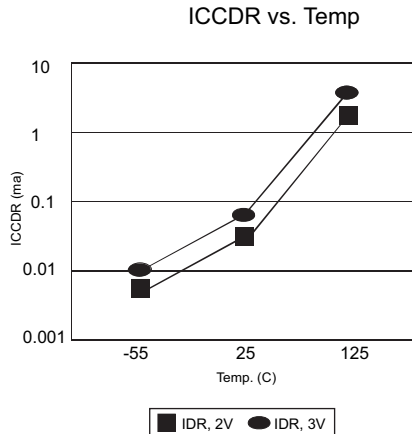
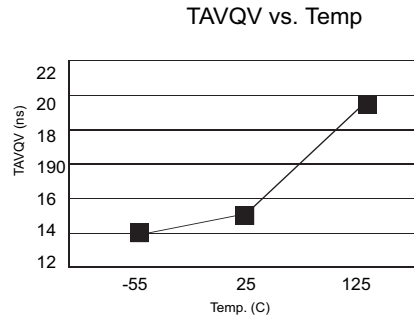
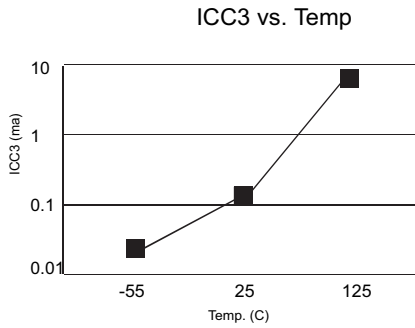
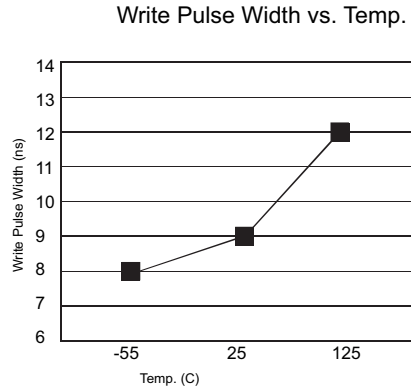
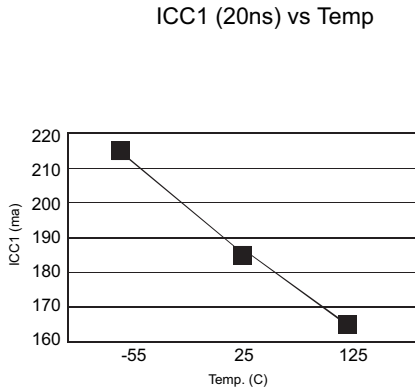




FIG. 6 – NORMALIZED OPERATING GRAPHS

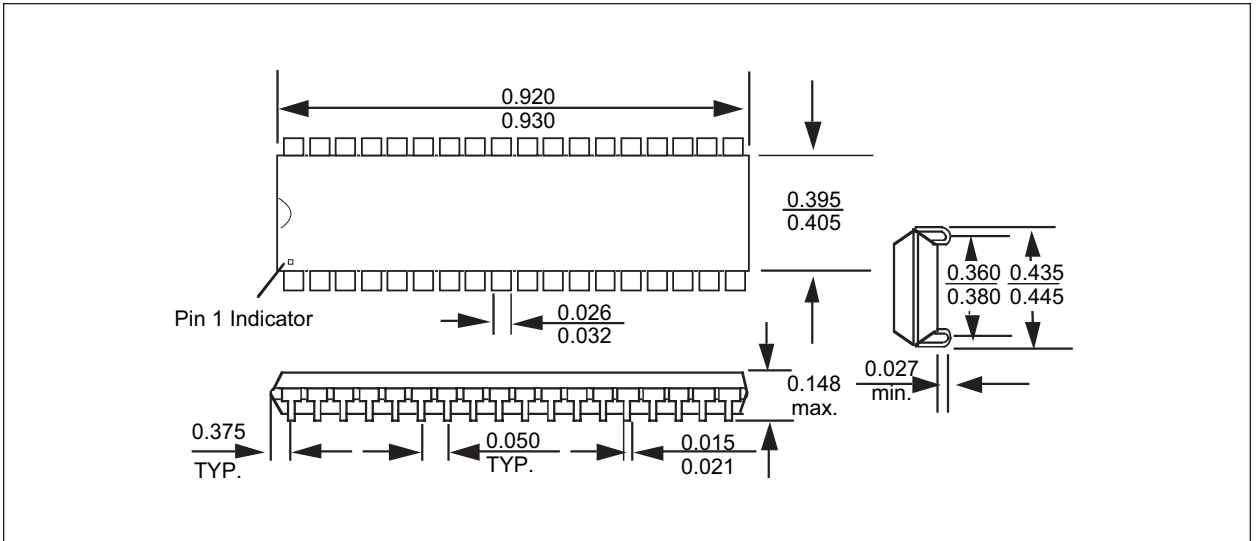


Normalized curves are offered as a service to our customers. They are not to be construed as a guarantee of operating characteristics.

Characteristics of actual devices will vary.



**PACKAGE 319: 36 LEAD, PLASTIC SMALL OUTLINE J-LEAD (SOJ)**



ALL DIMENSIONS ARE IN INCHES

**ORDERING INFORMATION**

