

## 32M-BIT ZEROSB™ SRAM

### FLOW THROUGH OPERATION

#### Description

The  $\mu$ PD44321181 is a 2,097,152-word by 18-bit and the  $\mu$ PD44321361 is a 1,048,576-word by 36-bit ZEROSB static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The  $\mu$ PD44321181 and  $\mu$ PD44321361 are optimized to eliminate dead cycles for read to write, or write to read transitions. These ZEROSB static RAMs integrate unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core. All input registers are controlled by a positive edge of the single clock input (CLK).

The  $\mu$ PD44321181 and  $\mu$ PD44321361 are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as buffer memory.

ZZ has to be set LOW at the normal operation. When ZZ is set HIGH, the SRAM enters Power Down State ("Sleep"). In the "Sleep" state, the SRAM internal state is preserved. When ZZ is set LOW again, the SRAM resumes normal operation.

The  $\mu$ PD44321181 and  $\mu$ PD44321361 are packaged in 100-pin PLASTIC LQFP with a 1.4 mm package thickness for high density and low capacitive loading.

#### Features

- Low voltage core supply:  $V_{DD} = 3.3 \pm 0.165 \text{ V} / 2.5 \pm 0.125 \text{ V}$
- Synchronous operation
- Operating temperature :  $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$  (-A75, -A85)  
 $T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$  (-A75Y, -A85Y)
- 100 percent bus utilization
- Internally self-timed write control
- Burst read / write : Interleaved burst and linear burst sequence
- Fully registered inputs and outputs for flow through operation
- All registers triggered off positive clock edge
- 3.3V or 2.5V LVTTTL Compatible : All inputs and outputs
- Fast clock access time : 7.5 ns (117 MHz), 8.5 ns (100 MHz)
- Asynchronous output enable : /G
- Burst sequence selectable : MODE
- Sleep mode : ZZ (ZZ = Open or Low : Normal operation)
- Separate byte write enable : /BW1 to /BW4 ( $\mu$ PD44321361)  
/BW1 and /BW2 ( $\mu$ PD44321181)
- Three chip enables for easy depth expansion
- Common I/O using three state outputs

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Ordering Information

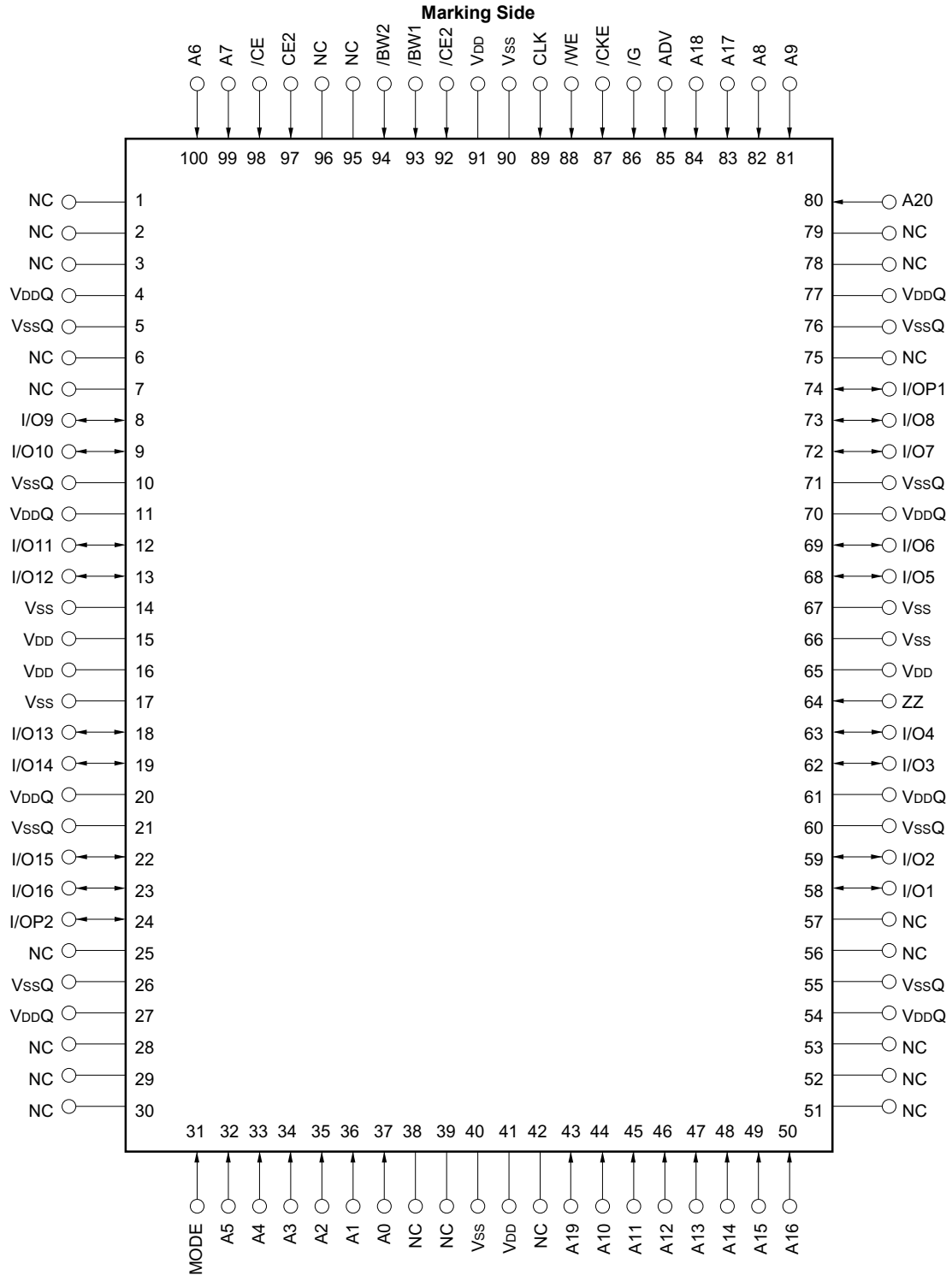
| Part number                        | Access Time<br>ns | Clock Frequency<br>MHz | Core Supply Voltage<br>V | I/O Interface         | Operating Temperature<br>°C | Package                           |
|------------------------------------|-------------------|------------------------|--------------------------|-----------------------|-----------------------------|-----------------------------------|
| μPD44321181GF-A75                  | 7.5               | 117                    | 3.3 ± 0.165              | 3.3 V or 2.5 V LVTTTL | 0 to 70                     | 100-pin PLASTIC<br>LQFP (14 x 20) |
|                                    |                   |                        | 2.5 ± 0.125              | 2.5 V LVTTTL          |                             |                                   |
| μPD44321181GF-A85                  | 8.5               | 100                    | 3.3 ± 0.165              | 3.3 V or 2.5 V LVTTTL |                             |                                   |
|                                    |                   |                        | 2.5 ± 0.125              | 2.5 V LVTTTL          |                             |                                   |
| μPD44321361GF-A75                  | 7.5               | 117                    | 3.3 ± 0.165              | 3.3 V or 2.5 V LVTTTL |                             |                                   |
|                                    |                   |                        | 2.5 ± 0.125              | 2.5 V LVTTTL          |                             |                                   |
| μPD44321361GF-A85                  | 8.5               | 100                    | 3.3 ± 0.165              | 3.3 V or 2.5 V LVTTTL |                             |                                   |
|                                    |                   |                        | 2.5 ± 0.125              | 2.5 V LVTTTL          |                             |                                   |
| μPD44321181GF-A75Y <sup>Note</sup> | 7.5               | 117                    | 3.3 ± 0.165              | 3.3 V or 2.5 V LVTTTL | -40 to +85                  |                                   |
|                                    |                   |                        | 2.5 ± 0.125              | 2.5 V LVTTTL          |                             |                                   |
| μPD44321181GF-A85Y <sup>Note</sup> | 8.5               | 100                    | 3.3 ± 0.165              | 3.3 V or 2.5 V LVTTTL |                             |                                   |
|                                    |                   |                        | 2.5 ± 0.125              | 2.5 V LVTTTL          |                             |                                   |
| μPD44321361GF-A75Y <sup>Note</sup> | 7.5               | 117                    | 3.3 ± 0.165              | 3.3 V or 2.5 V LVTTTL |                             |                                   |
|                                    |                   |                        | 2.5 ± 0.125              | 2.5 V LVTTTL          |                             |                                   |
| μPD44321361GF-A85Y <sup>Note</sup> | 8.5               | 100                    | 3.3 ± 0.165              | 3.3 V or 2.5 V LVTTTL |                             |                                   |
|                                    |                   |                        | 2.5 ± 0.125              | 2.5 V LVTTTL          |                             |                                   |

**Note** Under development

Pin Configurations

/xxx indicates active low signal.

100-pin PLASTIC LQFP (14 × 20)  
[μPD44321181GF]



**Remark** Refer to **Package Drawing** for the 1-pin index mark.

Pin Identifications

[μPD44321181GF]

| Symbol           | Pin No.                                                                                | Description                                                                                                            |
|------------------|----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|
| A0 to A20        | 37, 36, 35, 34, 33, 32, 100, 99, 82, 81,<br>44, 45, 46, 47, 48, 49, 50, 83, 84, 43, 80 | Synchronous Address Input                                                                                              |
| I/O1 to I/O16    | 58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13,<br>18, 19, 22, 23                        | Synchronous Data In,<br>Synchronous / Asynchronous Data Out                                                            |
| I/OP1, I/OP2     | 74, 24                                                                                 | Synchronous Data In (Parity),<br>Synchronous / Asynchronous Data Out (Parity)                                          |
| ADV              | 85                                                                                     | Synchronous Address Load / Advance Input                                                                               |
| /CE, CE2, /CE2   | 98, 97, 92                                                                             | Synchronous Chip Enable Input                                                                                          |
| /WE              | 88                                                                                     | Synchronous Write Enable Input                                                                                         |
| /BW1, /BW2       | 93, 94                                                                                 | Synchronous Byte Write Enable Input                                                                                    |
| /G               | 86                                                                                     | Asynchronous Output Enable Input                                                                                       |
| CLK              | 89                                                                                     | Clock Input                                                                                                            |
| /CKE             | 87                                                                                     | Synchronous Clock Enable Input                                                                                         |
| MODE             | 31                                                                                     | Asynchronous Burst Sequence Select Input<br>Have to tied to V <sub>DD</sub> or V <sub>SS</sub> during normal operation |
| ZZ               | 64                                                                                     | Asynchronous Power Down State Input                                                                                    |
| V <sub>DD</sub>  | 15, 16, 41, 65, 91                                                                     | Power Supply                                                                                                           |
| V <sub>SS</sub>  | 14, 17, 40, 66, 67, 90                                                                 | Ground                                                                                                                 |
| V <sub>DDQ</sub> | 4, 11, 20, 27, 54, 61, 70, 77                                                          | Output Buffer Power Supply                                                                                             |
| V <sub>SSQ</sub> | 5, 10, 21, 26, 55, 60, 71, 76                                                          | Output Buffer Ground                                                                                                   |
| NC               | 1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42,<br>51, 52, 53, 56, 57, 75, 78, 79, 95, 96   | No Connection                                                                                                          |



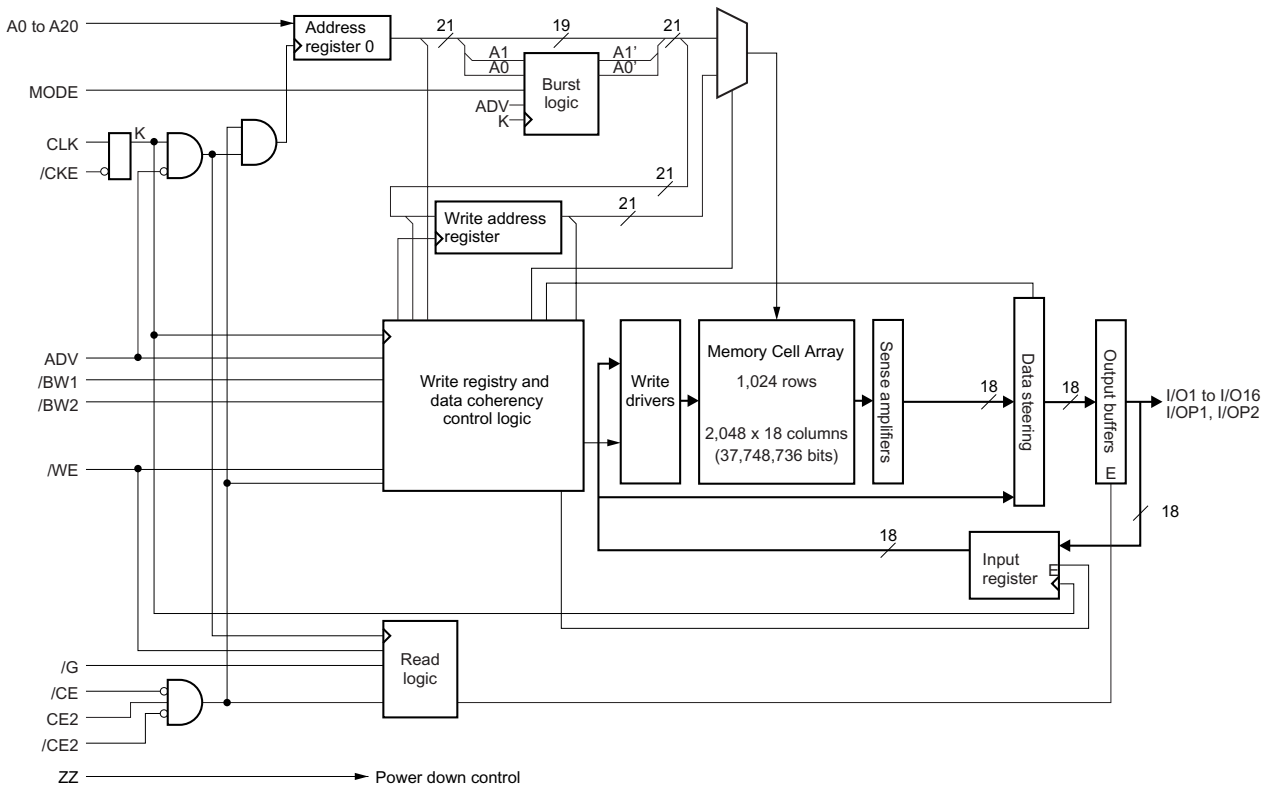
Pin Identifications

[μPD44321361GF]

| Symbol           | Pin No.                                                                                                                        | Description                                                                                                            |
|------------------|--------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|
| A0 to A19        | 37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44,<br>45, 46, 47, 48, 49, 50, 83, 84, 43                                             | Synchronous Address Input                                                                                              |
| I/O1 to I/O32    | 52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72,<br>73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13,<br>18, 19, 22, 23, 24, 25, 28, 29 | Synchronous Data In,<br>Synchronous / Asynchronous Data Out                                                            |
| I/OP1 to I/OP4   | 51, 80, 1, 30                                                                                                                  | Synchronous Data In (Parity),<br>Synchronous / Asynchronous Data Out (Parity)                                          |
| ADV              | 85                                                                                                                             | Synchronous Address Load / Advance Input                                                                               |
| /CE, CE2, /CE2   | 98, 97, 92                                                                                                                     | Synchronous Chip Enable Input                                                                                          |
| /WE              | 88                                                                                                                             | Synchronous Write Enable Input                                                                                         |
| /BW1 to /BW4     | 93, 94, 95, 96                                                                                                                 | Synchronous Byte Write Enable Input                                                                                    |
| /G               | 86                                                                                                                             | Asynchronous Output Enable Input                                                                                       |
| CLK              | 89                                                                                                                             | Clock Input                                                                                                            |
| /CKE             | 87                                                                                                                             | Synchronous Clock Enable Input                                                                                         |
| MODE             | 31                                                                                                                             | Asynchronous Burst Sequence Select Input<br>Have to tied to V <sub>DD</sub> or V <sub>SS</sub> during normal operation |
| ZZ               | 64                                                                                                                             | Asynchronous Power Down State Input                                                                                    |
| V <sub>DD</sub>  | 15, 16, 41, 65, 91                                                                                                             | Power Supply                                                                                                           |
| V <sub>SS</sub>  | 14, 17, 40, 66, 67, 90                                                                                                         | Ground                                                                                                                 |
| V <sub>DDQ</sub> | 4, 11, 20, 27, 54, 61, 70, 77                                                                                                  | Output Buffer Power Supply                                                                                             |
| V <sub>SSQ</sub> | 5, 10, 21, 26, 55, 60, 71, 76                                                                                                  | Output Buffer Ground                                                                                                   |
| NC               | 38, 39, 42                                                                                                                     | No Connection                                                                                                          |

Block Diagrams

[μPD44321181]



Burst Sequence

[μPD44321181]

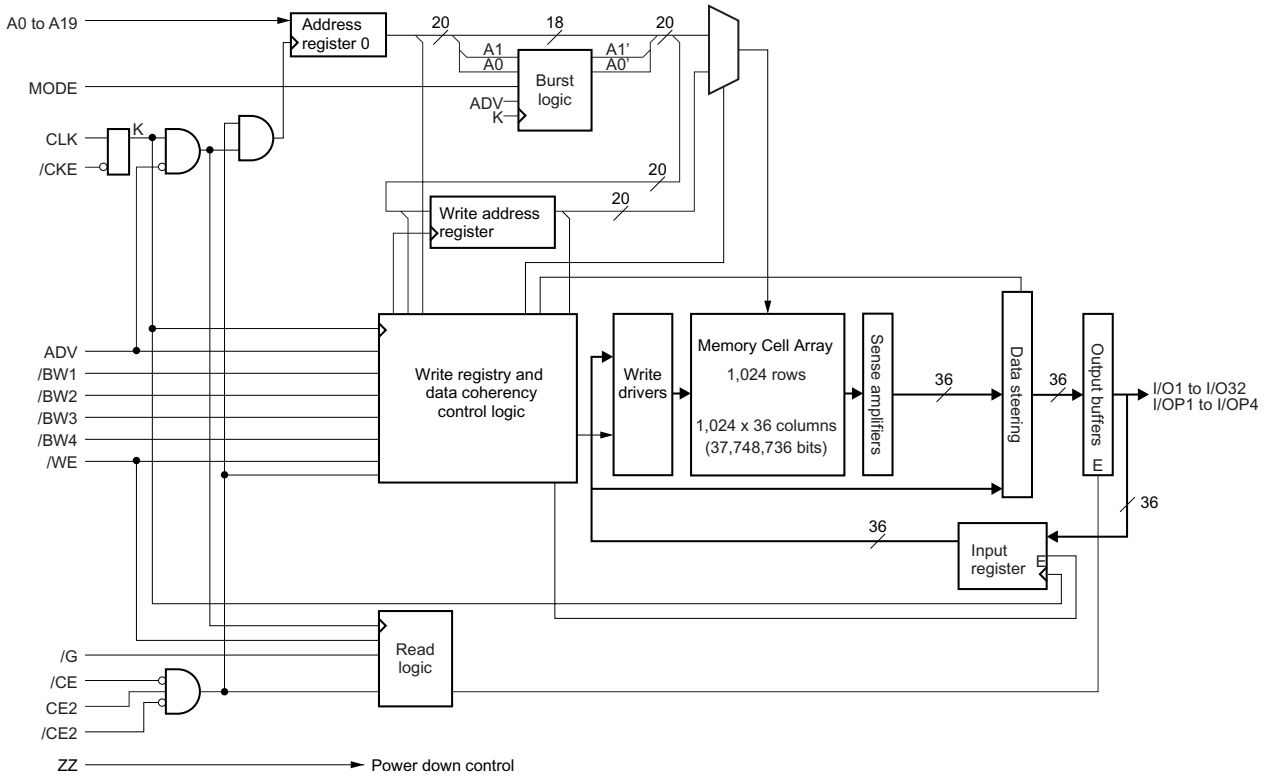
Interleaved Burst Sequence Table (MODE = V<sub>DD</sub>)

|                   |                     |
|-------------------|---------------------|
| External Address  | A20 to A2, A1, A0   |
| 1st Burst Address | A20 to A2, A1, /A0  |
| 2nd Burst Address | A20 to A2, /A1, A0  |
| 3rd Burst Address | A20 to A2, /A1, /A0 |

Linear Burst Sequence Table (MODE = V<sub>SS</sub>)

|                   |                 |                 |                 |                 |
|-------------------|-----------------|-----------------|-----------------|-----------------|
| External Address  | A20 to A2, 0, 0 | A20 to A2, 0, 1 | A20 to A2, 1, 0 | A20 to A2, 1, 1 |
| 1st Burst Address | A20 to A2, 0, 1 | A20 to A2, 1, 0 | A20 to A2, 1, 1 | A20 to A2, 0, 0 |
| 2nd Burst Address | A20 to A2, 1, 0 | A20 to A2, 1, 1 | A20 to A2, 0, 0 | A20 to A2, 0, 1 |
| 3rd Burst Address | A20 to A2, 1, 1 | A20 to A2, 0, 0 | A20 to A2, 0, 1 | A20 to A2, 1, 0 |

[μPD44321361]



**Burst Sequence**

[μPD44321361]

**Interleaved Burst Sequence Table (MODE = V<sub>DD</sub>)**

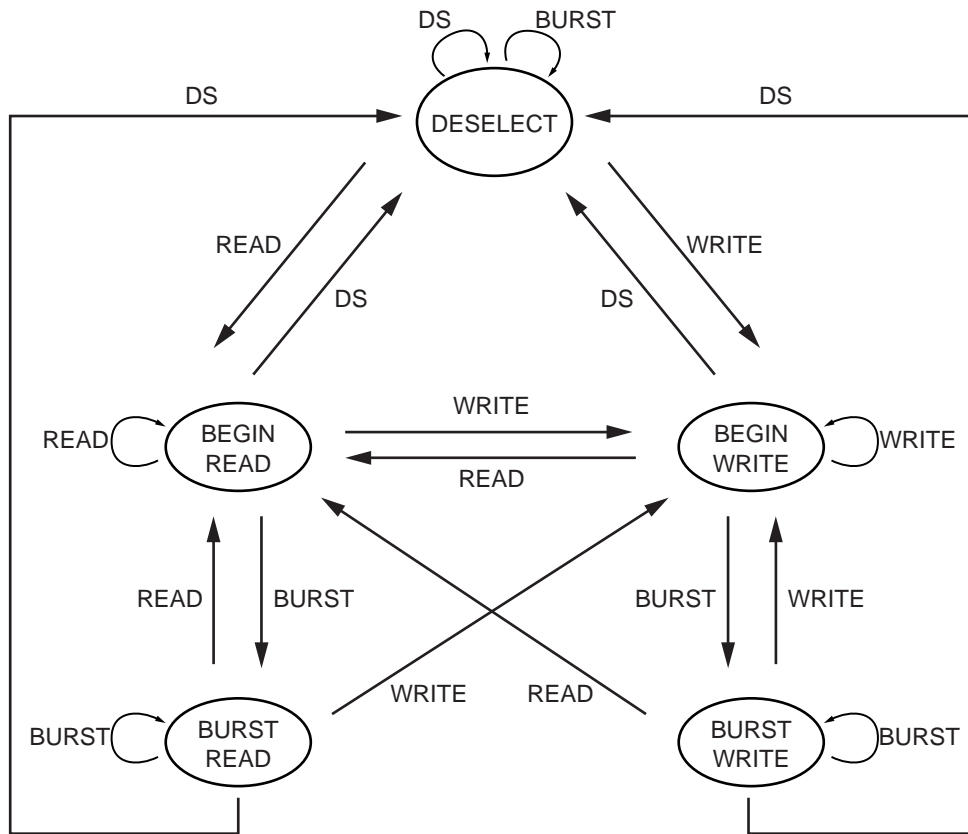
|                   |                     |
|-------------------|---------------------|
| External Address  | A19 to A2, A1, A0   |
| 1st Burst Address | A19 to A2, A1, /A0  |
| 2nd Burst Address | A19 to A2, /A1, A0  |
| 3rd Burst Address | A19 to A2, /A1, /A0 |

**Linear Burst Sequence Table (MODE = V<sub>SS</sub>)**

|                   |                 |                 |                 |                 |
|-------------------|-----------------|-----------------|-----------------|-----------------|
| External Address  | A19 to A2, 0, 0 | A19 to A2, 0, 1 | A19 to A2, 1, 0 | A19 to A2, 1, 1 |
| 1st Burst Address | A19 to A2, 0, 1 | A19 to A2, 1, 0 | A19 to A2, 1, 1 | A19 to A2, 0, 0 |
| 2nd Burst Address | A19 to A2, 1, 0 | A19 to A2, 1, 1 | A19 to A2, 0, 0 | A19 to A2, 0, 1 |
| 3rd Burst Address | A19 to A2, 1, 1 | A19 to A2, 0, 0 | A19 to A2, 0, 1 | A19 to A2, 1, 0 |



State Diagram



| Command | Operation                                    |
|---------|----------------------------------------------|
| DS      | Deselect                                     |
| Read    | New Read                                     |
| Write   | New Write                                    |
| Burst   | Burst Read, Burst Write or Continue Deselect |

- Remarks**
- States change on the rising edge of the clock.
  - A Stall or Ignore Clock Edge cycle is not shown in the above diagram. This is because /CKE HIGH only blocks the clock (CLK) input and does not change the state of the device.

**Asynchronous Truth Table**

| Operation   | /G | I/O             |
|-------------|----|-----------------|
| Read Cycle  | L  | Data-Out        |
| Read Cycle  | H  | High-Z          |
| Write Cycle | ×  | High-Z, Data-In |
| Deselected  | ×  | High-Z          |

**Remark** × : don't care

**Synchronous Truth Table**

| Operation                    | /CE | CE2 | /CE2 | ADV | /WE | /BWs | /CKE | CLK   | I/O      | Address  | Note |
|------------------------------|-----|-----|------|-----|-----|------|------|-------|----------|----------|------|
| Deselected                   | H   | ×   | ×    | L   | ×   | ×    | L    | L → H | High-Z   | None     | 1    |
| Deselected                   | ×   | L   | ×    | L   | ×   | ×    | L    | L → H | High-Z   | None     | 1    |
| Deselected                   | ×   | ×   | H    | L   | ×   | ×    | L    | L → H | High-Z   | None     | 1    |
| Continue Deselected          | ×   | ×   | ×    | H   | ×   | ×    | L    | L → H | High-Z   | None     | 1    |
| Read Cycle / Begin Burst     | L   | H   | L    | L   | H   | ×    | L    | L → H | Data-Out | External |      |
| Read Cycle / Continue Burst  | ×   | ×   | ×    | H   | ×   | ×    | L    | L → H | Data-Out | Next     |      |
| Write Cycle / Begin Burst    | L   | H   | L    | L   | L   | L    | L    | L → H | Data-In  | External |      |
| Write Cycle / Continue Burst | ×   | ×   | ×    | H   | ×   | L    | L    | L → H | Data-In  | Next     |      |
| Write Cycle / Write Abort    | L   | H   | L    | L   | L   | H    | L    | L → H | High-Z   | External |      |
| Write Cycle / Write Abort    | ×   | ×   | ×    | H   | ×   | H    | L    | L → H | High-Z   | Next     |      |
| Stall / Ignore Clock Edge    | ×   | ×   | ×    | ×   | ×   | ×    | H    | L → H | –        | Current  | 2    |

- Notes**
1. Deselect status is held until new "Begin Burst" entry.
  2. If an Ignore Clock Edge command occurs during a read operation, the I/O bus will remain active (Low impedance). If it occurs during a write cycle, the bus will remain High impedance. No write operation will be performed during the Ignore Clock Edge cycle.

- Remarks**
1. × : don't care
  2. /BWs = L means any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) are LOW.  
/BWs = H means all byte write enables (/BW1, /BW2, /BW3 or /BW4) are HIGH.

Partial Truth Table for Write Enables

[μPD44321181]

| Operation                                | /WE | /BW1 | /BW2 |
|------------------------------------------|-----|------|------|
| Read Cycle                               | H   | ×    | ×    |
| Write Cycle / Byte 1 (I/O [1:8], I/OP1)  | L   | L    | H    |
| Write Cycle / Byte 2 (I/O [9:16], I/OP2) | L   | H    | L    |
| Write Cycle / All Bytes                  | L   | L    | L    |
| Write Abort / NOP                        | L   | H    | H    |

Remark × : don't care

[μPD44321361]

| Operation                                 | /WE | /BW1 | /BW2 | /BW3 | /BW4 |
|-------------------------------------------|-----|------|------|------|------|
| Read Cycle                                | H   | ×    | ×    | ×    | ×    |
| Write Cycle / Byte 1 (I/O [1:8], I/OP1)   | L   | L    | H    | H    | H    |
| Write Cycle / Byte 2 (I/O [9:16], I/OP2)  | L   | H    | L    | H    | H    |
| Write Cycle / Byte 3 (I/O [17:24], I/OP3) | L   | H    | H    | L    | H    |
| Write Cycle / Byte 4 (I/O [25:32], I/OP4) | L   | H    | H    | H    | L    |
| Write Cycle / All Bytes                   | L   | L    | L    | L    | L    |
| Write Abort / NOP                         | L   | H    | H    | H    | H    |

Remark × : don't care

ZZ (Sleep) Truth Table

| ZZ                        | Chip Status |
|---------------------------|-------------|
| ≤ 0.2 V                   | Active      |
| Open                      | Active      |
| ≥ V <sub>DD</sub> - 0.2 V | Sleep       |

**Electrical Specifications**

**Absolute Maximum Ratings**

| Parameter                     | Symbol           | Conditions   | MIN.                 | TYP. | MAX.                   | Unit |
|-------------------------------|------------------|--------------|----------------------|------|------------------------|------|
| Supply voltage                | V <sub>DD</sub>  |              | -0.5                 |      | +4.0                   | V    |
| Output supply voltage         | V <sub>DDQ</sub> |              | -0.5                 |      | V <sub>DD</sub>        | V    |
| Input voltage                 | V <sub>IN</sub>  |              | -0.5 <sup>Note</sup> |      | V <sub>DD</sub> + 0.5  | V    |
| Input / Output voltage        | V <sub>IO</sub>  |              | -0.5 <sup>Note</sup> |      | V <sub>DDQ</sub> + 0.5 | V    |
| Operating ambient temperature | T <sub>A</sub>   | -A75, -A85   | 0                    |      | 70                     | °C   |
|                               |                  | -A75Y, -A85Y | -40                  |      | +85                    |      |
| Storage temperature           | T <sub>stg</sub> |              | -55                  |      | +125                   | °C   |

**Note** -2.0 V (MIN.) (Pulse width : 2 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended DC Operating Conditions (V<sub>DD</sub> = 3.3 ± 0.165 V)**

(1/2)

| Parameter                     | Symbol           | Conditions | MIN.                 | TYP. | MAX.                   | Unit |
|-------------------------------|------------------|------------|----------------------|------|------------------------|------|
| Supply voltage                | V <sub>DD</sub>  |            | 3.135                | 3.3  | 3.465                  | V    |
| <b>2.5 V LVTTTL Interface</b> |                  |            |                      |      |                        |      |
| Output supply voltage         | V <sub>DDQ</sub> |            | 2.375                | 2.5  | 2.9                    | V    |
| High level input voltage      | V <sub>IH</sub>  |            | 1.7                  |      | V <sub>DDQ</sub> + 0.3 | V    |
| Low level input voltage       | V <sub>IL</sub>  |            | -0.3 <sup>Note</sup> |      | +0.7                   | V    |
| <b>3.3 V LVTTTL Interface</b> |                  |            |                      |      |                        |      |
| Output supply voltage         | V <sub>DDQ</sub> |            | 3.135                | 3.3  | 3.465                  | V    |
| High level input voltage      | V <sub>IH</sub>  |            | 2.0                  |      | V <sub>DDQ</sub> + 0.3 | V    |
| Low level input voltage       | V <sub>IL</sub>  |            | -0.3 <sup>Note</sup> |      | +0.8                   | V    |

**Note** -0.8 V (MIN.) (Pulse width : 2 ns)

**Recommended DC Operating Conditions (V<sub>DD</sub> = 2.5 ± 0.125 V)**

(2/2)

| Parameter                | Symbol           | Conditions | MIN.                 | TYP. | MAX.                   | Unit |
|--------------------------|------------------|------------|----------------------|------|------------------------|------|
| Supply voltage           | V <sub>DD</sub>  |            | 2.375                | 2.5  | 2.625                  | V    |
| Output supply voltage    | V <sub>DDQ</sub> |            | 2.375                | 2.5  | 2.625                  | V    |
| High level input voltage | V <sub>IH</sub>  |            | 1.7                  |      | V <sub>DDQ</sub> + 0.3 | V    |
| Low level input voltage  | V <sub>IL</sub>  |            | -0.3 <sup>Note</sup> |      | +0.7                   | V    |

**Note** -0.8 V (MIN.) (Pulse width : 2 ns)

**DC Characteristics (V<sub>DD</sub> = 3.3 ± 0.165 V or 2.5 ± 0.125 V)**

| Parameter                     | Symbol            | Test condition                                                                                                                                                 | MIN.        | TYP. | MAX. | Unit |
|-------------------------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|------|------|
| Input leakage current         | I <sub>LI</sub>   | V <sub>IN</sub> (except ZZ, MODE) = 0 V to V <sub>DD</sub>                                                                                                     | -2          |      | +2   | μA   |
| I/O leakage current           | I <sub>LO</sub>   | V <sub>I/O</sub> = 0 V to V <sub>DDQ</sub> , Outputs are disabled.                                                                                             | -2          |      | +2   | μA   |
| Operating supply current      | I <sub>DD</sub>   | Device selected, Cycle = MAX.                                                                                                                                  | -A75, -A75Y |      | 290  | mA   |
|                               |                   | V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub> , I <sub>I/O</sub> = 0 mA                                                               | -A85, -A85Y |      | 270  |      |
| Standby supply current        | I <sub>SB</sub>   | Device deselected, Cycle = 0 MHz,<br>V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub> , All inputs are static.                           |             |      | 70   | mA   |
|                               | I <sub>SB1</sub>  | Device deselected, Cycle = 0 MHz,<br>V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2 V,<br>V <sub>I/O</sub> ≤ 0.2 V, All inputs are static. |             |      | 60   |      |
|                               | I <sub>SB2</sub>  | Device deselected, Cycle = MAX.<br>V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub>                                                      |             |      | 110  |      |
| Power down supply current     | I <sub>SBZZ</sub> | ZZ ≥ V <sub>DD</sub> - 0.2 V, V <sub>I/O</sub> ≤ V <sub>DDQ</sub> + 0.2 V                                                                                      |             |      | 60   | mA   |
| <b>2.5 V LVTTTL Interface</b> |                   |                                                                                                                                                                |             |      |      |      |
| High level output voltage     | V <sub>OH</sub>   | I <sub>OH</sub> = -2.0 mA                                                                                                                                      | 1.7         |      |      | V    |
|                               |                   | I <sub>OH</sub> = -1.0 mA                                                                                                                                      | 2.1         |      |      |      |
| Low level output voltage      | V <sub>OL</sub>   | I <sub>OL</sub> = +2.0 mA                                                                                                                                      |             |      | 0.7  | V    |
|                               |                   | I <sub>OL</sub> = +1.0 mA                                                                                                                                      |             |      | 0.4  |      |
| <b>3.3 V LVTTTL Interface</b> |                   |                                                                                                                                                                |             |      |      |      |
| High level output voltage     | V <sub>OH</sub>   | I <sub>OH</sub> = -4.0 mA                                                                                                                                      | 2.4         |      |      | V    |
| Low level output voltage      | V <sub>OL</sub>   | I <sub>OL</sub> = +8.0 mA                                                                                                                                      |             |      | 0.4  | V    |

**Capacitance (T<sub>A</sub> = 25 °C, f = 1MHz)**

| Parameter                  | Symbol           | Test condition         | MIN. | TYP. | MAX. | Unit |
|----------------------------|------------------|------------------------|------|------|------|------|
| Input capacitance          | C <sub>IN</sub>  | V <sub>IN</sub> = 0 V  |      |      | 6.0  | pF   |
| Input / Output capacitance | C <sub>I/O</sub> | V <sub>I/O</sub> = 0 V |      |      | 8.0  | pF   |
| Clock input capacitance    | C <sub>clk</sub> | V <sub>clk</sub> = 0 V |      |      | 6.0  | pF   |

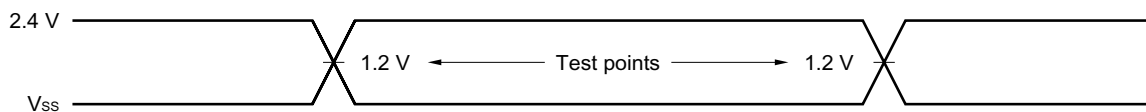
**Remark** These parameters are periodically sampled and not 100% tested.

AC Characteristics ( $V_{DD} = 3.3 \pm 0.165 \text{ V}$  or  $2.5 \pm 0.125 \text{ V}$ )

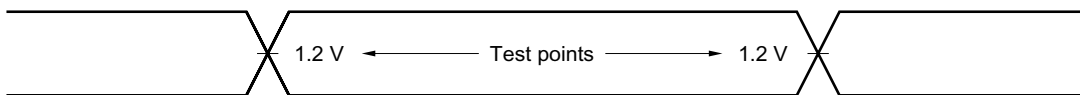
AC Test Conditions

2.5 V LVTTTL Interface

Input waveform (Rise / Fall time  $\leq 2.4 \text{ ns}$ )

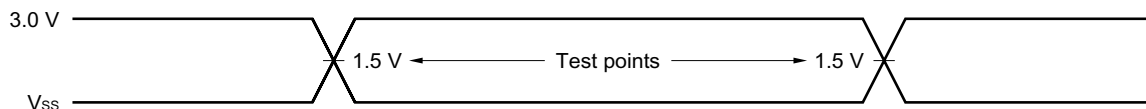


Output waveform

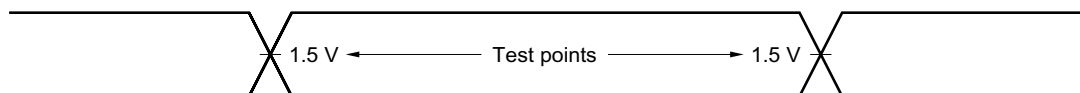


3.3 V LVTTTL Interface

Input waveform (Rise / Fall time  $\leq 3.0 \text{ ns}$ )



Output waveform

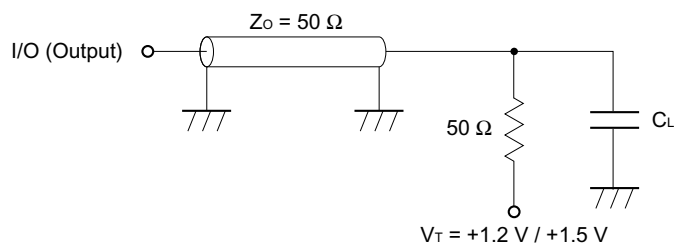


Output load condition

$C_L$ : 30 pF

5 pF (TKHQX1, TKHQX2, TGLQX, TGHQZ, TKHQZ)

Figure External load at test



Remark  $C_L$  includes capacitances of the probe and jig, and stray capacitances.

Read and Write Cycle

| Parameter                       | Symbol          |         | -A75, -A75Y<br>(117 MHz) |              | -A85, -A85Y<br>(100 MHz) |              | Unit     | Notes |
|---------------------------------|-----------------|---------|--------------------------|--------------|--------------------------|--------------|----------|-------|
|                                 | Standard        | Alias   | MIN.                     | MAX.         | MIN.                     | MAX.         |          |       |
| Cycle time                      | TKHKH           | TCYC    | 8.6                      | –            | 10                       | –            | ns       |       |
| Clock access time               | TKHQV           | TCD     | –                        | 7.5          | –                        | 8.5          | ns       |       |
| Output enable access time       | TGLQV           | TOE     | –                        | 3.5          | –                        | 3.5          | ns       |       |
| Clock high to output active     | TKHQX1          | TDC1    | 2.5                      | –            | 2.5                      | –            | ns       | 1, 2  |
| Clock high to output change     | TKHQX2          | TDC2    | 2.5                      | –            | 2.5                      | –            | ns       |       |
| Output enable to output active  | TGLQX           | TOLZ    | 0                        | –            | 0                        | –            | ns       | 1     |
| Output disable to output High-Z | TGHQZ           | TOHZ    | 0                        | 3.5          | 0                        | 3.5          | ns       | 1     |
| Clock high to output High-Z     | TKHQZ           | TCZ     | 2.5                      | 5            | 2.5                      | 5            | ns       | 1, 2  |
| Clock high pulse width          | TKHKL           | TCH     | 2.5                      | –            | 2.5                      | –            | ns       |       |
| Clock low pulse width           | TKLKH           | TCL     | 2.5                      | –            | 2.5                      | –            | ns       |       |
| Setup times                     | Address         | TAVKH   | TAS                      | 1.5          | –                        | 2            | –        | ns    |
|                                 | Address advance | TADVVKH | TADVS                    |              |                          |              |          |       |
|                                 | Clock enable    | TEVKH   | TCES                     |              |                          |              |          |       |
|                                 | Chip enable     | TCVKH   | TCSS                     |              |                          |              |          |       |
|                                 | Data in         | TDVKH   | TDS                      |              |                          |              |          |       |
|                                 | Write enable    | TWVKH   | TWS                      |              |                          |              |          |       |
| ★ Hold times                    | Address         | TKHAX   | TAH                      | 0.5<br>(1.0) | –<br>(–)                 | 0.5<br>(1.0) | –<br>(–) | ns    |
|                                 | Address advance | TKHADVX | TADVH                    |              |                          |              |          |       |
|                                 | Clock enable    | TKHEX   | TCEH                     |              |                          |              |          |       |
|                                 | Chip enable     | TKHCX   | TCSH                     |              |                          |              |          |       |
|                                 | Data in         | TKHDX   | TDH                      |              |                          |              |          |       |
|                                 | Write enable    | TKHWX   | TWH                      |              |                          |              |          |       |
| Power down entry time           | TZZE            | TZZE    | –                        | 8.6          | –                        | 10           | ns       |       |
| Power down recovery time        | TZZR            | TZZR    | –                        | 8.6          | –                        | 10           | ns       |       |

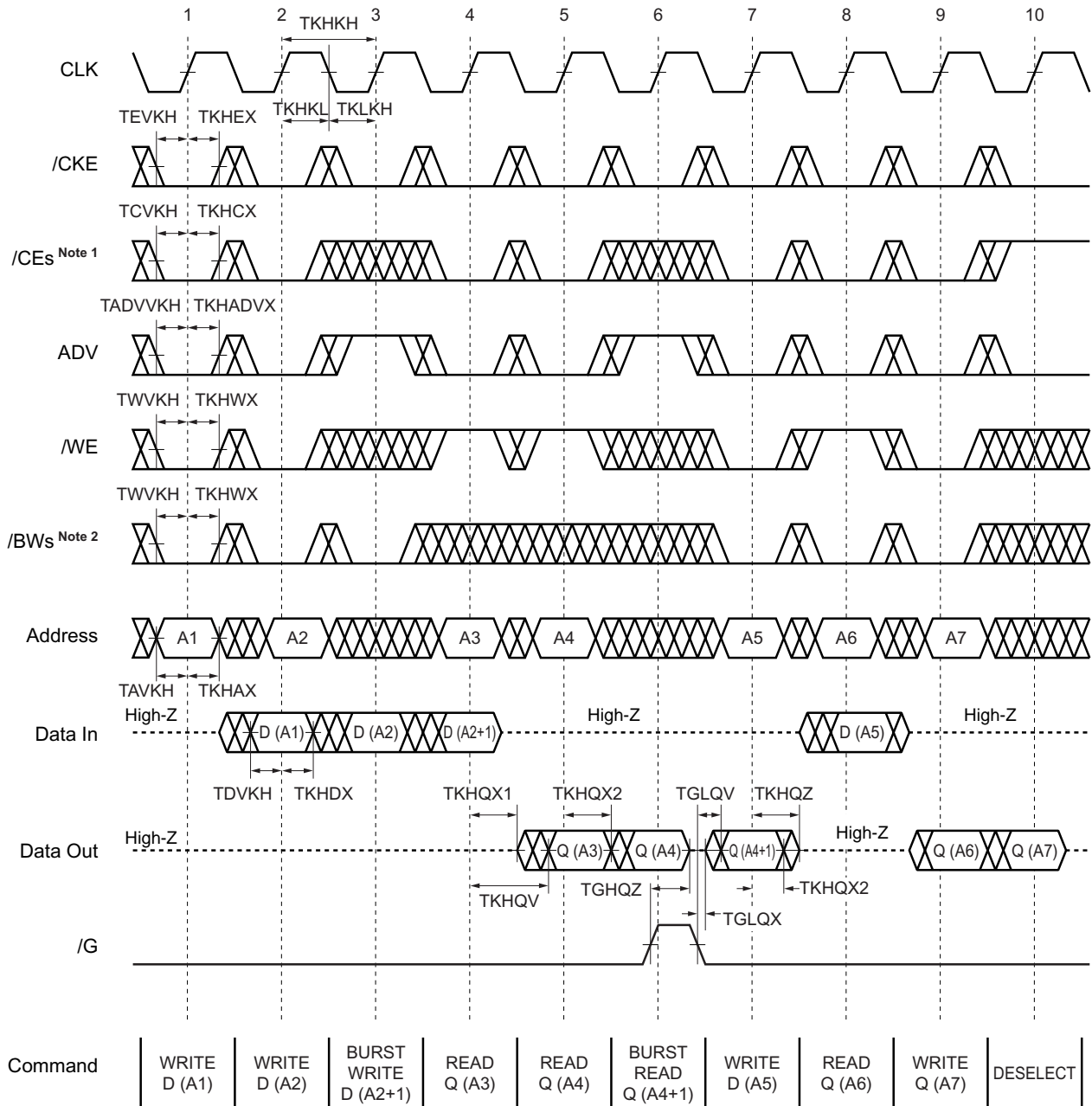
Notes 1. Transition is measured ±200 mV from steady state.

2. To avoid bus contention, the output buffers are designed such that TKHQZ (device turn-off) is faster than TKHQX1 (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because TKHQX1 is a min. parameter that is worse case at totally different conditions (T<sub>A</sub> min., V<sub>DD</sub> max.) than TKHQZ, which is a max. parameter (worse case at T<sub>A</sub> max., V<sub>DD</sub> min.).

★ 3. These values apply when V<sub>DD</sub> = 3.3 V ±0.165 V with a 3.3 V LVTTTL interface, or when V<sub>DD</sub> = 2.5 V ±0.125 V with a 2.5 V LVTTTL interface.

Values in parentheses apply when V<sub>DD</sub> = 3.3 V ±0.165 V with a 2.5 V LVTTTL interface.

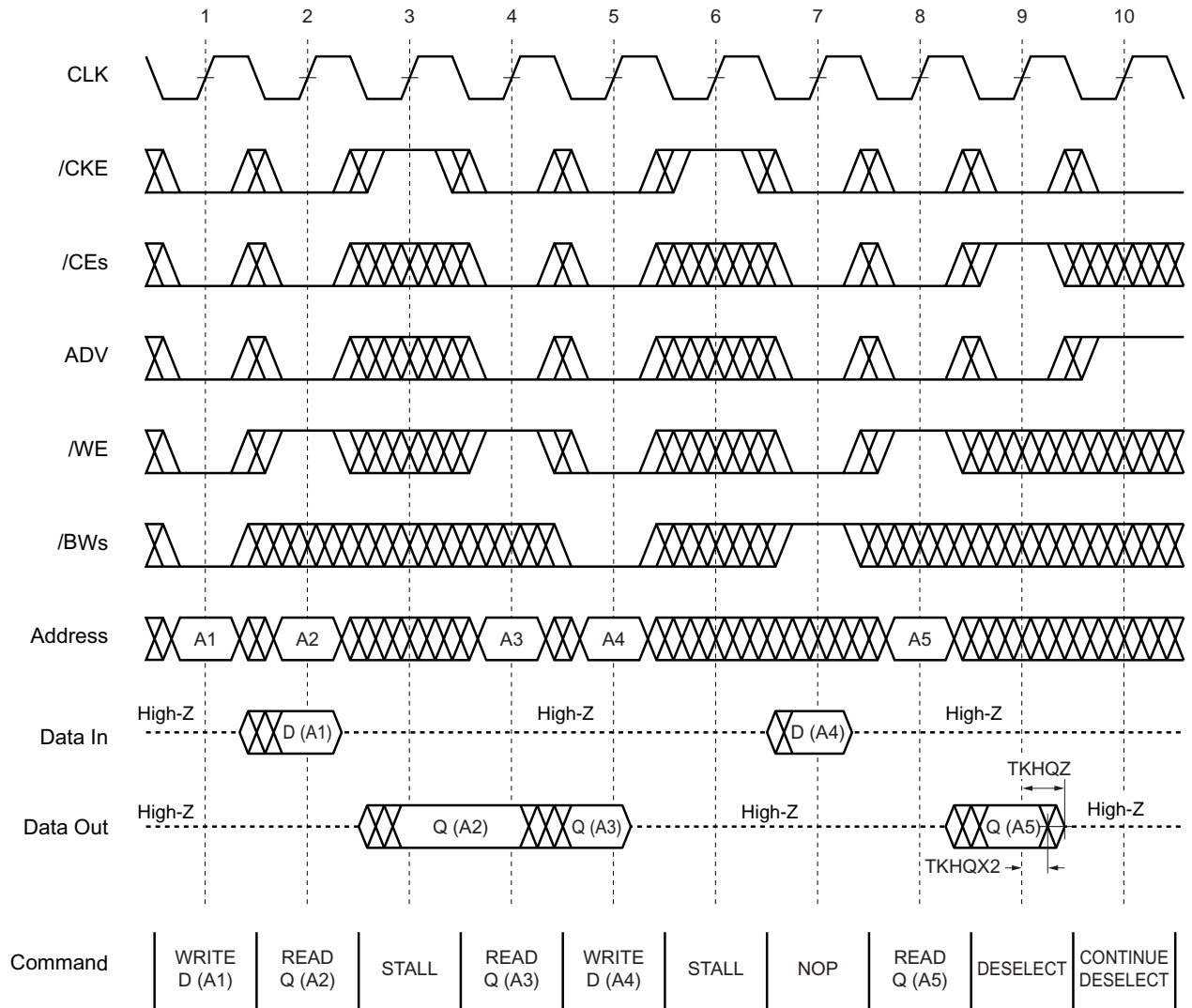
READ / WRITE CYCLE



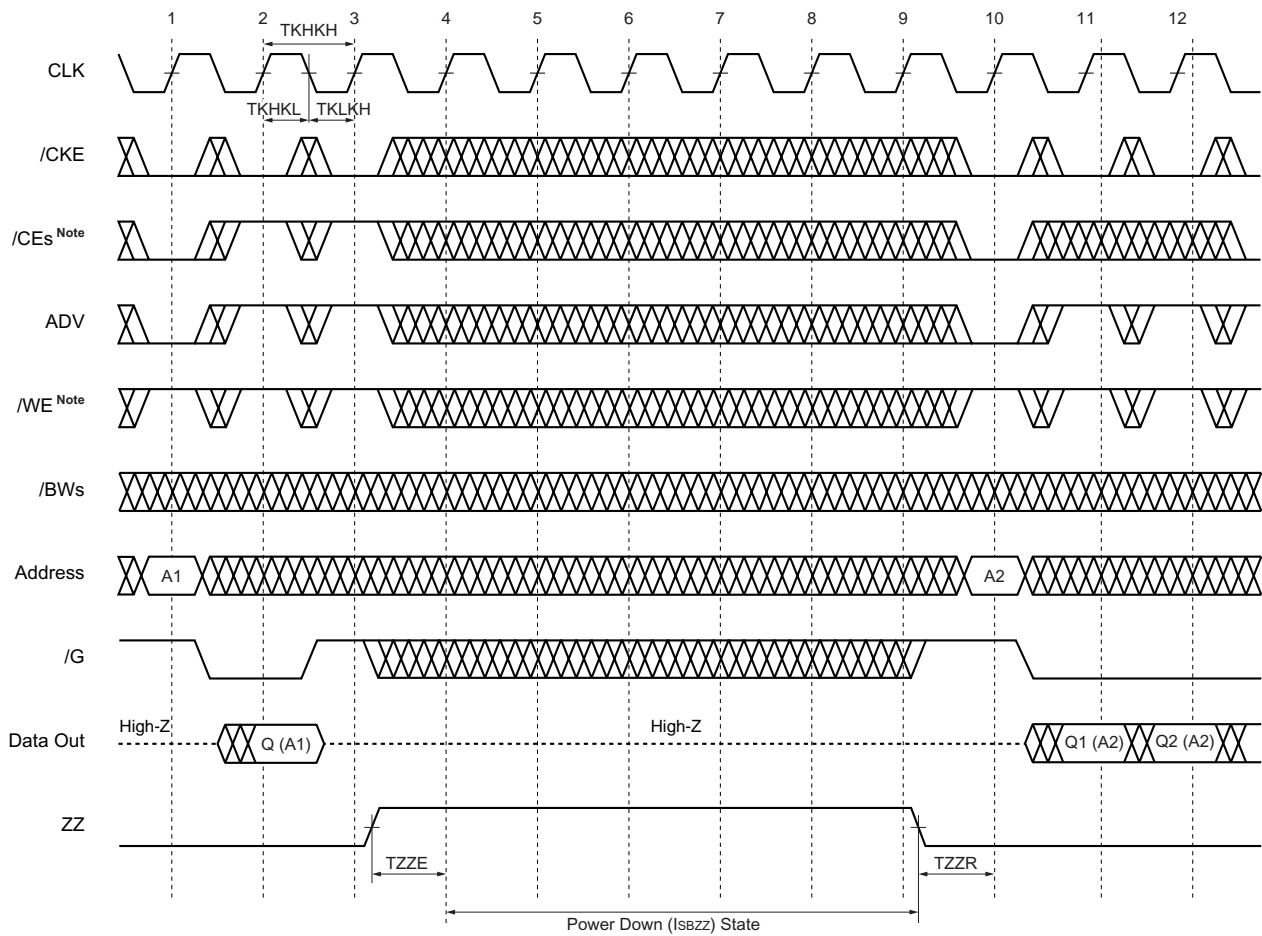
- Notes**
1. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.
  2. /BWs refers to /BW1, /BW2, /BW3 and /BW4. When /BWs is LOW, any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) are LOW.



NOP, STALL AND DESELECT CYCLE



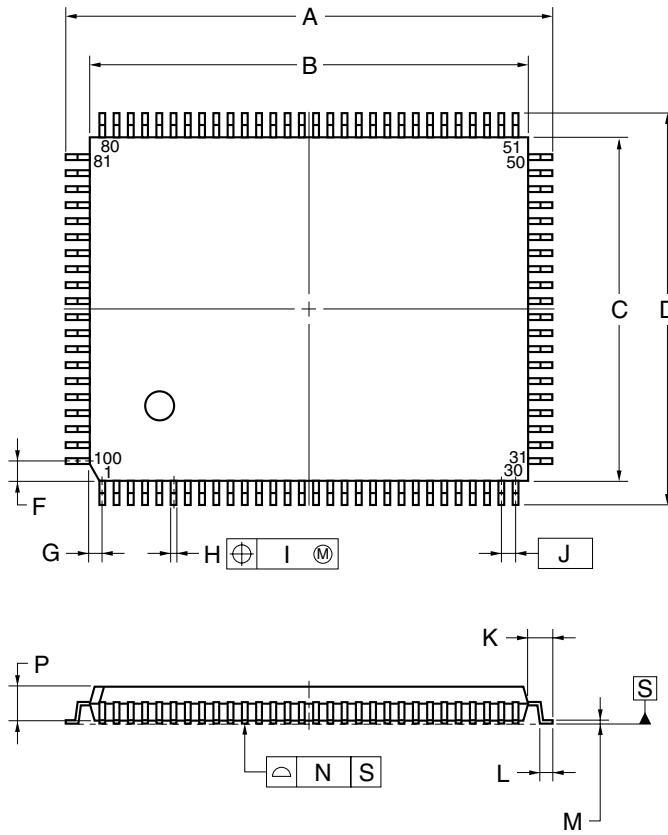
POWER DOWN (ZZ) CYCLE



**Note** /WE or /CEs must be held HIGH at CLK rising edge (clock edge No.3 in this figure) prior to power down state entry.

Package Drawing

100-PIN PLASTIC LQFP (14x20)



detail of lead end

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM                   | MILLIMETERS                            |
|------------------------|----------------------------------------|
| A                      | 22.0±0.2                               |
| B                      | 20.0±0.2                               |
| C                      | 14.0±0.2                               |
| D                      | 16.0±0.2                               |
| F                      | 0.825                                  |
| G                      | 0.575                                  |
| H                      | 0.32 <sup>+0.08</sup> <sub>-0.07</sub> |
| I                      | 0.13                                   |
| J                      | 0.65 (T.P.)                            |
| K                      | 1.0±0.2                                |
| L                      | 0.5±0.2                                |
| M                      | 0.17 <sup>+0.06</sup> <sub>-0.05</sub> |
| N                      | 0.10                                   |
| P                      | 1.4                                    |
| Q                      | 0.125±0.075                            |
| R                      | 3° <sup>+7°</sup> <sub>-3°</sub>       |
| S                      | 1.7 MAX.                               |
| <b>S100GF-65-8ET-1</b> |                                        |

**Recommended Soldering Condition**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD44321181 and  $\mu$ PD44321361.

**Types of Surface Mount Devices**

$\mu$ PD44321181GF : 100-pin PLASTIC LQFP (14 x 20)

$\mu$ PD44321361GF : 100-pin PLASTIC LQFP (14 x 20)

**Revision History**

| Edition/<br>Date          | Page            |                     | Type of<br>revision | Location                           | Description<br>(Previous edition → This edition)                                                                                   |
|---------------------------|-----------------|---------------------|---------------------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|
|                           | This<br>edition | Previous<br>edition |                     |                                    |                                                                                                                                    |
| 3rd edition/<br>Sep. 2003 | Throughout      | Throughout          | Addition            | -A75Y, -A85Y                       | "Note Under development" was added                                                                                                 |
|                           |                 |                     | Modification        | –                                  | Integrate -C75, -C85 to -A75, -A85                                                                                                 |
|                           |                 |                     | Deletion            | –                                  | -A65, -A65Y (133MHz)                                                                                                               |
| 4th edition/<br>Nov. 2003 | p.15            | p.15                | Modification        | Read and Write Cycle<br>Hold times | Values when $V_{DD} = 3.3\text{ V} \pm 0.165\text{ V}$ , with 2.5 V<br>LVTTTL interface have been added.<br>Note 3 has been added. |

[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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