

## 29F52•29F53 8-Bit Registered Transceiver

### General Description

The 29F52 and 29F53 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The A<sub>0</sub>-A<sub>7</sub> output pins are guaranteed to sink 24 mA (20 mA mil.) while the B<sub>0</sub>-B<sub>7</sub> output pins are designed for 64 mA.

The 29F53 is an inverting option of the 29F52. Both transceivers are AMD Am2952/2953 functional equivalents.

### Features

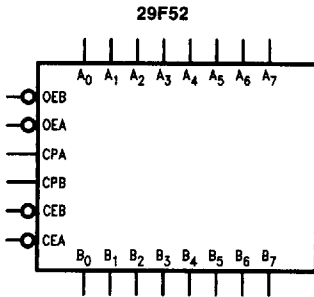
- 8-bit registered transceivers
- Separate clock, clock enable and TRI-STATE output enable provided for each register
- AMD Am2952/2953 functional equivalents
- Both inverting and non-inverting options available
- 24-Pin slimline package

### Ordering Code: See Section 11

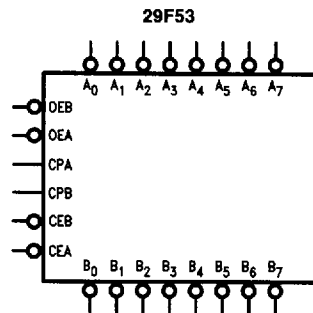
Commercial	Package Number	Package Description
29F52SPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
29F52SC (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
29F53SPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line

**Note 1:** Devices also available in 13" reel. Use suffix = SCX.

### Logic Symbols

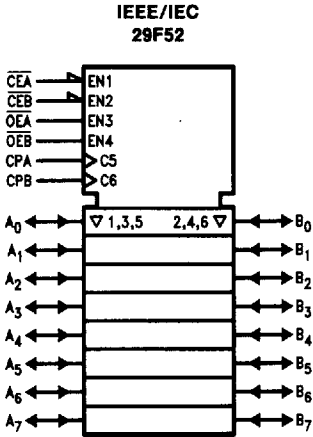


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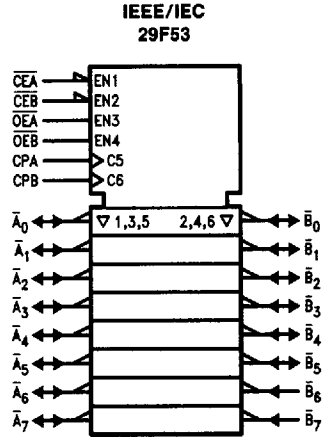


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**Logic Symbols (Continued)**



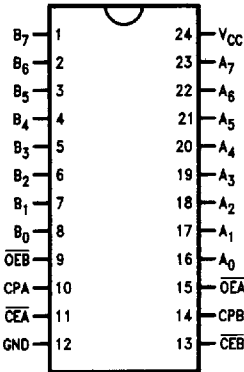
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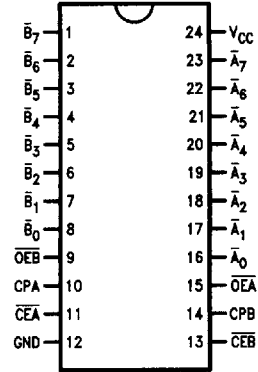
**Connection Diagrams**

**Pin Assignment for DIP and SOIC 29F52**



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**Pin Assignment for DIP 29F53**

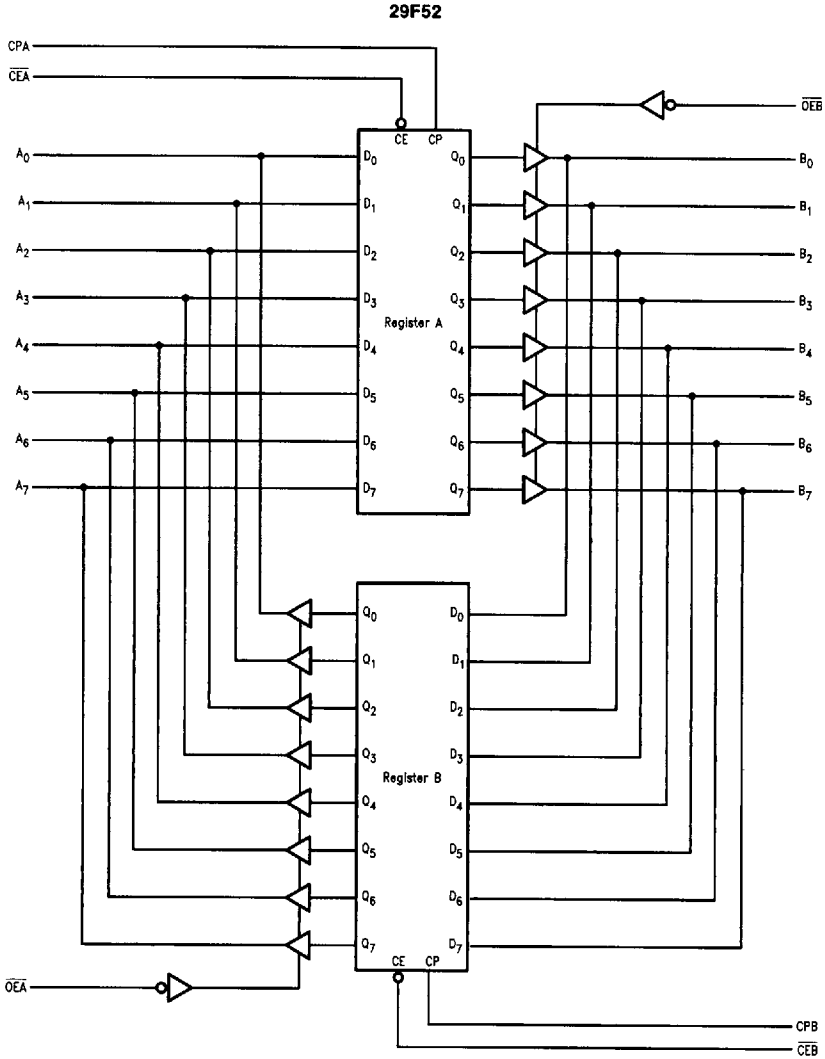


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**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

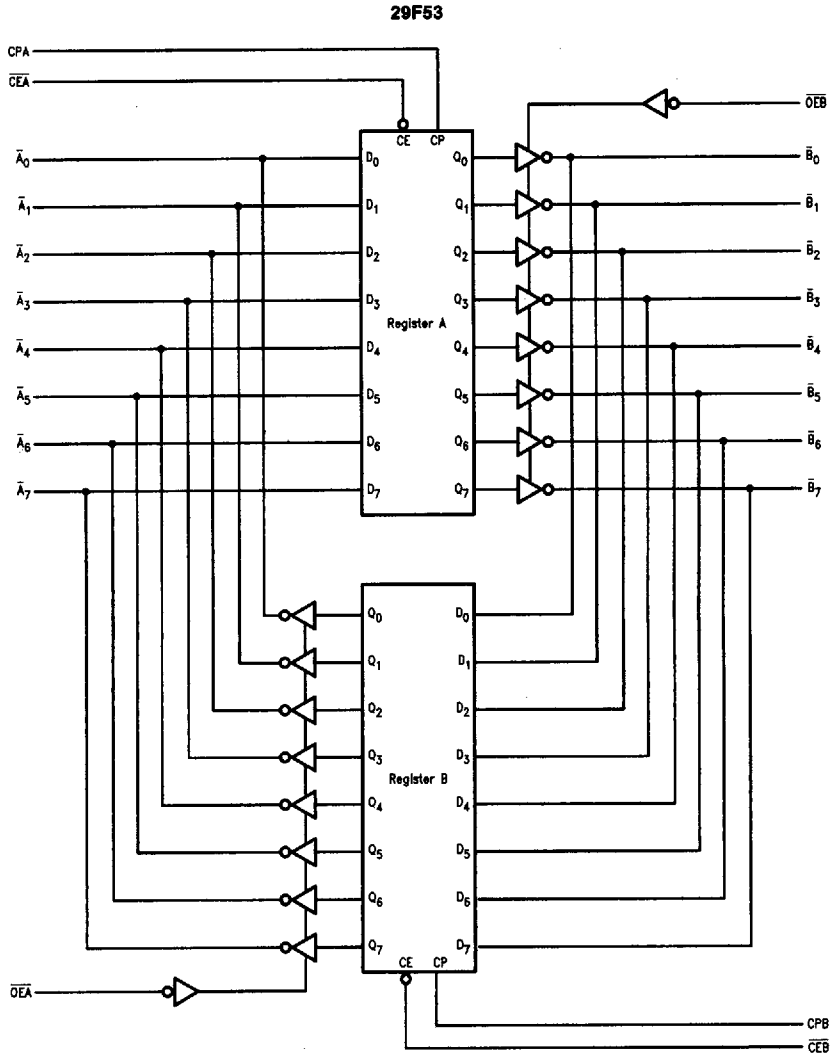
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> -A <sub>7</sub>	A-Register Inputs/ B-Register TRI-STATE Outputs	3.5/1.083 150/40 (33.3)	70 $\mu$ A/0.65 mA -3 mA/24 mA (20 mA)
B <sub>0</sub> -B <sub>7</sub>	B Register Inputs/ A-Register TRI-STATE Outputs	3.5/1.083 600/106.6 (80)	70 $\mu$ A/0.65 mA -12 mA/64 mA (48 mA)
OEA	Output Enable A-Register	1.0/1.0	20 $\mu$ A/-0.6 mA
CPA	A-Register Clock	1.0/1.0	20 $\mu$ A/-0.6 mA
CEA	A-Register Clock Enable	1.0/1.0	20 $\mu$ A/-0.6 mA
OEB	Output Enable B-Register	1.0/1.0	20 $\mu$ A/-0.6 mA
CPB	B-Register Clock	1.0/1.0	20 $\mu$ A/-0.6 mA
CEB	B-Register Clock Enable	1.0/1.0	20 $\mu$ A/-0.6 mA

# Block Diagrams



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**Block Diagrams (Continued)**



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**Output Control**

OE	Internal Q	Y-Output		Function
		29F52	29F53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

**Register Function Table (Applies to A or B Register)**

Inputs			Internal Q	Function
D	CP	CE		
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↘	L	H	

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = HIGH Impedance  
 ↗ = LOW-to-HIGH Transition  
 ↘ = HIGH-to-LOW Transition  
 NC = No Change

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = -12 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = -15 mA (B <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA (A <sub>n</sub> )
74F 5% V <sub>CC</sub>	2.7		I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )				
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 48 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA (B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current				μA	Max	V <sub>IN</sub> = 2.7V (Non-I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test				μA	Max	V <sub>IN</sub> = 7.0V (Non-I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)				mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current				mA	Max	V <sub>IN</sub> = 0.5V (Non-I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current				μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current				μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-60	-150		mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current				μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test				μA	0.0V	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current				mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current				mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current				mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{MII}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay CPA or CPB to $A_n$ or $B_n$	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	2-3
$t_{pZH}$ $t_{pZL}$	Output Enable Time $\overline{\text{OE}}A$ or $\overline{\text{OE}}B$ to $A_n$ or $B_n$	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{\text{OE}}A$ or $\overline{\text{OE}}B$ to $A_n$ or $B_n$	2.5 2.5	6.5 5.5	9.0 7.5			2.0 2.0	10.0 8.5	ns	2-5

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{MII}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $A_n$ or $B_n$ to CPA or CPB	4.0 4.0				4.5 4.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $A_n$ or $B_n$ to CPA or CPB	2.0 2.0				2.5 2.5		ns	2-6
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{\text{CE}}A$ or $\overline{\text{CE}}B$ to CPA or CPB	1.0 4.0				1.5 4.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{\text{CE}}A$ or $\overline{\text{CE}}B$ to CPA or CPB	2.0 2.0				2.5 2.5		ns	2-6
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0				3.5 3.5		ns	2-4