SD1730 (TH560)

RF POWER BIPOLAR TRANSISTORS
HF SSB APPLICATIONS

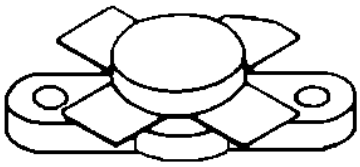
FEATURES SUMMARY

- OPTIMIZED FOR SSB
- 30 MHz
- 28 VOLTS
- IMD –30 dB
- EFFICIENCY 40%
- COMMON EMITTER
- GOLD METALLIZATION
- P_{OUT} = 220 W PEP WITH 12 dB GAIN

DESCRIPTION

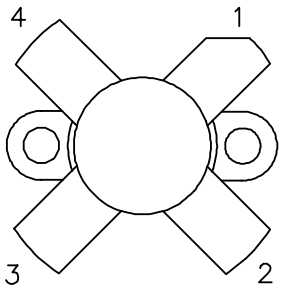
The SD1730 is a 28 V epitaxial silicon NPN planar transistor designed primarily for SSB and VHF communications. The devices utilizes emitter ballasting for improved ruggedness and reliability.

Figure 1. Package



.500 4L FL (M174)
epoxy sealed

Figure 2. Pin Connection



1. Collector
2. Emitter
3. Base
4. Emitter

Table 1. Order Codes

Order Codes	Marking	Package	Packaging
SD1730 (TH560)	SD1730	M174	PLASTIC TRAYS

Table 2. Absolute Maximum Ratings (T_{case} = 25°C)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	70	V
V_{CEO}	Collector-Emitter Voltage	35	V
V_{EBO}	Emitter-Base Voltage	4.0	V
I_C	Device Current	16	A
P_{DISS}	Power Dissipation	320	W
T_J	Junction Temperature	+200	°C
T_{STG}	Storage Temperature	– 65 to +150	°C

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Junction-Case Thermal Resistance	0.6	°C/W

ELECTRICAL SPECIFICATIONS (T_{case} = 25°C)

Table 4. Static

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
BV_{CES}	I_C = 100 mA; V_{BE} = 0 V	70	—	—	V
BV_{CEO}	I_C = 200 mA; I_B = 0 mA	35	—	—	V
BV_{EBO}	I_E = 20 mA; I_C = 0 mA	4.0	—	—	V
I_{CEO}	V_{CE} = 30 V; I_E = 0 mA	—	—	5	mA
I_{CES}	V_{CE} = 35 V; I_E = 0 mA	—	—	5	mA
h_{FE}	V_{CE} = 5 V; I_C = 7 A	15	—	60	—

Table 5. Dynamic

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
P_{OUT}	f = 30 MHz; V_{CE} = 28 V; I_{CQ} = 750 mA	220	—	—	W
P_G(1)	P_{OUT} = 220 W PEP; V_{CE} = 28 V; I_{CQ} = 750 mA	12	—	—	dB
IMD(1)	P_{OUT} = 220 W PEP; V_{CE} = 28 V; I_{CQ} = 750 mA	—	—	–30	dBc
η_c(1)	P_{OUT} = 220 W PEP; V_{CE} = 28 V; I_{CQ} = 750 mA	40	—	—	%
C_{OB}	f = 1 MHz; V_{CB} = 28 V	—	450	—	pF
Load Mismatch	P_{OUT} = 220 W PEP; V_{CE} = 28 V; I_{CQ} = 750 mA	—	∞:1	—	VSWR

Note: 1. f_1 = 30.00 MHz, f_2 = 30.001 MHz

TYPICAL PERFORMANCE

Figure 3. Power Output PEP vs Power Input

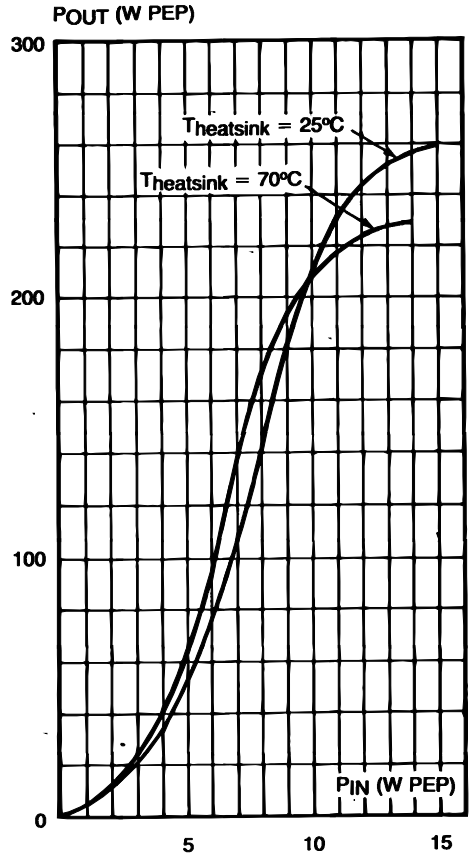


Figure 4. Collector Efficiency vs Power Output PEP

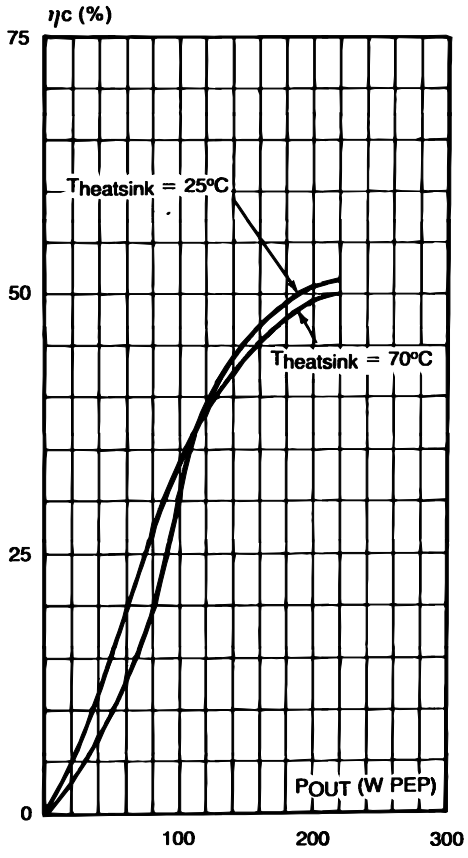


Figure 5. Intermodulation Distortion vs Power Output PEP

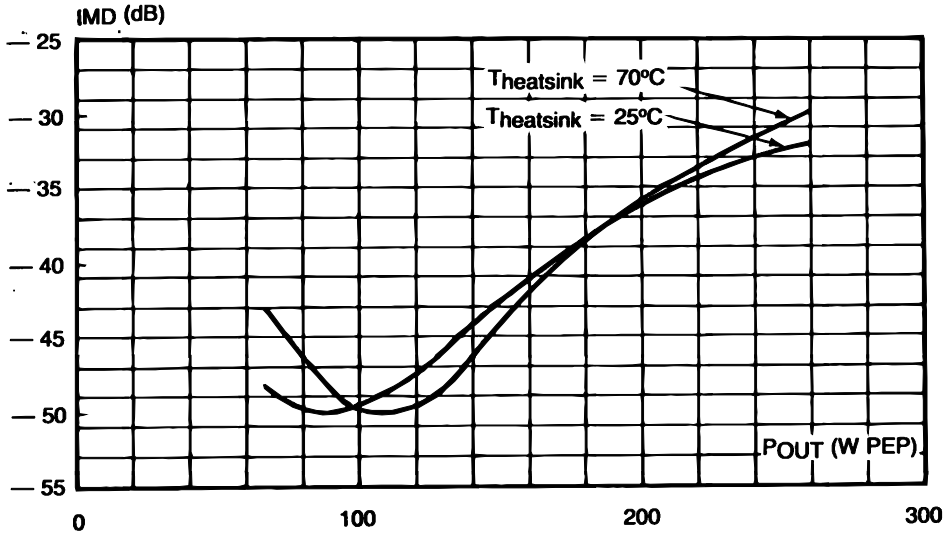


Figure 6. Power Gain vs Power Output

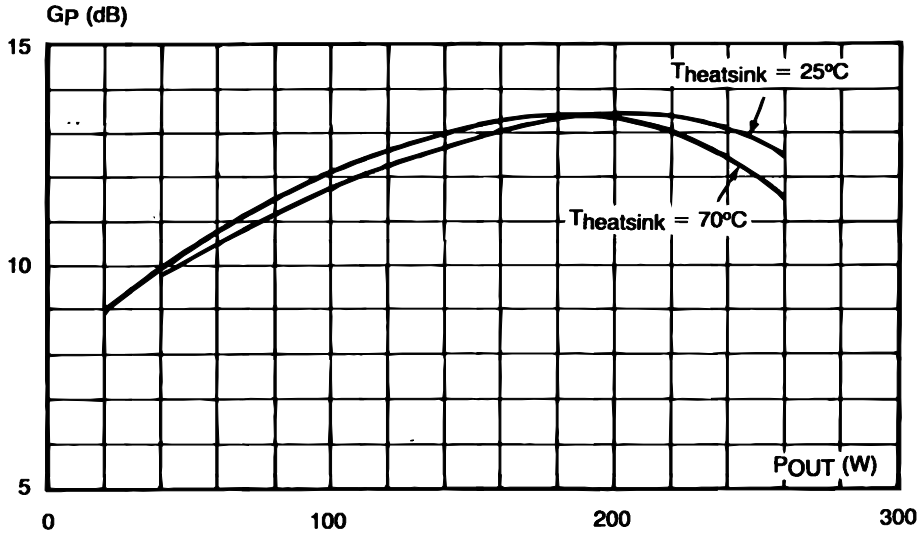


Table 6. Impedance Data

FREQ.	Z_{IN} (Ω)	Z_{CL} (Ω)
30 MHz	1.15 + j 0.41	1.25 + j 1.92

TEST CIRCUIT

Figure 7. Test Circuit

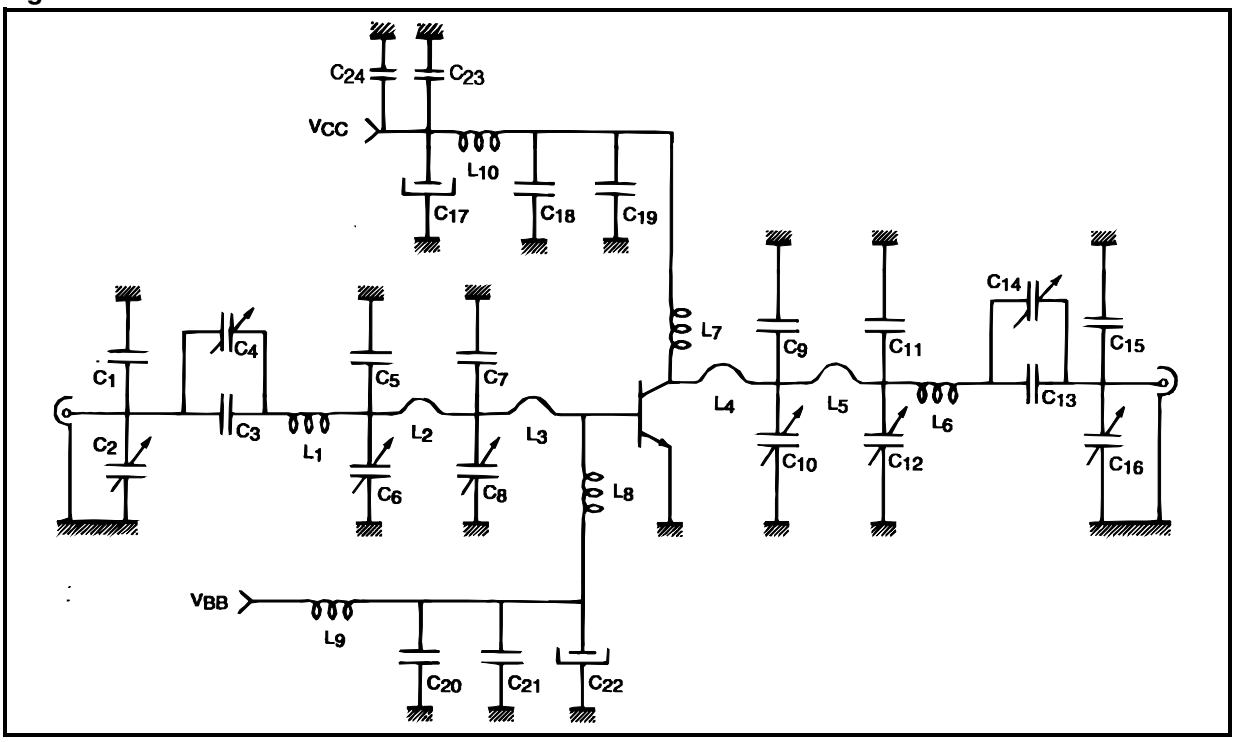
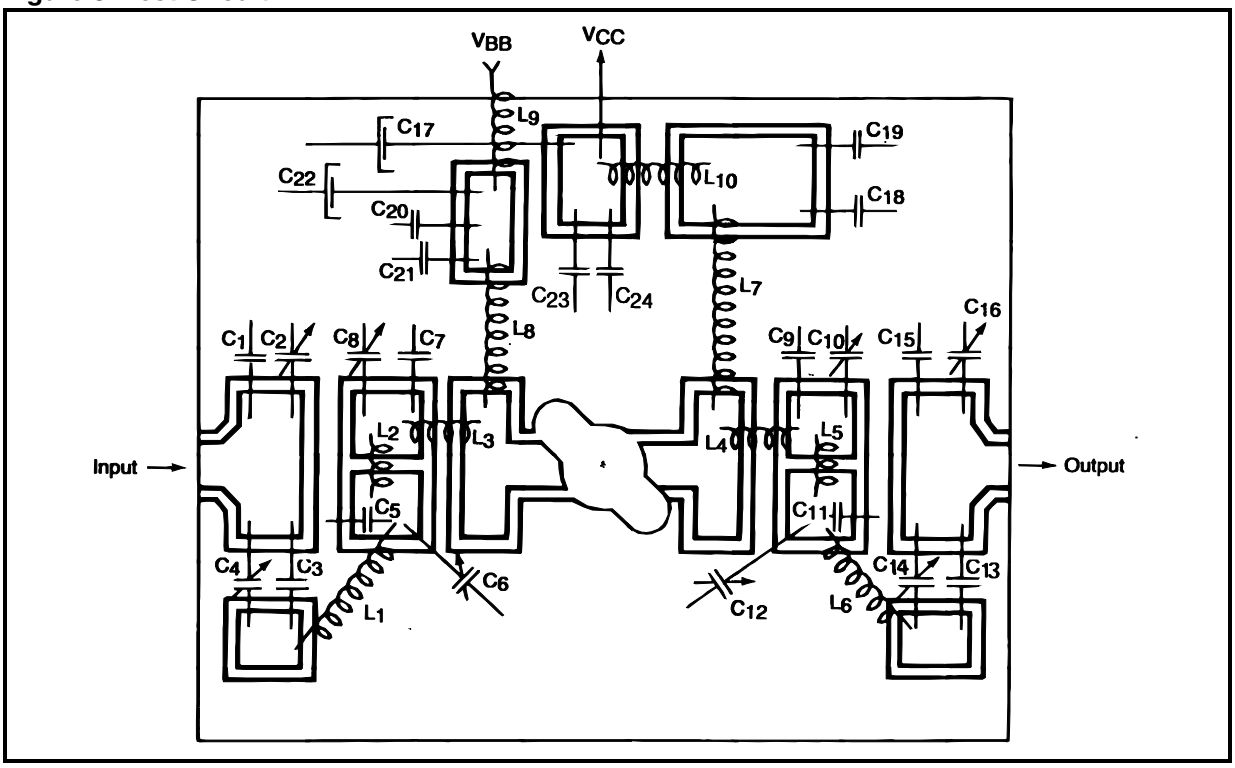


Table 7. Test Circuit

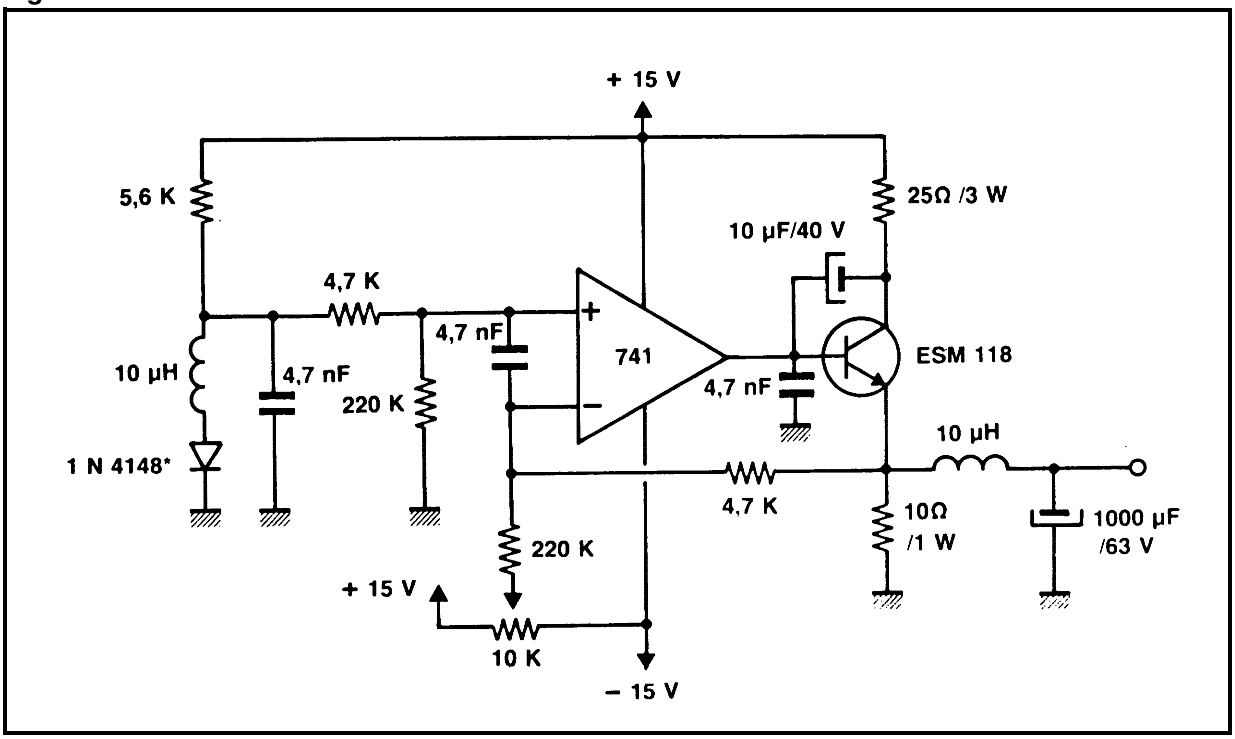
C1	180pF
C2, C4, C6, C8, C10, C12, C14, C16	Arco 428
C3	820pF
C5, C13	680pF
C7, C11	1.2nF
C9	1.5nF
C17, C22	470µF, 40V
C18	10nF
C19, C21, C23	1nF
C20, C24	100nF, 63V
L1	3 Turns, Diameter 10mm, 1.3mm Wire, Length 10mm
L2, L5	Hair Pin Copper foil 40 x 5mm, 0.2mm Thick
L3, L4	Hair Pin Copper Foil 10 x 5mm, 0.2mm Thick
L6	5 Turns, Diameter 10mm, 1.3mm Wire, Length 15mm
L7	3 Turns, Diameter 10mm, 1.3mm Wire, Length 25mm
L8	Choke
L9	Choke
L10	Choke

Figure 8. Test Circuit



BIAS CIRCUIT

Figure 9. Bias Circuit

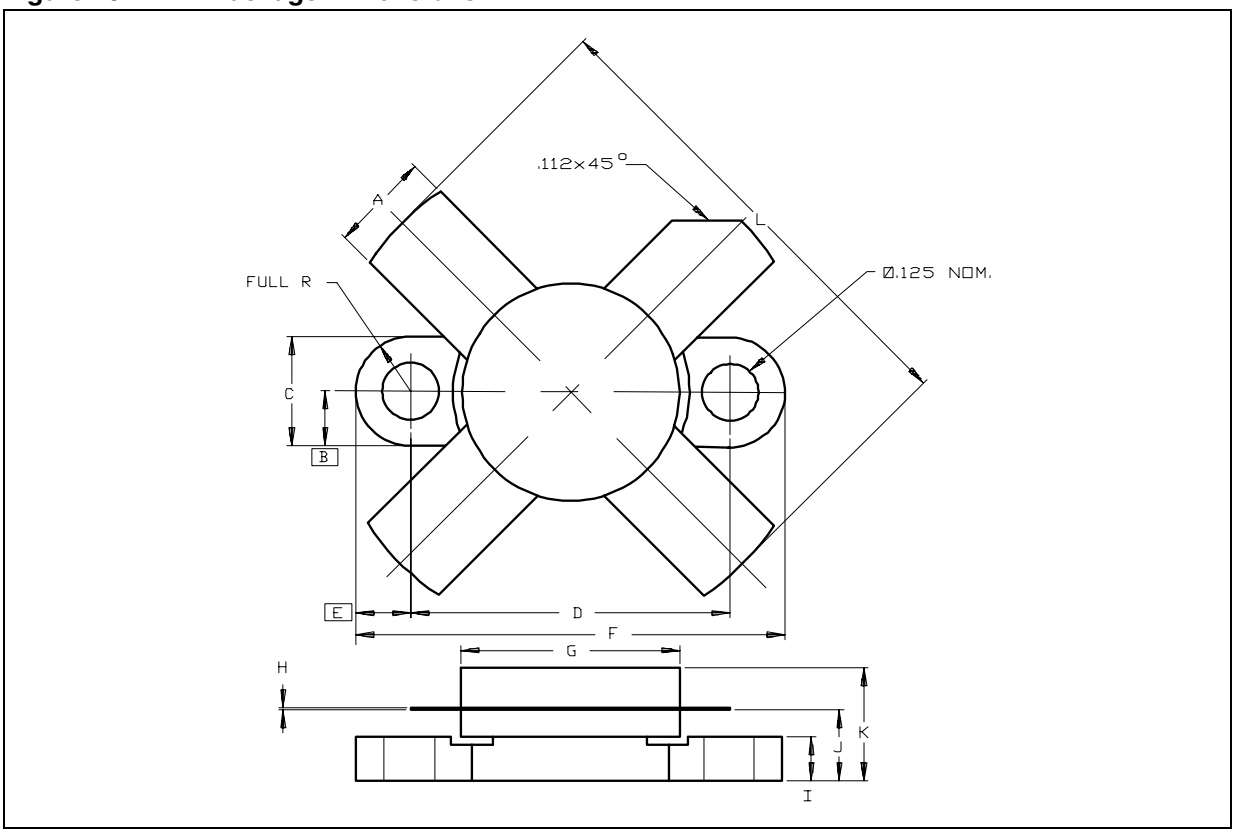


PACKAGE MECHANICAL

Table 8. M174 Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	5.59		5.84	0.220		0.230
B		3.18			0.125	
C	6.22		6.48	0.245		0.255
D	18.28		18.54	0.720		0.730
E		3.18			0.125	
F	24.64		24.89	0.970		0.980
G	12.57		12.83	0.495		0.505
H	0.08		0.18	0.003		0.007
I	2.29		2.79	0.090		0.110
J	4.06		4.45	0.160		0.175
K			7.11			0.280
L			26.67			1.050

Figure 10. M174 Package Dimensions



Note: Drawing is not to scale.

REVISION HISTORY

Table 9. Revision History

Date	Revision	Description of Changes
September-1994	1	First Issue
3-June-2004	2	Stylesheet update. No content change.