

# AmZ8133 • AmZ8173

## Octal Latches with Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

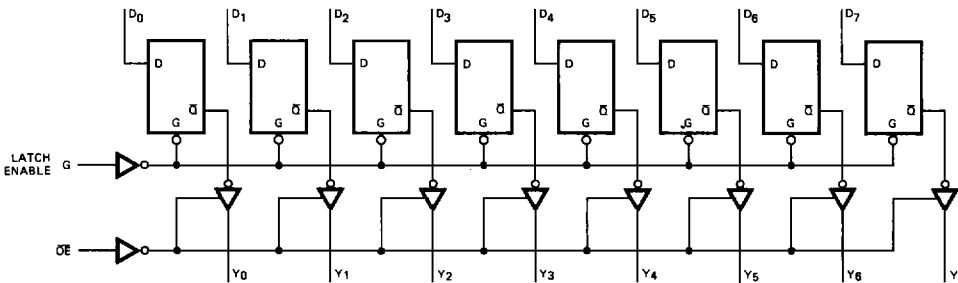
- 18ns max data in to data out
- Non-inverting AmZ8173, inverting AmZ8133
- Three-state outputs interface directly with bus organized systems
- Hysteresis on latch enable input for improved noise margin
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The AmZ8133 and AmZ8173 are octal latches with three-state outputs for bus organized system applications. The latches appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, OE, is LOW. When OE is HIGH the bus output is in the high-impedance state.

The AmZ8173 has non-inverted data inputs while the AmZ8133 is inverting.

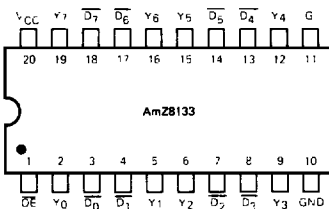
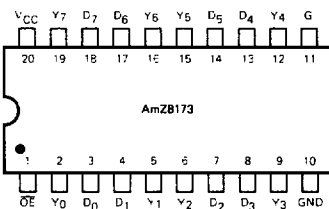
### LOGIC DIAGRAM AmZ8173



Inputs D<sub>0</sub> through D<sub>7</sub> are inverted on the AmZ8133.

BLI-041

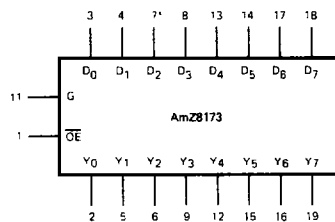
### CONNECTION DIAGRAMS Top Views



Note: Pin 1 is marked for orientation.

BLI-042

### LOGIC SYMBOL



V<sub>CC</sub> = Pin 20  
GND = Pin 10

Inputs D<sub>0</sub> through D<sub>7</sub> are inverted on the AmZ8133.

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### ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 5\%$  MIN. = 4.75V MAX. = 5.25V

MIL  $T_A = -55^\circ\text{C to } +125^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 10\%$  MIN. = 4.50V MAX. = 5.50V

### DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -1.0\text{mA}$	MIL	2.4	3.4	Volts
			$I_{OH} = -2.6\text{mA}$	COM'L	2.4	3.4	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{MIN.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12\text{mA}$			0.4	Volts
			$I_{OL} = 24\text{mA}$			0.5	
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL		0.7	Volts
				COM'L		0.8	
$V_i$	Input Clamp Voltage	$V_{CC} = \text{MIN.}, I_{IN} = -18\text{mA}$				-1.5	Volts
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX.}, V_{IN} = 0.4\text{V}$				-0.4	mA
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 2.7\text{V}$				20	$\mu\text{A}$
$I_I$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 7.0\text{V}$				0.1	mA
$I_{OZ}$	Off-State (High-Impedance) Output Current	$V_{CC} = \text{MAX.}$		$V_O = 0.4\text{V}$		-20	$\mu\text{A}$
				$V_O = 2.4\text{V}$		20	
$I_{SC}$	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$		-30		-85	mA
$I_{CC}$	Power Supply Current (Note 4)	$V_{CC} = \text{MAX.}$			24	40	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. Inputs grounded; outputs open.

### MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	-0.5V to $V_{CC}$ max.
DC Input Voltage	-0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

AmZ8133

SWITCHING CHARACTERISTICS

( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ )

Parameters	Description	Min	Typ	Max	Units	Test Conditions
$t_{PLH}$	Enable to Output		20	30	ns	$C_L = 45\text{pF}$ $R_L = 667\Omega$
$t_{PHL}$			18	30		
$t_{PLH}$	Data Input to Output		13	20	ns	
$t_{PHL}$			15	23		
$t_s(H)$	HIGH Data to Enable	3			ns	
$t_s(L)$	LOW Data to Enable	0			ns	
$t_h(H)$	HIGH Data to Enable	13			ns	
$t_h(L)$	LOW Data to Enable	7			ns	
$t_{pw}$	Enable Pulse Width	15			ns	
$t_{ZH}$	$\overline{OE}$ to $Y_i$			28	ns	
$t_{ZL}$				36		
$t_{HZ}$	$\overline{OE}$ to $Y_i$			20	ns	$C_L = 5\text{pF}$ $R_L = 667\Omega$
$t_{LZ}$				25		

AmZ8133

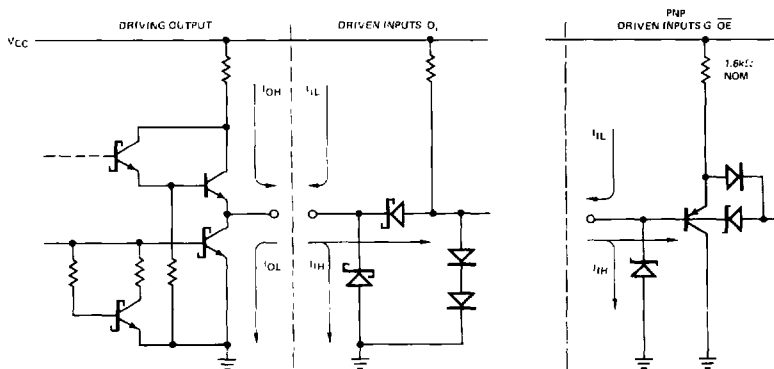
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	COM'L		MIL		Units	Test Conditions
		Min.	Max.	Min.	Max.		
		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			
$t_{PLH}$	Enable to Output		35		40	ns	$C_L = 45\text{pF}$ $R_L = 667\Omega$
$t_{PHL}$			35		40		
$t_{PLH}$	Data Input to Output		20		21	ns	
$t_{PHL}$			25		30		
$t_s(H)$	HIGH Data to Enable	5		5	ns		
$t_s(L)$	LOW Data to Enable	0		0	ns		
$t_h(H)$	HIGH Data to Enable	14		15	ns		
$t_h(L)$	LOW Data to Enable	9		10	ns		
$t_{pw}$	Enable Pulse Width	17		20	ns		
$t_{ZH}$	$\overline{OE}$ to $Y_i$		28		28	ns	
$t_{ZL}$			36		36		
$t_{HZ}$	$\overline{OE}$ to $Y_i$		33		36	ns	$C_L = 5\text{pF}$ $R_L = 667\Omega$
$t_{LZ}$			33		36		

\*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

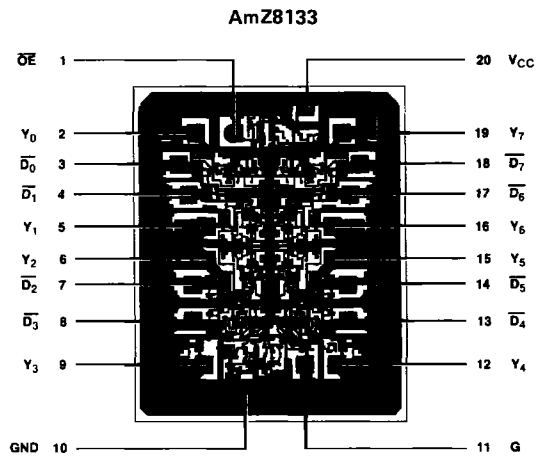
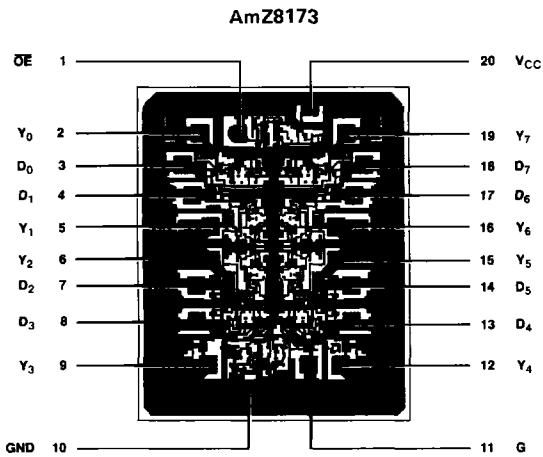


Note: Actual current flow direction shown.

BLI-044



## Metallization and Pad Layouts



DIE SIZE 0.073" X 0.089"

## FUNCTION TABLES

AmZ8173

Inputs			Internal	Outputs	Function
OE	G	D <sub>i</sub>	Q <sub>i</sub>	Y <sub>i</sub>	
H	X	X	X	Z	Hi-Z
L	H	L	H	L	Transparent
L	H	H	L	H	
L	L	X	NC	NC	Latched

AmZ8133

Inputs			Internal	Outputs	Function
OE	G	D <sub>i</sub>	Q <sub>i</sub>	Y <sub>i</sub>	
H	X	X	X	Z	Hi-Z
L	H	L	H	H	Transparent
L	H	H	L	L	
L	L	X	NC	NC	Latched

H = HIGH  
L = LOW  
X = Don't Care

NC = No Change  
Z = High Impedance

## DEFINITION OF FUNCTIONAL TERMS

AmZ8173

- D<sub>i</sub>** The latch data inputs.
- G** The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.
- Y<sub>i</sub>** The three-state latch outputs.
- OE** The output enable control. When OE is LOW, the outputs Y<sub>i</sub> are enabled. When OE is HIGH, the outputs Y<sub>i</sub> are in the high-impedance (off) state.

AmZ8133

- D<sub>i</sub>** The latch inverting data inputs.
- G** The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.
- Y<sub>i</sub>** The three-state latch outputs.
- OE** The output enable control. When OE is LOW, the inverted outputs Y<sub>i</sub> are enabled. When OE is HIGH, the outputs Y<sub>i</sub> are in the high-impedance (off) state.