Document Title

512Kx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

Revision No.	History	Draft Data	Remark
0.0	Initial Draft	December 3, 1998	Preliminary
1.0	Finalize	April 28, 1999	Final

512K×8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 512K×8
- Power Supply Voltage
  KM68V4100C Family: 3.0~3.6V
  KM68U4100C Family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 48(36)-uBGA-6.10x8.90

GENERAL DESCRIPTION

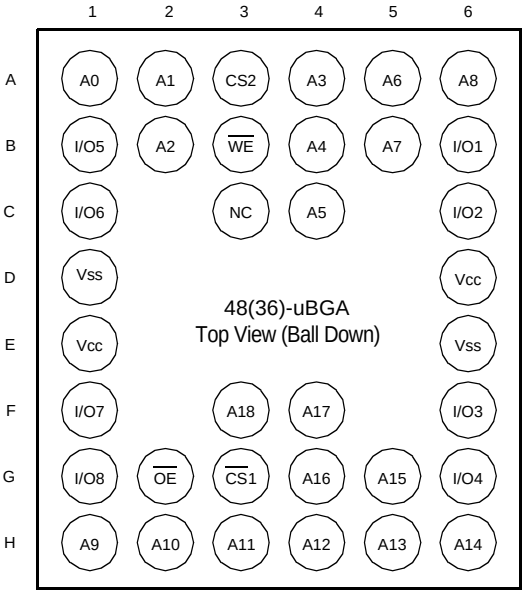
The KM68V4100C and KM68U4100C families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support industrial operating temperature range and have chip scale package type for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
KM68V4100CLI-L	Industrial(-40~85°C)	3.0~3.6V	70[1]/85ns	20µA	30mA	48(36)-uBGA
KM68U4100CLI-L		2.7~3.3V	70[1]/85/100ns			

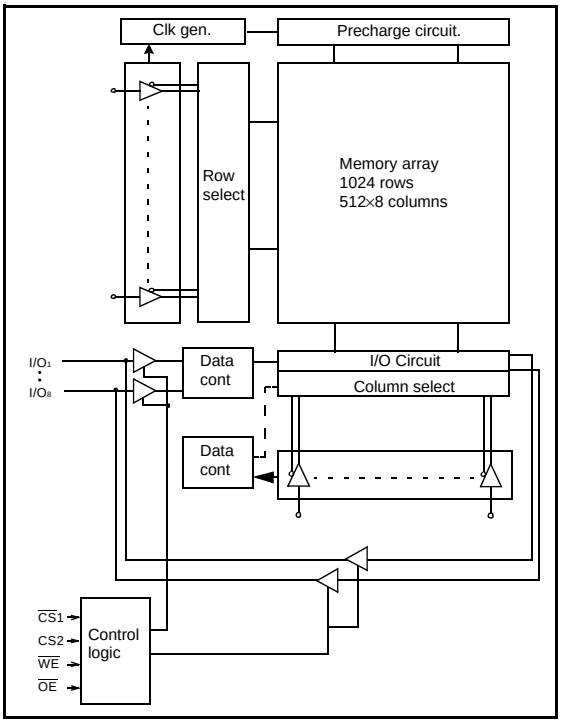
1. The paramerter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$1, CS2	Chip Select Inputs	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{WE}$	Write Enable Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
A_0~A_{18}	Address Inputs	NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Industrial Temp Products(-40~85°C)	
Part Name	**Function**
KM68V4100CLZI-7L	48-uBGA, 70ns, 3.3V, LL
KM68V4100CLZI-8L	48-uBGA, 85ns, 3.3V, LL
KM68U4100CLZI-7L	48-uBGA, 70ns, 3.0V, LL
KM68U4100CLZI-8L	48-uBGA, 85ns, 3.0V, LL
KM68U4100CLZI-10L	48-uBGA, 100ns, 3.0V, LL

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1]	X[1]	X[1]	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X[1]	L	Din	Write	Active

1. X means don't care (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to V_{CC}+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	-40 to 85	°C	KM68V4100CLI, KM68U4100CLI

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	Vcc	KM68V4100C Family KM68U4100C Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	KM68V4100C, KM68U4100C Family	2.2	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	KM68V4100C, KM68U4100C Family	-0.3[3)]	-	0.6	V

Note:
1. Industrial Product: T_A=-40 to 85°C, otherwise specified
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤ 30ns
3. Undershoot: -2.0V in case of pulse width ≤ 30ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

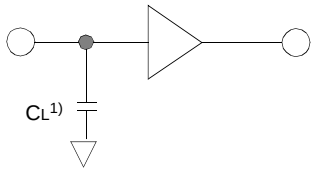
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{IO}=Vss to Vcc	-1	-	1	µA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, $\overline{WE}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}	-	-	4	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA $\overline{CS_1}$≤0.2V, CS_2≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥Vcc-0.2V	-	-	4	mA
	I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}	-	-	30	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA	2.2	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}, Other inputs = V_{IL} or V_{IH}	-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V or CS_2≤0.2V, Other inputs=0~Vcc	-	-	20	µA

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V
Input rising and falling time : 5ns
Input and output reference voltage :1.5V
Output load(see right) : C_L=100pF+1TTL
C_L[1)]=30pF+1TTL

1. 70ns products



1. Including scope and jig capacitance

AC CHARACTERISTICS (T_A=-40 to 85°C, KM68V4100C Family: 3.0~3.6V, KM68U4100C Family: 2.7~3.3V)

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	70	-	85	-	100	-	ns
	Address access time	t_{AA}	-	70	-	85	-	100	ns
	Chip select to output	t_{CO1}, t_{CO2}	-	70	-	85	-	100	ns
	Output enable to valid output	t_{OE}	-	35	-	40	-	50	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	25	0	25	0	30	ns
	Output disable to high-Z output	t_{OHZ}	0	25	0	25	0	30	ns
	Output hold from address change	t_{OH}	10	-	10	-	15	-	ns
Write	Write cycle time	t_{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t_{CW}	60	-	70	-	80	-	ns
	Address set-up time	t_{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t_{AW}	60	-	70	-	80	-	ns
	Write pulse width	t_{WP}	55	-	55	-	70	-	ns
	Write recovery time	t_{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	25	0	25	0	30	ns
	Data to write time overlap	t_{DW}	30	-	35	-	40	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	5	-	ns

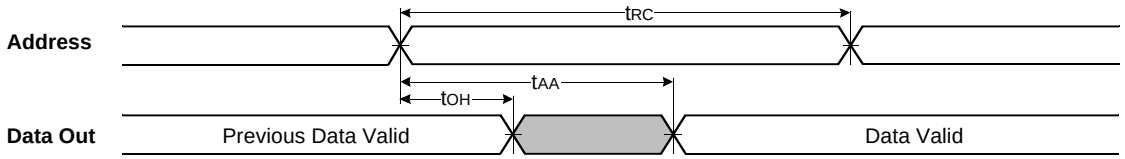
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS_1} \geq Vcc-0.2V$[1)]	2.0	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS_1} \geq Vcc-0.2V$[1)]	-	0.5	20	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}		5	-	-	

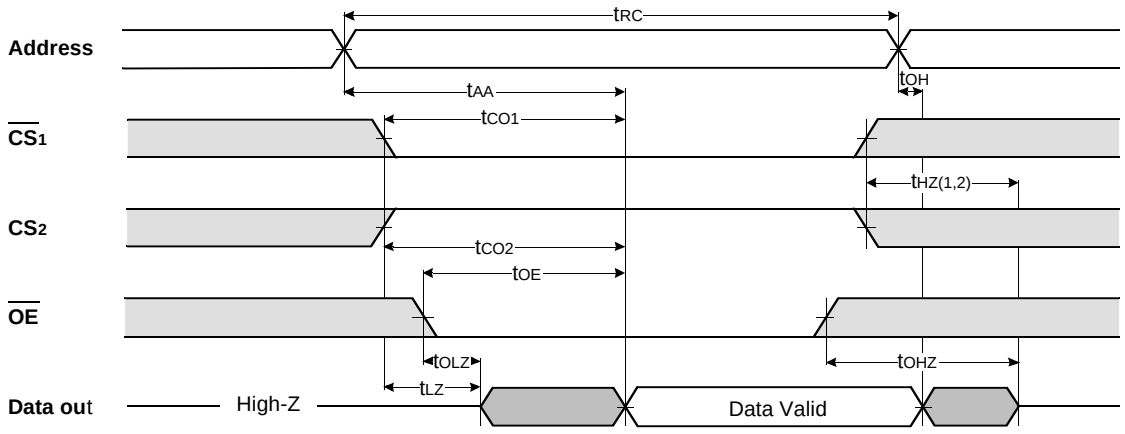
1. $\overline{CS_1} \geq Vcc-0.2V$, $CS_2 \geq Vcc-0.2V$(CS_1 controlled) or $CS_2 \leq 0.2V$(CS_2 controlled)

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH})



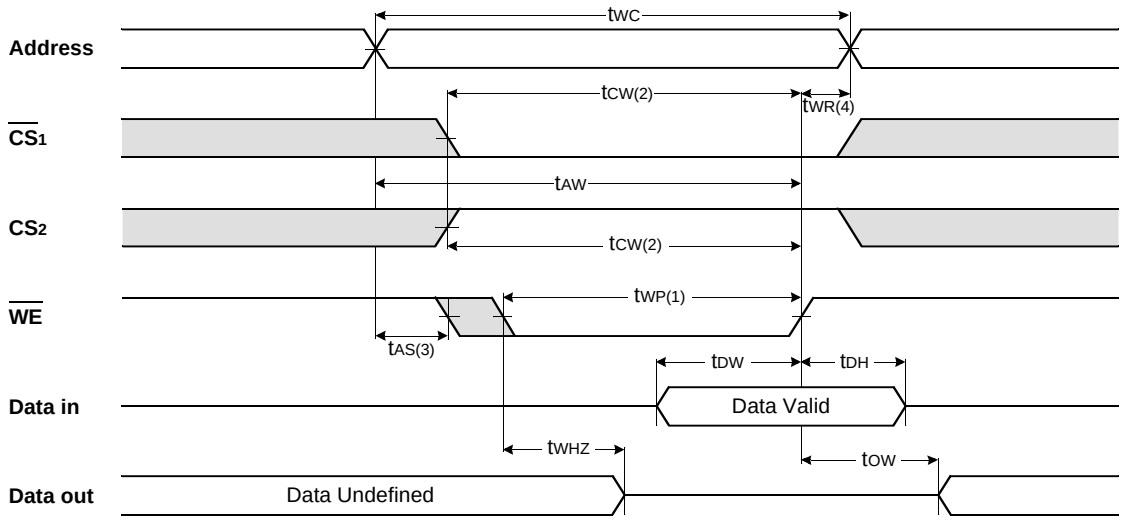
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



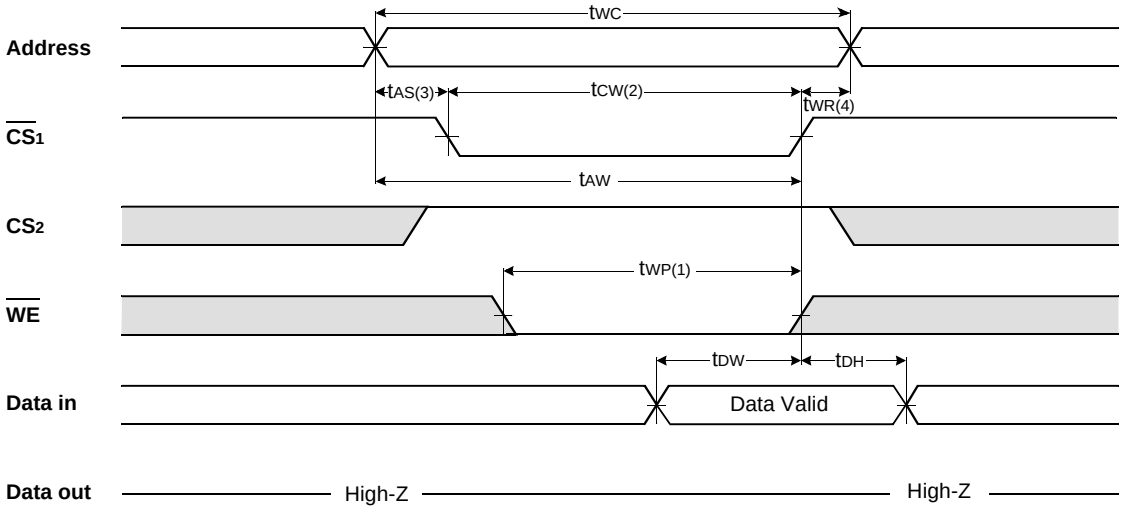
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

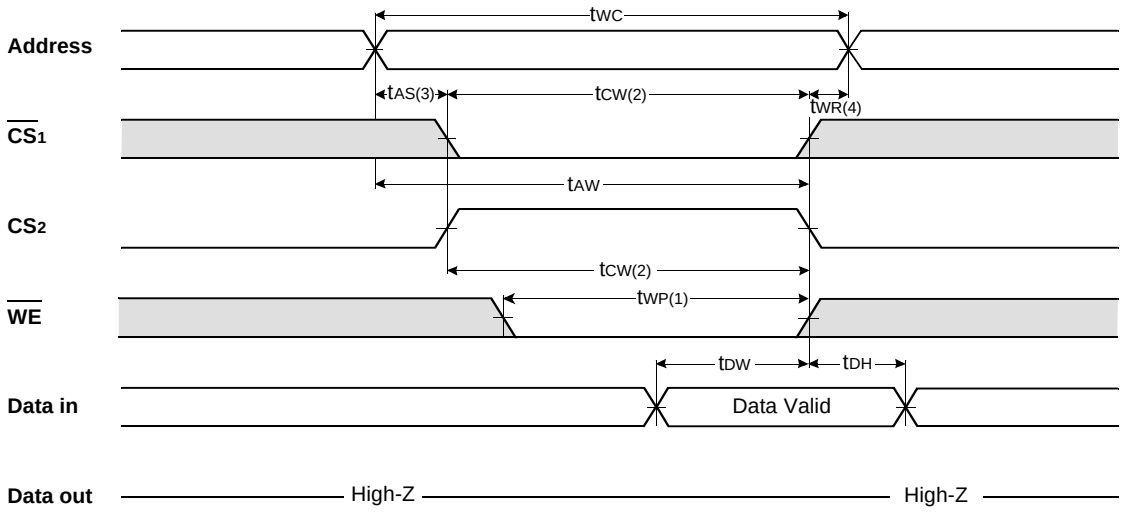
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS_2 Controlled)

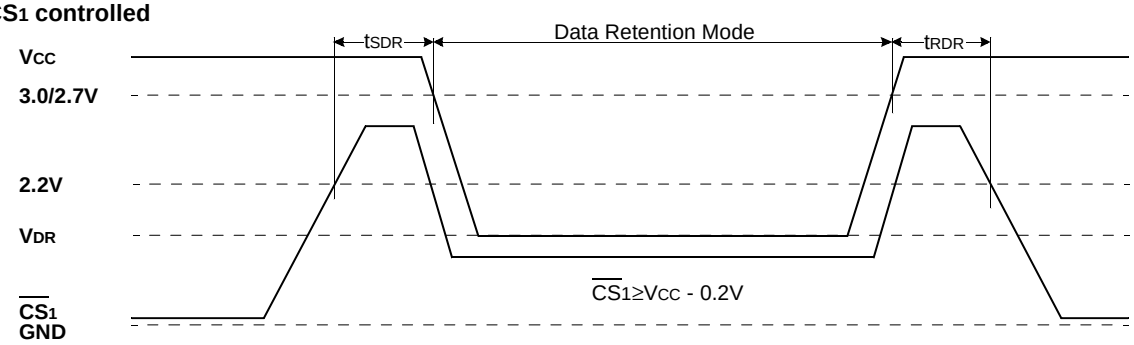


NOTES (WRITE CYCLE)

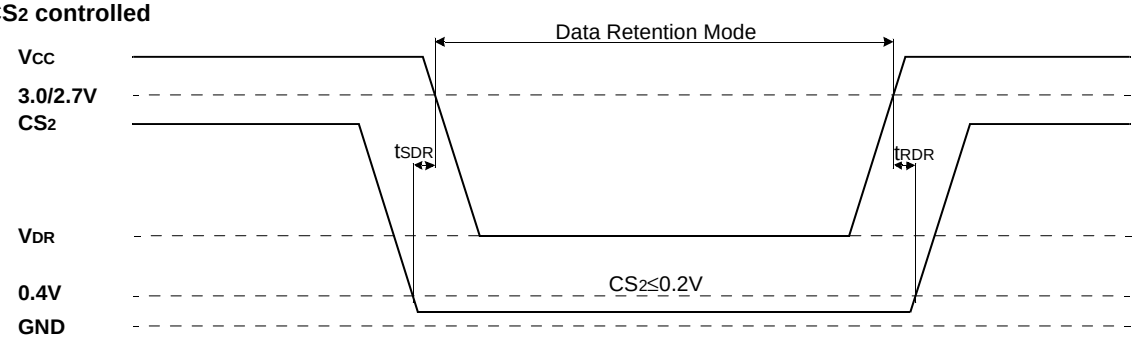
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among CS_1 going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high t_{WR2} applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled



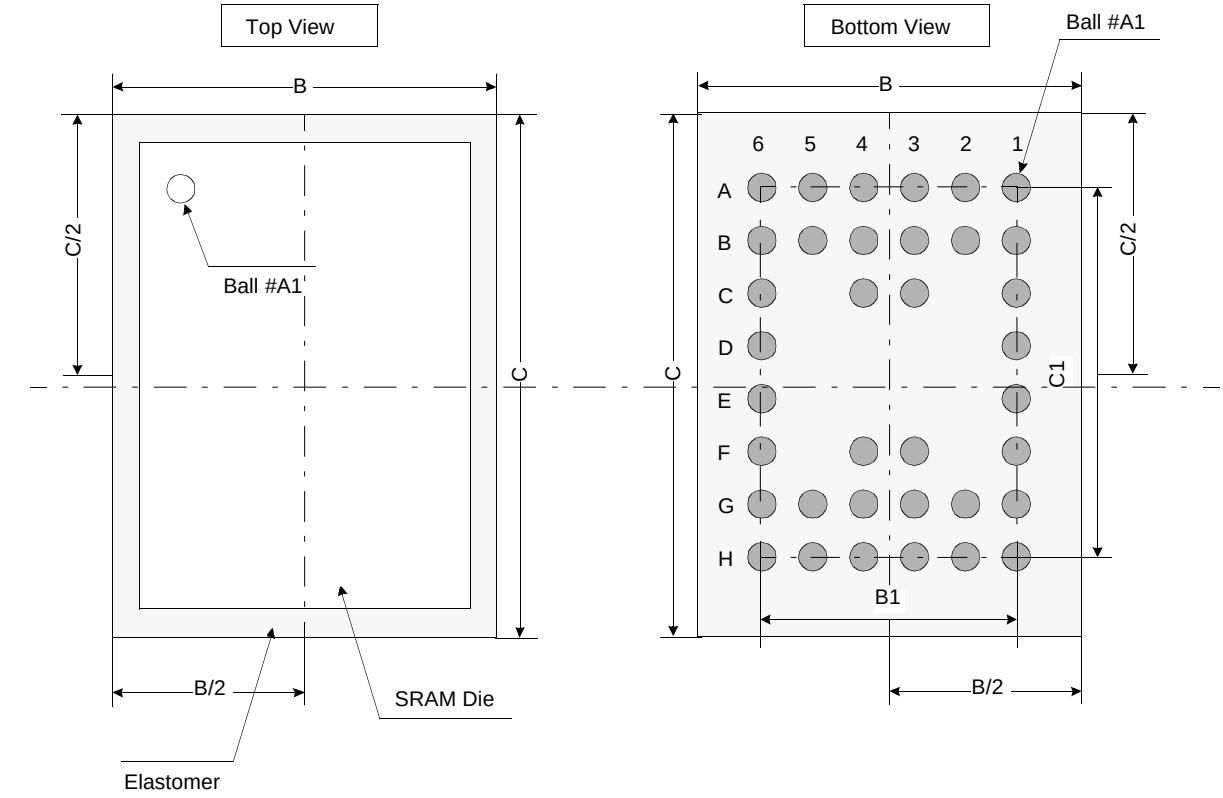
CS_2 controlled

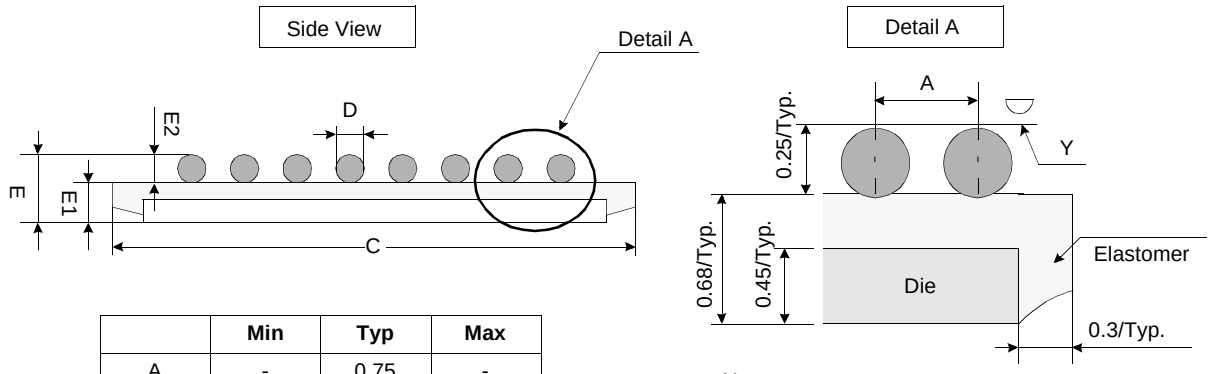


PACKAGE DIMENSIONS

Units: millimeters

48 BALL MICRO BALL GRID ARRAY- 0.75mm ball pitch





	Min	Typ	Max
A	-	0.75	-
B	6.00	6.10	6.20
B1	-	3.75	-
C	8.80	8.90	9.00
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.93	0.94
E1	-	0.68	-
E2	-	0.25	-
Y	-	-	0.08

Notes.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)