

Document Title**128Kx36-Bit Synchronous Pipelined Burst SRAM**Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	May . 15. 1997	Preliminary
0.1	Change 7.5 bin to 7.2	January . 13 . 1998	Preliminary
0.2	Change speed symbol 6.0/6.7/7.2/8.5 to 60/67/72/85	February. 02. 1998	Preliminary
0.3	Change DC characteristics V <sub>DD</sub> condition from V <sub>DD</sub> =3.3V+10%/-5% Change Input/output leakage currant for ±1μA to ±2μA Modify Read timing & Power down cycle timing. Change I <sub>SB2</sub> value from 30mA to 20mA. Remove DC characteristics I <sub>SB1</sub> - L ver.& I <sub>SB2</sub> - L ver .	February. 12. 1998	Preliminary
0.4	Remove Low power version. Add 119BGA(7x17 Ball Grid Array Package)	March. 11 . 1998	Preliminary
0.5	Change Undershoot spec from -3.0V(pulse width≤20ns) to -2.0V(pulse width≤tcyc/2) Add Overshoot spec 4.6V((pulse width≤tcyc/2) Change V <sub>IH</sub> max from 5.5V to V <sub>DD</sub> +0.5V	April. 14. 1998	Preliminary
0.6	Change I <sub>SB2</sub> value from 20mA to 30mA. Change V <sub>DD</sub> condition from V <sub>DD</sub> =3.3V+10%/-5% to V <sub>DD</sub> =3.3V+0.3V/-0.165V.	May.13. 1998	Preliminary
0.7	Modify DC characteristics( Input Leakage Current test Conditions) form V <sub>DD</sub> =V <sub>SS</sub> to V <sub>DD</sub> to Max.	May.14.1998	Preliminary
1.0	Final spec Release	May. 15. 1998	Final
2.0	Add V <sub>DDQ</sub> Supply voltage( 2.5V )	Dec. 02. 1998	Final
3.0	Remove 119BGA(7x17 Ball Grid Array Package) .	Nov. 26. 1999	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

128Kx36-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 3.3V + 0.3V / -0.165V$  Power Supply.
- $V_{DDQ}$  Supply Voltage  $3.3V + 0.3V / -0.165V$  for 3.3V I/O or  $2.5V + 0.4V / -0.125V$  for 2.5V I/O.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A Package .

FAST ACCESS TIMES

PARAMETER	Symbol	60	67	72	85	Unit
Cycle Time	t <sub>CYC</sub>	6.0	6.7	7.2	8.5	ns
Clock Access Time	t <sub>CD</sub>	3.5	3.8	4.0	4.0	ns
Output Enable Access Time	t <sub>OE</sub>	3.5	3.8	4.0	4.0	ns

GENERAL DESCRIPTION

The KM736V789 is a 4,718,592-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 128K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications;  $\overline{GW}$ ,  $\overline{BW}$ ,  $\overline{LBO}$ , ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by  $\overline{GW}$ , and each byte write is performed by the combination of  $\overline{WEx}$  and  $\overline{BW}$  when  $\overline{GW}$  is high. And with  $\overline{CS}_1$  high,  $\overline{ADSP}$  is blocked to control signals.

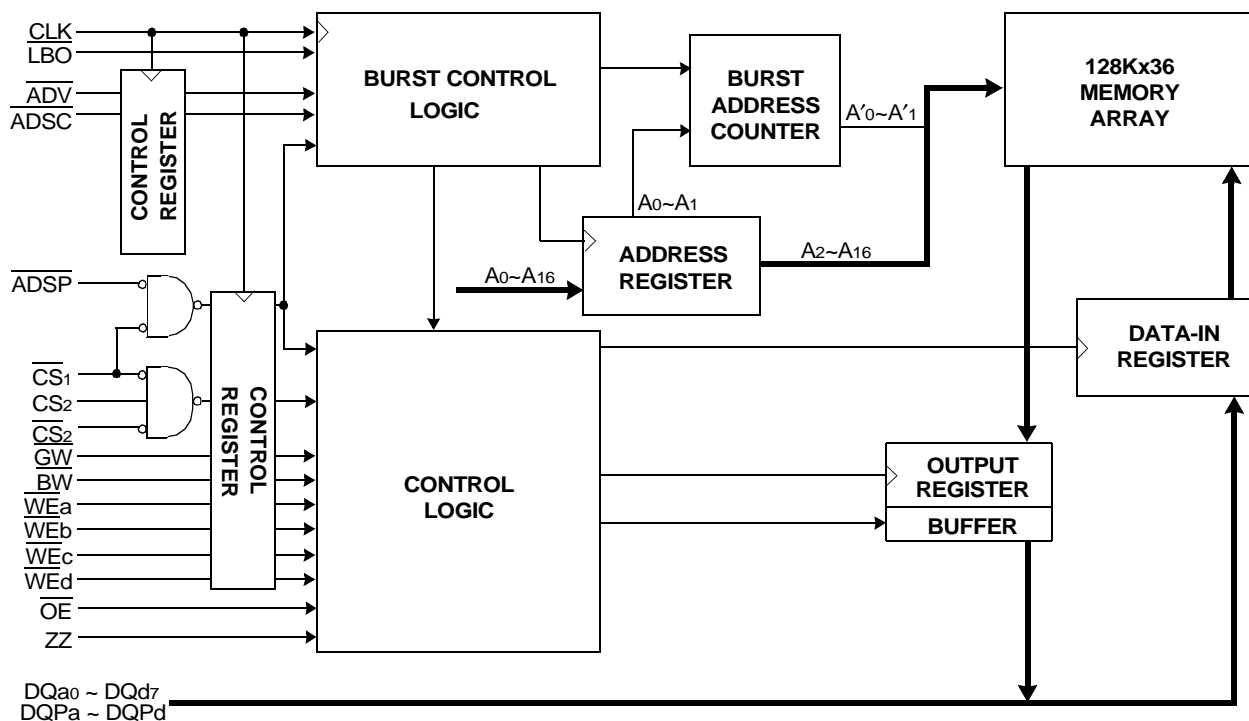
Burst cycle can be initiated with either the address status processor( $\overline{ADSP}$ ) or address status cache controller( $\overline{ADSC}$ ) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance( $\overline{ADV}$ ) input.

$\overline{LBO}$  pin is DC operated and determines burst sequence(linear or interleaved).

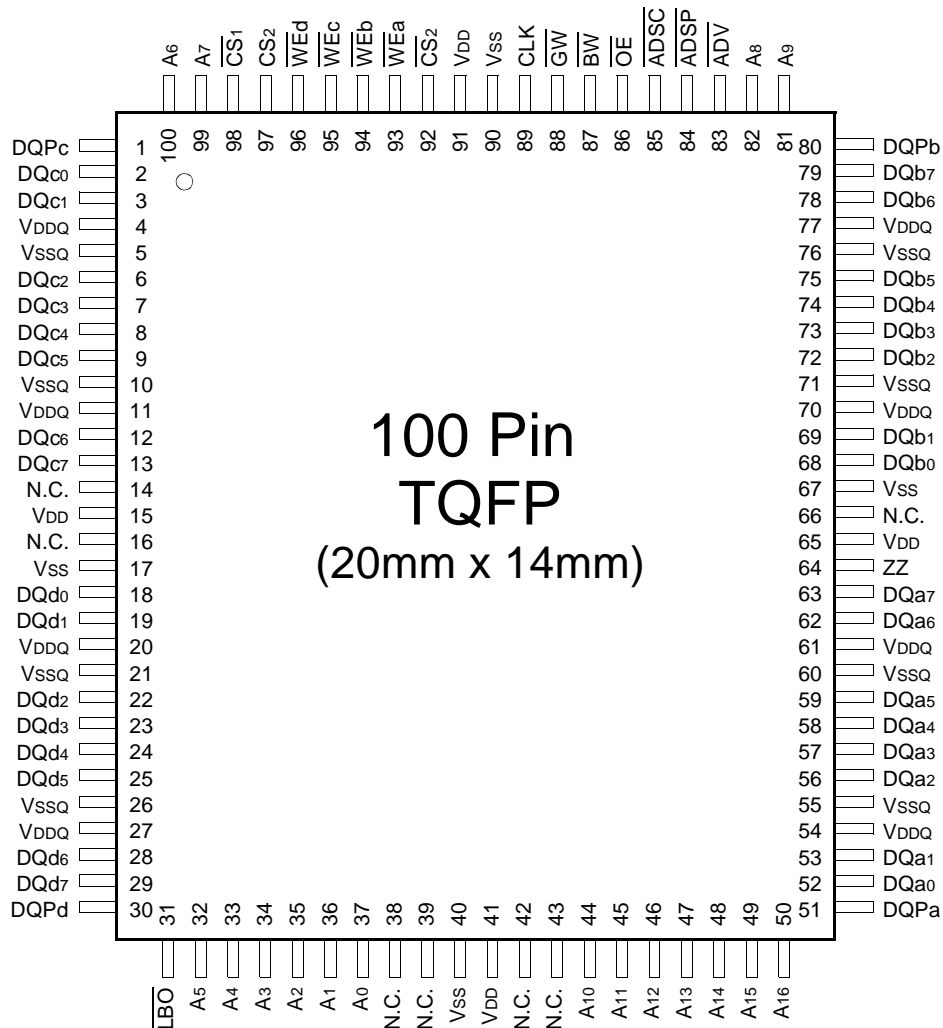
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM736V789 is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A16	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,66
ADV	Burst Address Advance	83	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSP	Address Status Processor	84	DQb0~b7		68,69,72,73,74,75,78,79
ADSC	Address Status Controller	85	DQc0~c7		2,3,6,7,8,9,12,13
CLK	Clock	89	DQd0~d7		18,19,22,23,24,25,28,29
CS1	Chip Select	98	DQPa~Pd		51,80,1,30
CS2	Chip Select	97	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
CS2	Chip Select	92	VSSQ	Output Ground	5,10,21,26,55,60,71,76
WE(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

**FUNCTION DESCRIPTION**

The KM736V789 is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of  $\overline{OE}$ , LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by  $\overline{ADSC}$ , ADSP and  $\overline{ADV}$  and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with  $\overline{ADV}$ .

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with  $\overline{ADSP}$ (regardless of  $\overline{WEx}$  and  $\overline{ADSC}$ )using the new external address clocked into the on-chip address register whenever  $\overline{ADSP}$  is sampled low, the chip selects are sampled active, and the output buffer is enabled with  $\overline{OE}$ . In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins.  $\overline{ADV}$  is ignored on the clock edge that samples  $\overline{ADSP}$  asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when  $\overline{WEx}$  are sampled High and  $\overline{ADV}$  is sampled low. And  $\overline{ADSP}$  is blocked to control signals by disabling  $\overline{CS1}$ .

All byte write is done by  $\overline{GW}$ (regardless of  $\overline{BW}$  and  $\overline{WEx}$ ), and each byte write is performed by the combination of  $\overline{BW}$  and  $\overline{WEx}$  when  $\overline{GW}$  is high.

Write cycles are performed by disabling the output buffers with  $\overline{OE}$  and asserting  $\overline{WEx}$ .  $\overline{WEx}$  are ignored on the clock edge that samples  $\overline{ADSP}$  low, but are sampled on the subsequent clock edges. The output buffers are disabled when  $\overline{WEx}$  are sampled Low(regardless of  $\overline{OE}$ ). Data is clocked into the data input register when  $\overline{WEx}$  sampled Low. The address increases internally to the next address of burst, if both  $\overline{WEx}$  and  $\overline{ADV}$  are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals( $\overline{WEa}$ ,  $\overline{WEb}$ ,  $\overline{WEc}$  or  $\overline{WEd}$ ) sampled low. The  $\overline{WEa}$  control DQa0 ~ DQa7 and DQPa,  $\overline{WEb}$  controls DQb0 ~ DQb7 and DQPb,  $\overline{WEc}$  controls DQc0 ~ DQc7 and DQPc, and  $\overline{WEd}$  control DQd0 ~ DQd7 and DQPd. Read or write cycle may also be initiated with  $\overline{ADSC}$ , instead of  $\overline{ADSP}$ . The differences between cycles initiated with  $\overline{ADSC}$  and  $\overline{ADSP}$  as are follows;

$\overline{ADSP}$  must be sampled high when  $\overline{ADSC}$  is sampled low to initiate a cycle with  $\overline{ADSC}$ .  
 $\overline{WEx}$  are sampled on the same clock edge that sampled  $\overline{ADSC}$  low(and  $\overline{ADSP}$  high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

**BURST SEQUENCE TABLE**

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1.  $\overline{LBO}$  pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS <sub>1</sub>	CS <sub>2</sub>	CS <sub>2</sub>	ADSP	ADSC	ADV	WRITE	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- Notes : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.  
 3. WRITE = L means Write operation in WRITE TRUTH TABLE.  
 WRITE = H means Read operation in WRITE TRUTH TABLE.  
 4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

- Notes : 1. X means "Don't Care".  
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

OPERATION	ZZ	OE	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

**PASS-THROUGH TRUTH TABLE**

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	WRITE	OPERATION	CS <sub>1</sub>	WRITE	OE	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

**Note** : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	VIN	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	VIO	-0.3 to VDDQ+0.5	V
Power Dissipation	Pd	1.6	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

\***Note** : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING CONDITIONS at 3.3V I/O (0°C ≤ TA ≤ 70°C)**

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.6	V
	VDDQ	3.135	3.3	3.6	V
Ground	Vss	0	0	0	V

**OPERATING CONDITIONS at 2.5V I/O (0°C ≤ TA ≤ 70°C)**

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.6	V
	VDDQ	2.375	2.5	2.9	V
Ground	Vss	0	0	0	V

**CAPACITANCE\* (TA=25°C, f=1MHz)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOUT=0V	-	7	pF

\***Notes** : Sampled not 100% tested.

**DC ELECTRICAL CHARACTERISTICS**( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$ )

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	IIL	$V_{DD} = \text{Max}$ ; $V_{IN}=V_{SS}$ to $V_{DD}$	-2	+2	$\mu\text{A}$	
Output Leakage Current	IOL	Output Disabled, $V_{OUT}=V_{SS}$ to $V_{DDQ}$	-2	+2	$\mu\text{A}$	
Operating Current	ICC	Device Selected, $I_{OUT}=0\text{mA}$ , $ZZ \leq V_{IL}$ , All Inputs= $V_{IL}$ or $V_{IH}$ Cycle Time $\geq t_{CYC}$ Min	-60	-	425	mA
			-67	-	400	
			-72	-	375	
			-85	-	350	
Standby Current	ISB	Device deselected, $I_{OUT}=0\text{mA}$ , $ZZ \leq V_{IL}$ , $f=\text{Max}$ , All Inputs $\leq 0.2\text{V}$ or $\geq V_{DD}-0.2\text{V}$	-60	-	130	mA
			-67	-	120	
			-72	-	110	
			-85	-	110	
	ISB1	Device deselected, $I_{OUT}=0\text{mA}$ , $ZZ \leq 0.2\text{V}$ , $f = 0$ , All Inputs=fixed ( $V_{DD}-0.2\text{V}$ or $0.2\text{V}$ )	-	-	30	mA
ISB2	Device deselected, $I_{OUT}=0\text{mA}$ , $ZZ \geq V_{DD}-0.2\text{V}$ , $f=\text{Max}$ , All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	-	30	mA	
Output Low Voltage(3.3V I/O)	VOL	$I_{OL} = 8.0\text{mA}$	-	0.4	V	
Output High Voltage(3.3V I/O)	VOH	$I_{OH} = -4.0\text{mA}$	2.4	-	V	
Output Low Voltage(2.5V I/O)	VOL	$I_{OL} = 1.0\text{mA}$	-	0.4	V	
Output High Voltage(2.5V I/O)	VOH	$I_{OH} = -1.0\text{mA}$	2.0	-	V	
Input Low Voltage(3.3V I/O)	VIL		-0.5*	0.8	V	
Input High Voltage(3.3V I/O)	VIH		2.0	$V_{DD}+0.5^{**}$	V	
Input Low Voltage(2.5V I/O)	VIL		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	VIH		1.7	$V_{DD}+0.5^{**}$	V	

\*  $V_{IL}(\text{Min})=-2.0(\text{Pulse Width} \leq t_{CYC}/2)$

\*\*  $V_{IH}(\text{Max})=4.6(\text{Pulse Width} \leq t_{CYC}/2)$

\*\* In Case of I/O Pins, the Max.  $V_{IH}=V_{DDQ}+0.5\text{V}$

**TEST CONDITIONS**

( $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$ ,  $V_{DDQ}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$  or  $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$ ,  $V_{DDQ}=2.5\text{V}+0.4\text{V}/-0.125\text{V}$ ,  $T_A=0$  to  $70^\circ\text{C}$ )

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	2ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	2ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	$V_{DDQ}/2$
Output Load	See Fig. 1

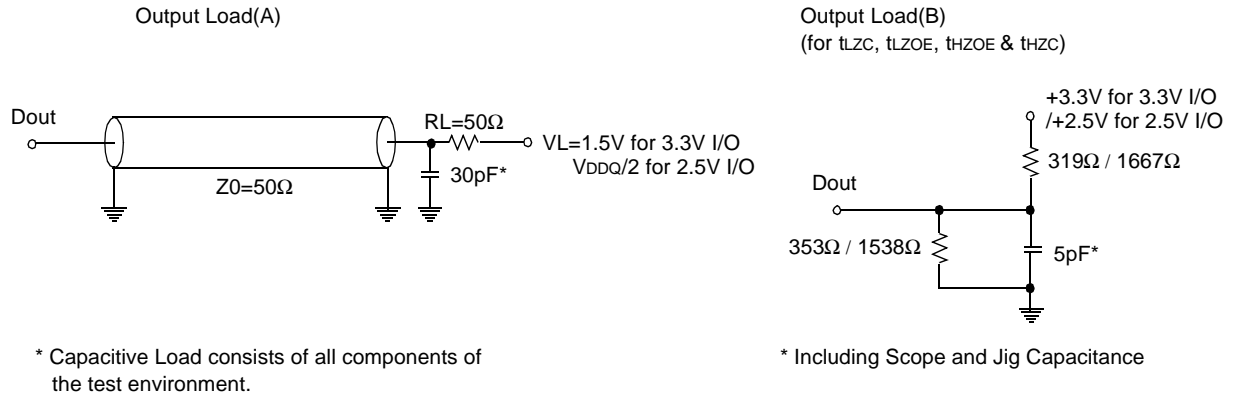


Fig. 1

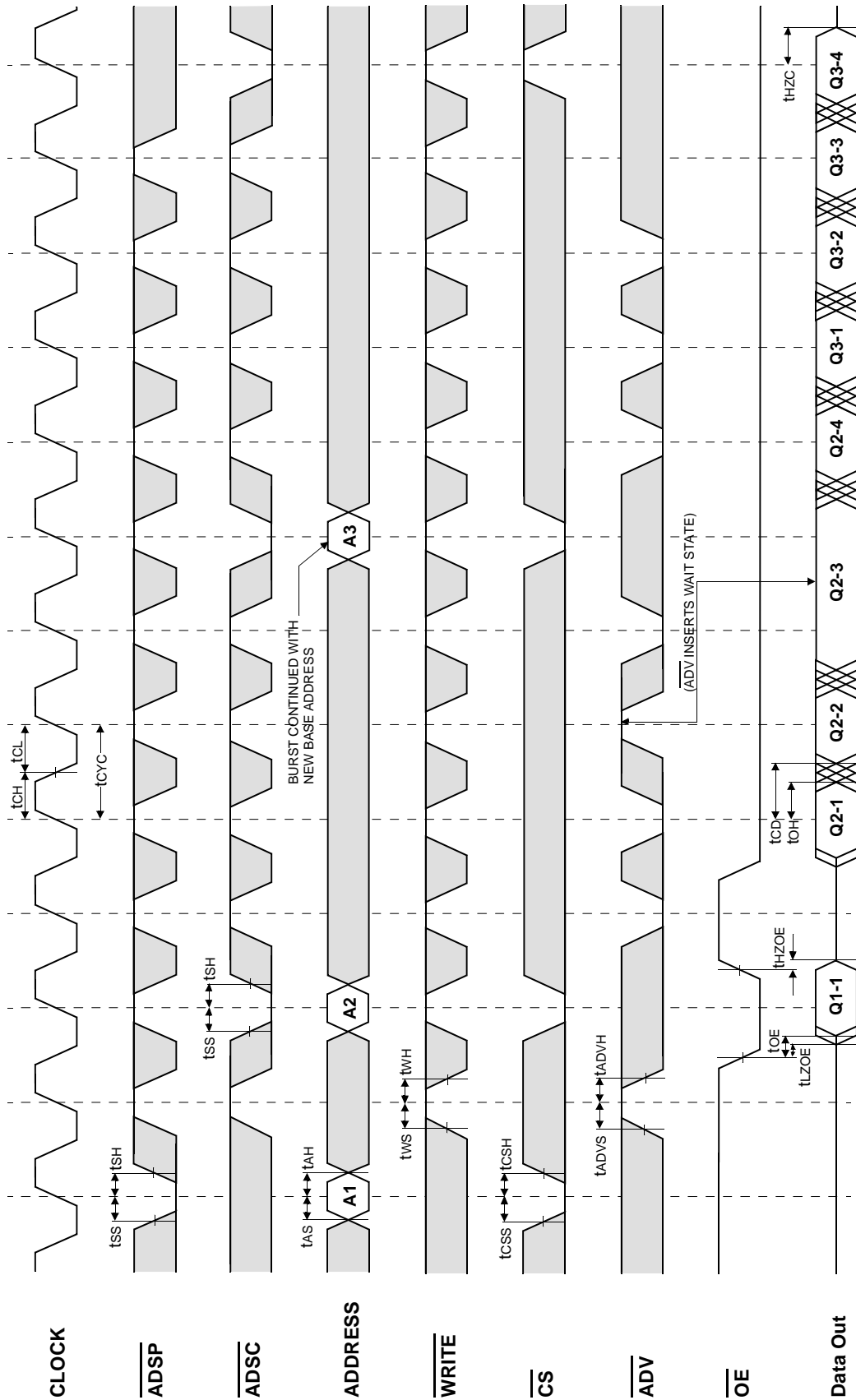
AC TIMING CHARACTERISTICS (TA=0 to 70°C, VDD=3.3V+0.3V/-0.165V)

PARAMETER	SYMBOL	-60		-67		-72		-85		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	tCYC	6.0	-	6.7	-	7.2	-	8.5	-	ns
Clock Access Time	tCD	-	3.5	-	3.8	-	4.0	-	4.0	ns
Output Enable to Data Valid	tOE	-	3.5	-	3.8	-	4.0	-	4.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.5	-	3.5	-	3.8	-	3.8	ns
Clock High to Output High-Z	tHZC	1.5	6.0	1.5	6.7	1.5	7.2	1.5	8.5	ns
Clock High Pulse Width	tCH	2.4	-	2.6	-	2.8	-	3.4	-	ns
Clock Low Pulse Width	tCL	2.4	-	2.6	-	2.8	-	3.4	-	ns
Address Setup to Clock High	tAS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Address Status Setup to Clock High	tSS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Data Setup to Clock High	tDS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Write Setup to Clock High ( $\overline{GW}$ , $\overline{BW}$ , $\overline{WEx}$ )	tWS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	tADVS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	tCSS	1.5	-	1.5	-	1.5	-	1.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ( $\overline{GW}$ , $\overline{BW}$ , $\overline{WEx}$ )	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycle

Note : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever  $\overline{ADSC}$  and/or  $\overline{ADSP}$  is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.  
 2. Both chip selects must be active whenever  $\overline{ADSC}$  or  $\overline{ADSP}$  is sampled low in order for the this device to remain enabled.  
 3.  $\overline{ADSC}$  or  $\overline{ADSP}$  must not be asserted for at least 2 Clock after leaving ZZ state.



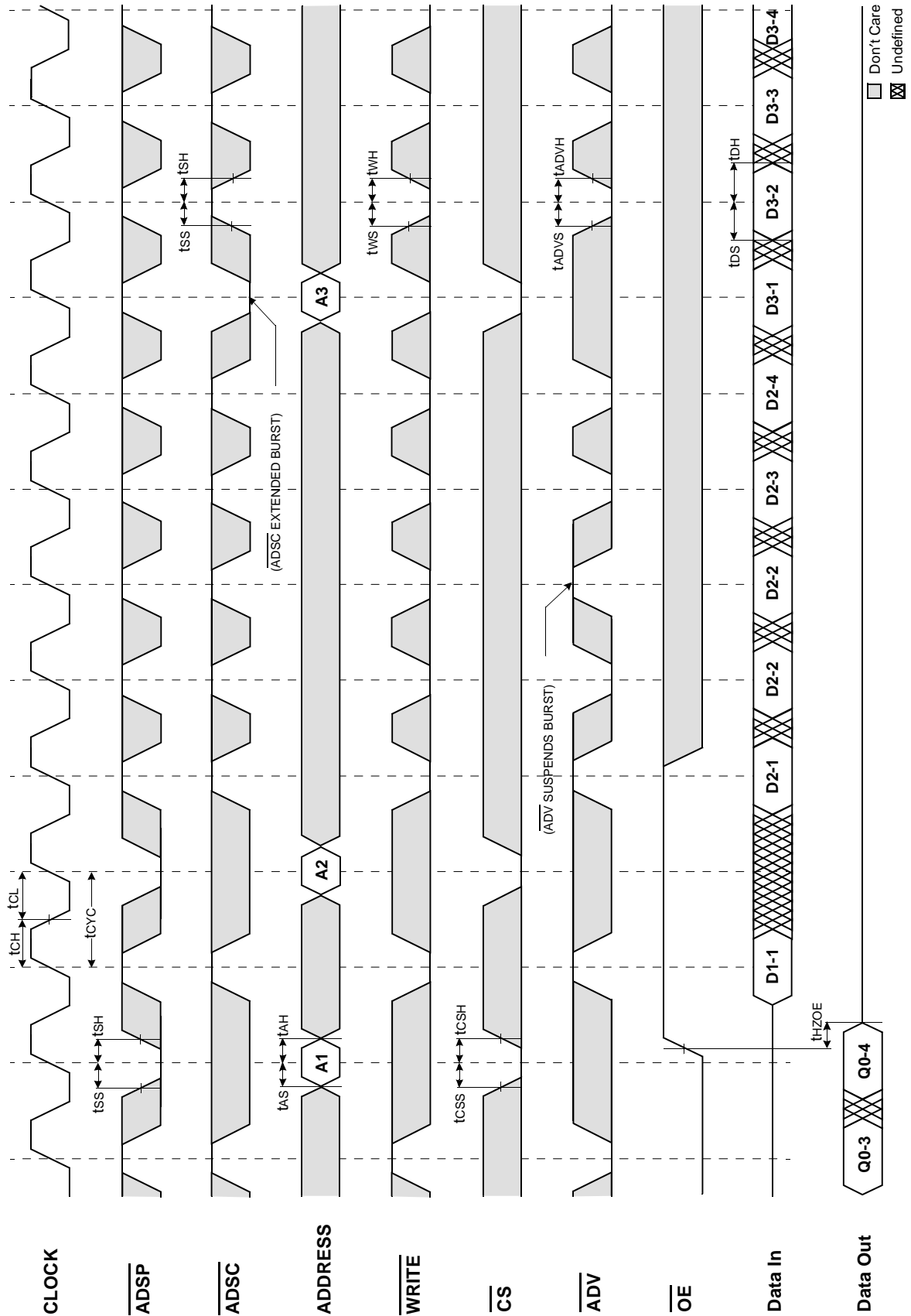
TIMING WAVEFORM OF READ CYCLE



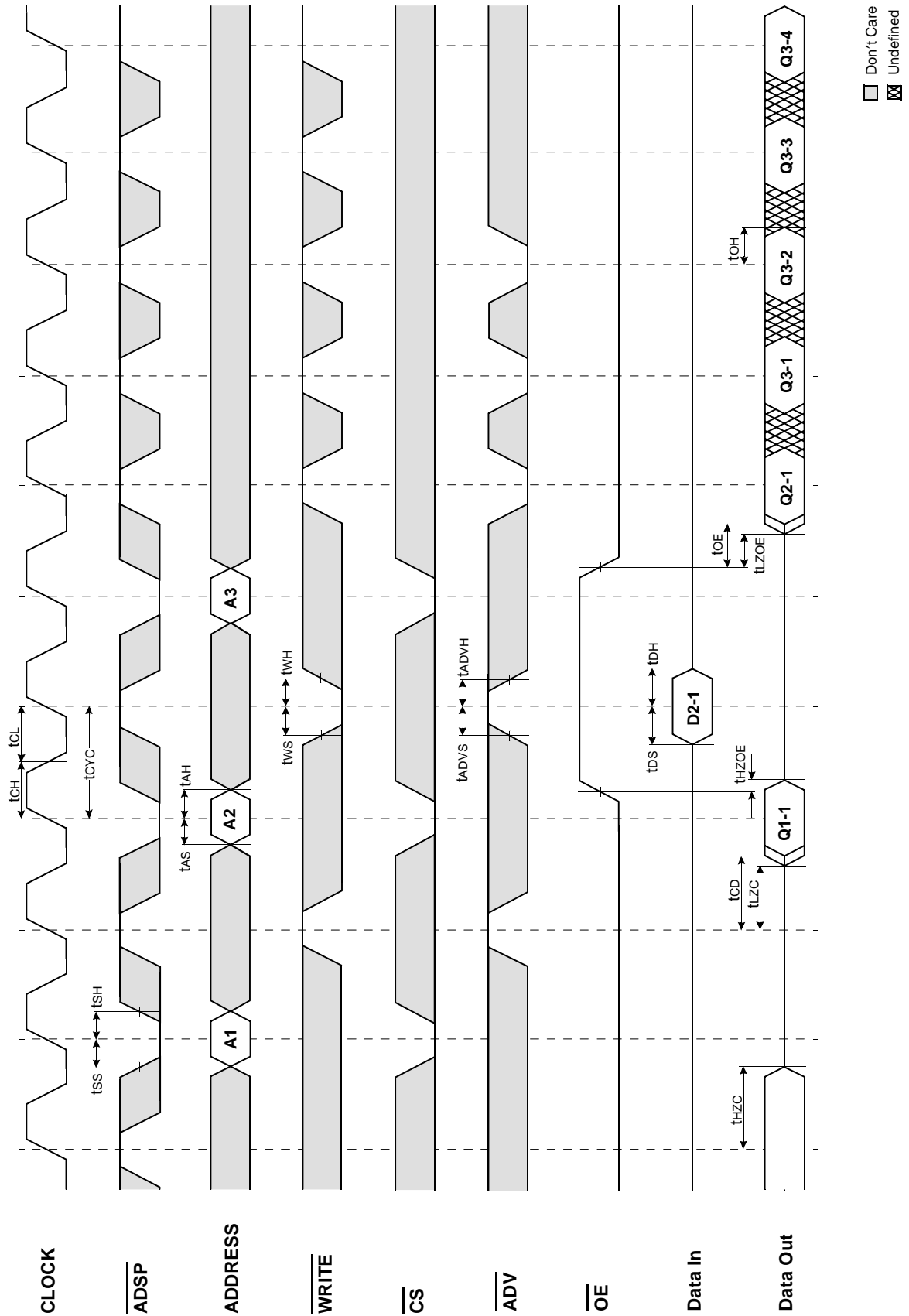
□ Don't Care  
 ⊠ Undefined

NOTES :  $\overline{WRITE} = L$  means  $\overline{GW} = L$ , or  $\overline{GW} = H, \overline{BW} = L, \overline{WE} = L$   
 $\overline{CS} = L$  means  $\overline{CS1} = L, \overline{CS2} = H$  and  $\overline{CS2} = L$   
 $\overline{CS} = H$  means  $\overline{CS1} = H$ , or  $\overline{CS1} = L$  and  $\overline{CS2} = H$ , or  $\overline{CS1} = L$ , and  $\overline{CS2} = L$

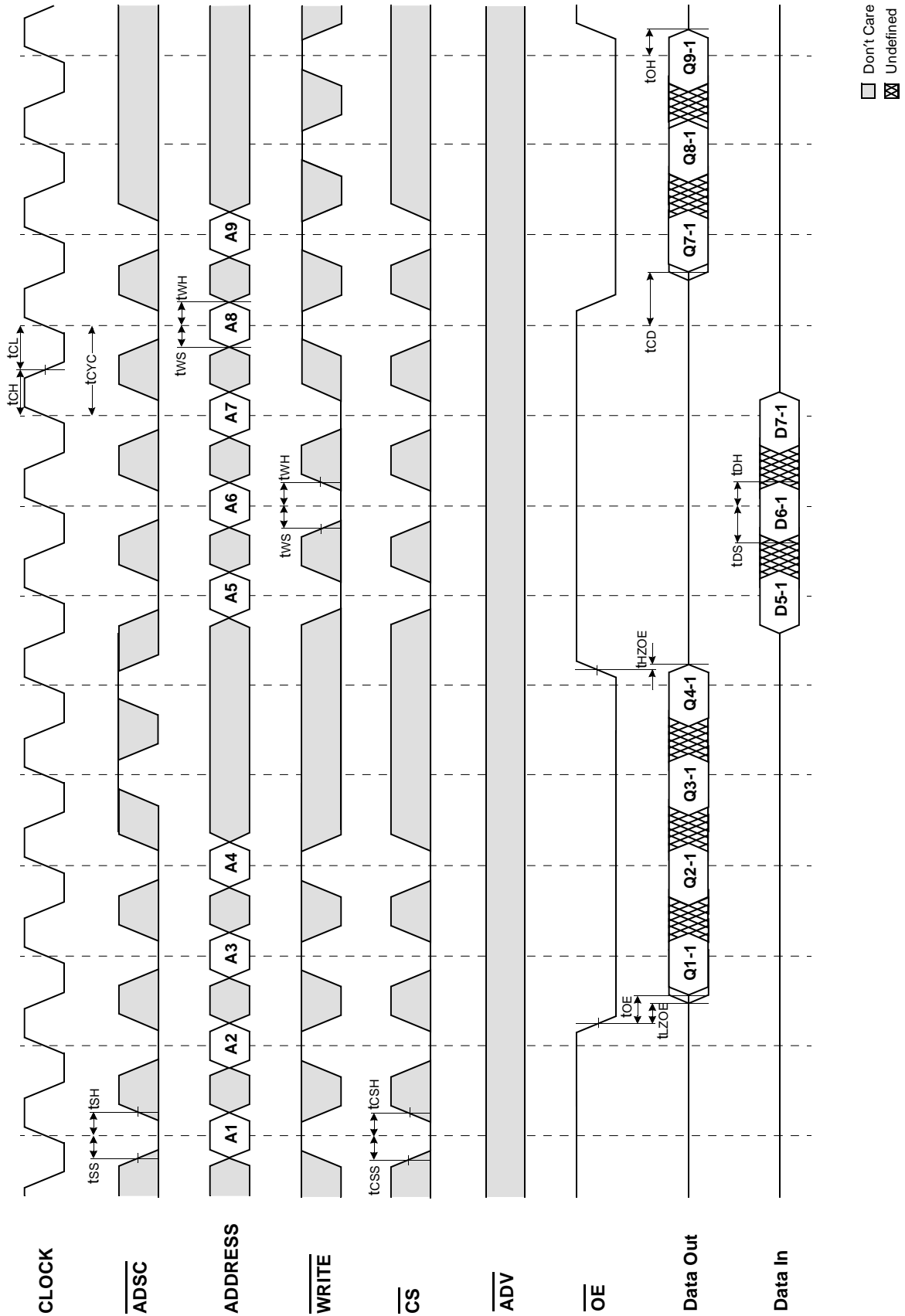
TIMING WAVEFORM OF WRTE CYCLE



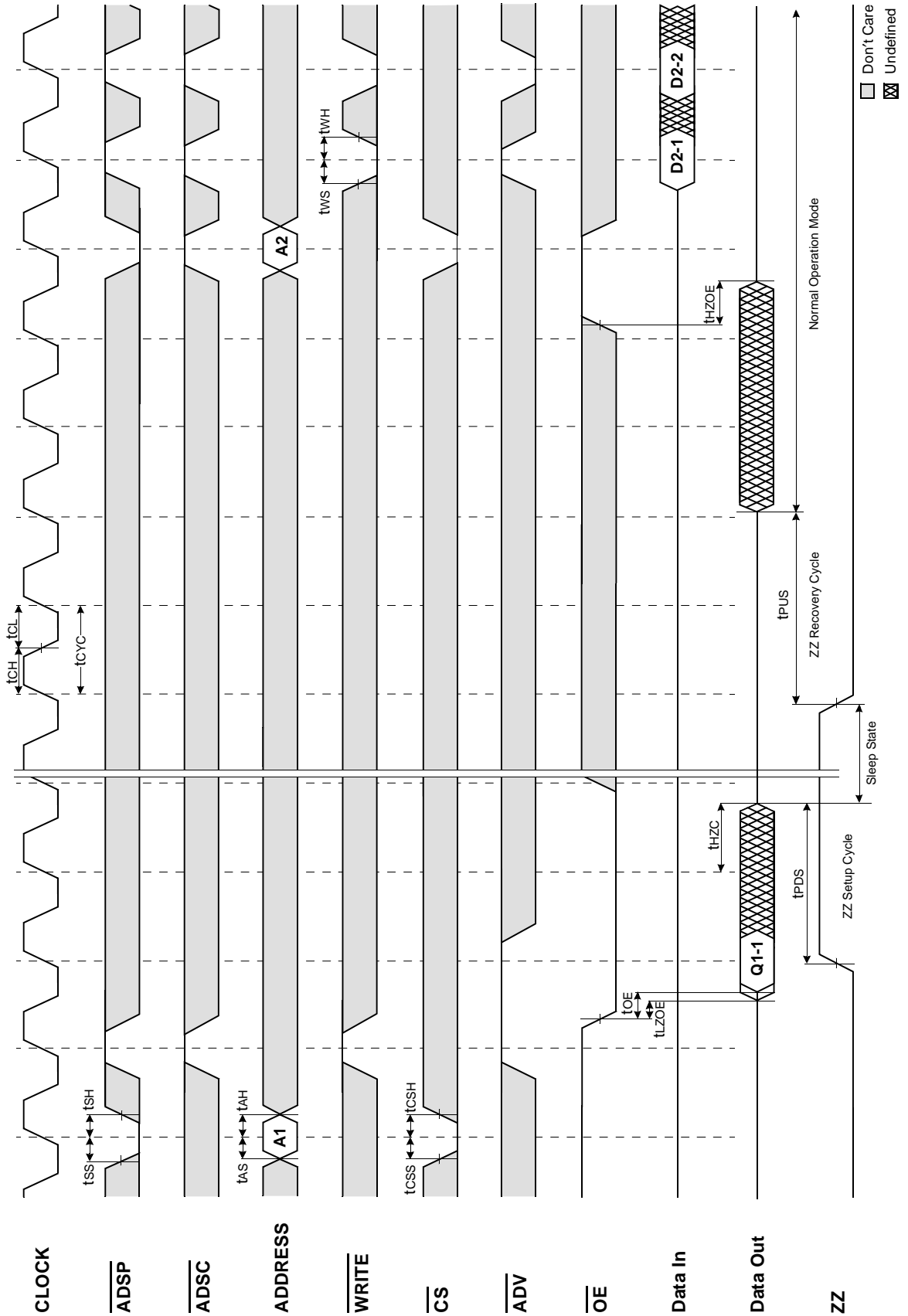
**TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED,  $\overline{\text{ADSC}}=\text{HIGH}$ )**



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED,  $\overline{\text{ADSP}}=\text{HIGH}$ )



TIMING WAVEFORM OF POWER DOWN CYCLE

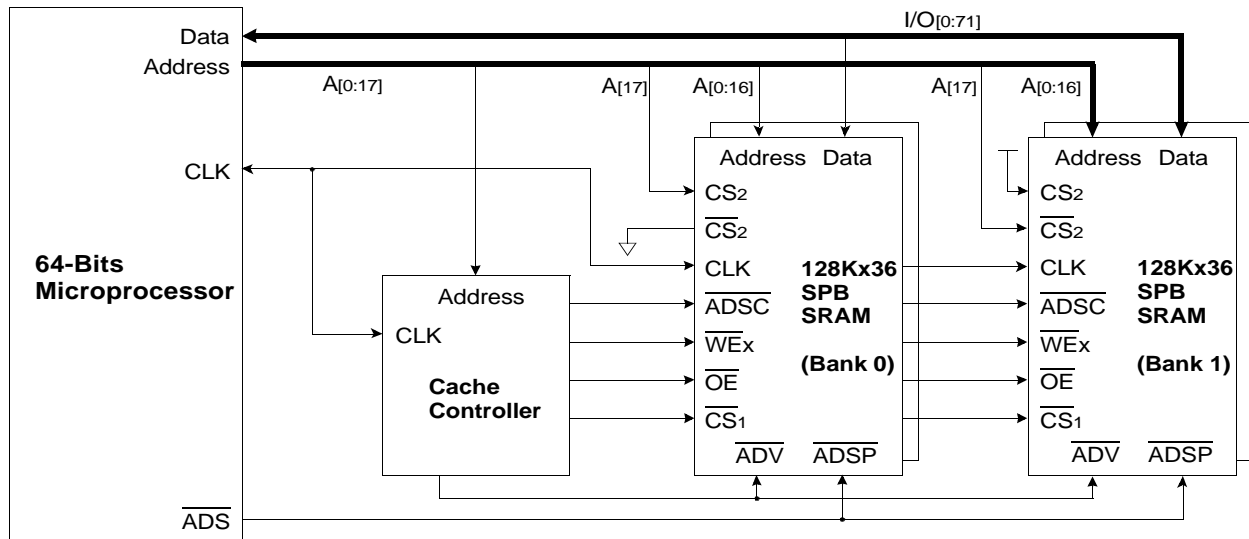


□ Don't Care  
 ⊠ Undefined

APPLICATION INFORMATION

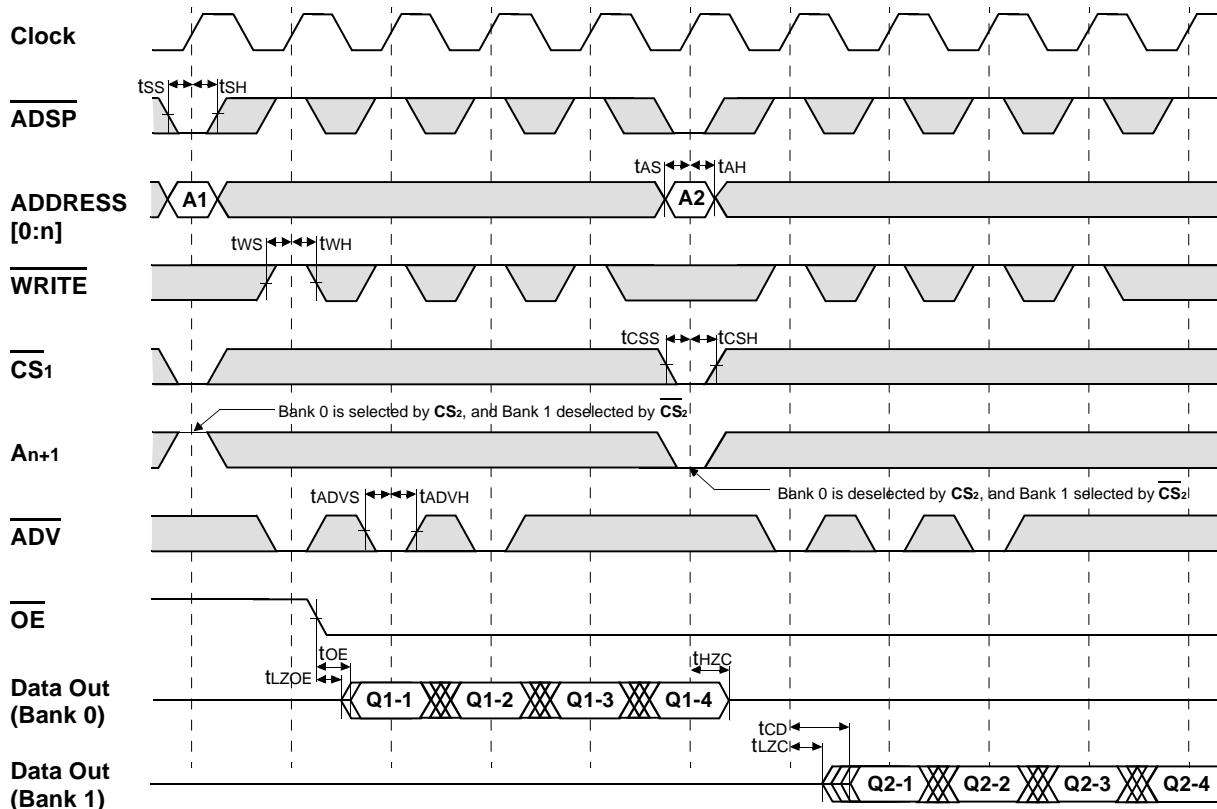
DEPTH EXPANSION

The Samsung 128Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



\*Notes : n = 14 32K depth  
 15 64K depth  
 16 128K depth  
 17 256K depth

□ Don't Care    ⊗ Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A

Units: millimeters/inches

