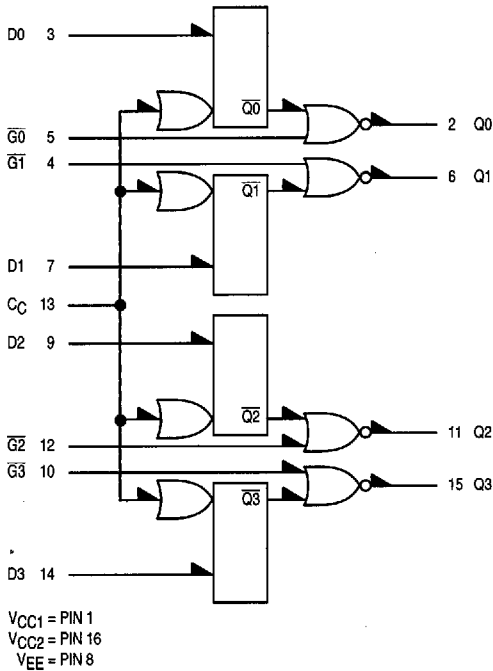


Quad Latch

The MC10168 is a Quad Latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative-going transition of the clock.

$P_D = 310 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = \bar{G} \text{ to } Q = 2 \text{ ns typ}$
 D to Q = 3 ns typ
 C to Q = 4 ns typ
 $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$

LOGIC DIAGRAM



TRUTH TABLE

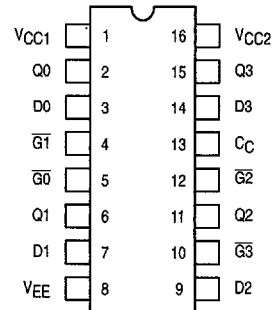
\bar{G}	C	D	Q_{n+1}
H	X	X	L
L	L	X	Q_n
L	H	L	L
L	H	H	H

MC10168



P SUFFIX
PLASTIC PACKAGE
CASE 648-08

PIN ASSIGNMENT



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		82		60	75		82	mAdc
Input Current	I_{inH}	3,7,9,14 4,5,10,12 13		390 425 460			245 265 290		245 265 290	μ Adc
	I_{inL}	*	0.5		0.5			0.3		μ Adc
Output Voltage	Logic 1 V_{OH}	2 6	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc
Output Voltage	Logic 0 V_{OL}	2 6	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc
Threshold Voltage	Logic 1 V_{OHA}	2 6	-1.080 -1.080		-0.980 -0.980			-0.910 -0.910		Vdc
Threshold Voltage	Logic 0 V_{OLA}	2 6		-1.655 -1.655			-1.630 -1.630		-1.595 -1.595	Vdc
Switching Times (50 Ω Load)										ns
Propagation Delay	Data t_{3+2+}	2	1.0	5.6	1.0	3.0	5.4	1.1	5.9	
	Gate t_{5-2+}	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4	
	Clock t_{13+2+}	2	1.0	5.8	1.0	4.0	5.6	1.2	6.2	
Setup Time	t_{3+13+}	2	2.5		2.5			2.5		
Hold Time	t_{13+3+}	2	1.0		1.0			1.0		
Rise Time (20 to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	
Fall Time (20 to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	

* Individually test each input applying V_{IH} or V_{IL} to input under test.

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ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)					
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
@ Test Temperature								
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2	
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2	
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
Power Supply Drain Current	I _E	8					8	1, 16
Input Current	I _{inH}	3,7,9,14	*				8	1, 16
		4,5,10,12 13	*				8	1, 16
Output Voltage	Logic 1	V _{OH}	2	3, 13			8	1, 16
			6	7, 13			8	1, 16
Output Voltage	Logic 0	V _{OL}	2	3, 5			8	1, 16
			6	4, 7			8	1, 16
Threshold Voltage	Logic 1	V _{OHA}	2	13		3	8	1, 16
			6	13		7	8	1, 16
Threshold Voltage	Logic 0	V _{OLA}	2	13		3	8	1, 16
			6	13		7	8	1, 16
Switching Times	(50Ω Load)		+1.11V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	Data	t ₃₊₂₊	2		3	2	8	1, 16
	Gate	t ₅₋₂₊	2		5	2	8	1, 16
	Clock	t ₁₃₊₂₊	2		13	2	8	1, 16
Setup Time		t ₃₊₁₃₊	2				8	1, 16
Hold Time		t ₁₃₊₃₊	2				8	1, 16
Rise Time	(20 to 80%)	t ₂₊	2		3	2	8	1, 16
Fall Time	(20 to 80%)	t ₂₋	2		3	2	8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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