TOSHIBA

3-to-8 Line Decoder/Latch

The TC74HC237A is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs (Y0 - Y1) will go high.
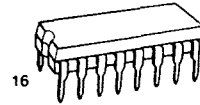
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all the outputs go low.

G1, G2A, and G2B inputs are provided to ease cascade connection and for use as an address decoder for memory systems.
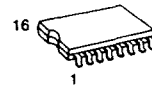
All inputs are equipped with protection circuits against static discharge or transient excess voltage.
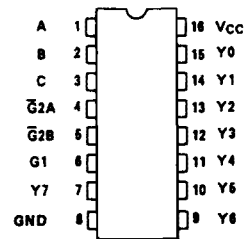
Features

- High Speed: t_{pd} = 14ns(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28%V_{CC}(Min.)
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS238

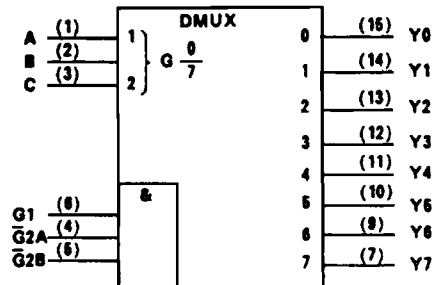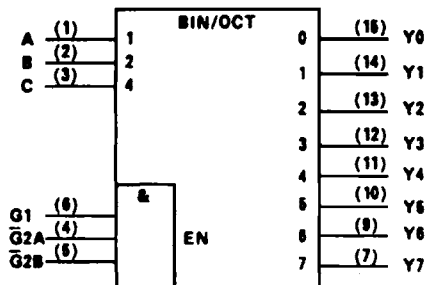|			
A	1	16	Vcc
B	2	15	Y0
C	3	14	Y1
$\overline{G}2A$	4	13	Y2
$\overline{G}2B$	5	12	Y3
G1	6	11	Y4
Y7	7	10	Y5
GND	8	9	Y6

(TOP VIEW)

Pin Assignment

IEC Logic Symbol

Truth Table

Inputs						Outputs								Selected Output
Enable			Select											
GL	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
L	X	X	X	X	X	L	L	L	L	L	L	L	L	None
X	H	X	X	X	X	L	L	L	L	L	L	L	L	None
X	X	H	X	X	X	L	L	L	L	L	L	L	L	None
H	L	L	L	L	L	H	L	L	L	L	L	L	L	Y0
H	L	L	L	L	H	L	H	L	L	L	L	L	L	Y1
H	L	L	L	H	L	L	L	H	L	L	L	L	L	Y2
H	L	L	L	H	H	L	L	L	H	L	L	L	L	Y3
H	L	L	H	L	L	L	L	L	L	H	L	L	L	Y4
H	L	L	H	L	H	L	L	L	L	L	H	L	L	Y5
H	L	L	H	H	L	L	L	L	L	L	L	H	L	Y6
H	L	L	H	H	H	L	L	L	L	L	L	L	H	Y7

X: Don't Care

Logic Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(0 ~V_{CC} = 2.0V) 0 ~ 500(0 ~V_{CC} = 4.5V) 0 ~ 400(0 ~V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C			Ta = -40 ~ 85°C		Unit
					Min.	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	—		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	—		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20µA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -4 mA I_{OH} = -5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20µA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	µA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	

AC Electrical Characteristics (C$_L$ = 15pF, V$_{CC}$ = 5V, Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	4	8	
Propagation Delay Time ($\overline{A,B,C}$-$\overline{Y}$)	t_{pLH} t_{pHL}	–	–	14	26	ns
Propagation Delay Time (G,G-Y)	t_{pLH} t_{pHL}	–	–	14	26	

AC Electrical Characteristics (C$_L$ = 50pF, Input t$_r$ = t$_f$ = 6ns)

Parameter	Symbol	Test Condition	V$_{CC}$	Ta = 25°C			Ta = -40 ~ 85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	2.0	–	30	75	–	95	
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A,B,C-Y)	t_{pLH} t_{pHL}	–	2.0	–	50	150	–	190	ns
			4.5	–	17	30	–	38	
			6.0	–	15	26	–	32	
Propagation Delay Time (G, $\overline{G}$-Y)	t_{pLH} t_{pHL}	–	2.0	–	50	150	–	190	
			4.5	–	17	30	–	38	
			6.0	–	15	26	–	32	
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$	–		–	53	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$