SILICON EPITAXIAL TRANSISTORS

NPN transistors in a microminiature (SMD) plastic package intended for surface mounted applications. They are primarily intended for use in telephony and professional communication equipment.

QUICK REFERENCE DATA

Collector-base voltage (open emitter)	V_{CBO}	max.	60 V
Collector-emitter voltage (open base)	V_{CEO}	max.	40 V
Emitter-base voltage (open collector)	V_{EBO}	max.	6 V
Collector current (DC)	I_C	max.	200 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
DC current gain I_C = 10 mA; V_{CE} = 1 V	h_{FE}	100 to 300	
Transition frequency at f = 100 MHz I_C = 10 mA; V_{CE} = 20 V	f_T	min.	300 MHz

MECHANICAL DATA

Dimensions in mm

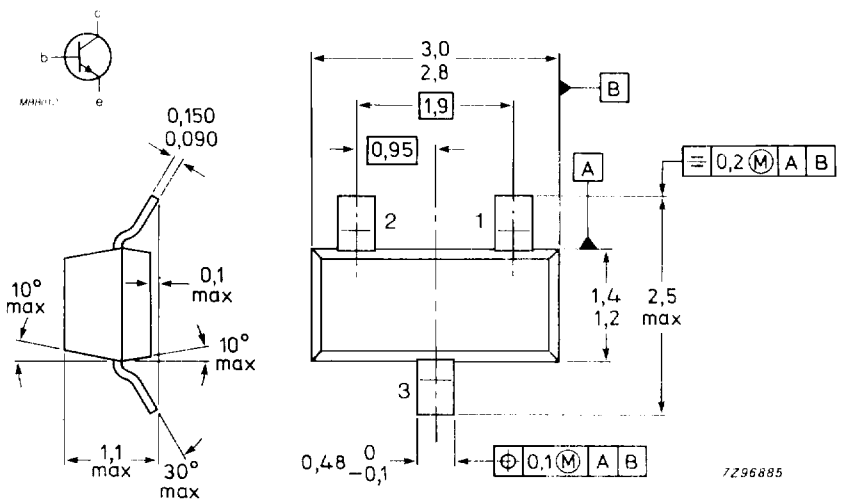
Fig.1 SOT23.

Marking code

PMBS3904: P9A

Pinning

1 = base
2 = emitter
3 = collector



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	60	V
Collector-emitter voltage (open base)	V_{CEO}	max.	40	V
Emitter-base voltage (open collector)	V_{EBO}	max.	6	V
Collector current (DC)	I_C	max.	200	mA
Total power dissipation* up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

$T_j = P\,(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

Thermal resistance from junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Collector-emitter breakdown voltage** I_C = 1 mA; I_B = 0	$V_{(BR)CEO}$	min.	40	V
Collector-base breakdown voltage I_C = 10 μA; I_E = 0	$V_{(BR)CBO}$	min.	60	V
Emitter-base breakdown voltage I_E = 10 μA; I_C = 0	$V_{(BR)EBO}$	min.	6	V
Collector cut-off current V_{CE} = 30 V; V_{EB} = 3 V	I_{CEX}	max.	50	nA
Output capacitance at f = 1 MHz I_E = 0; V_{CB} = 5 V	C_c	max.	4	pF
Input capacitance at f = 1 MHz I_C = 0; V_{BE} = 0,5 V	C_e	max.	8	pF
Base current with reverse biased emitter junction V_{EB} = 3 V; V_{CE} = 30 V	I_{BEX}	max.	50	nA

* Mounted on a ceramic substrate: area = 10 x 8 mm²; thickness = 0.7 mm.

** Pulse test conditions: t_p = 300 μs; duty factor ≤ 2%.

Saturation voltages			
I_C = 10 mA; I_B = 1 mA	V_{CEsat}	max.	0.2 V
I_C = 50 mA; I_B = 5 mA	V_{CEsat}	max.	0.3 V
I_C = 10 mA; I_B = 1 mA	V_{BEsat}	min.	0.65 V
	V_{BEsat}	max.	0.85 V
I_C = 50 mA; I_B = 5 mA	V_{BEsat}	max.	0.95 V
DC current gain*			
I_C = 0.1 mA; V_{CE} = 1 V	h_{FE}	min.	40
I_C = 1 mA; V_{CE} = 1 V	h_{FE}	min.	70
I_C = 10 mA; V_{CE} = 1 V	h_{FE}	min.	100
	h_{FE}	max.	300
I_C = 50 mA; V_{CE} = 1 V	h_{FE}	min.	60
I_C = 100 mA; V_{CE} = 1 V	h_{FE}	min.	30
Transition frequency at f = 100 MHz			
I_C = 10 mA; V_{CE} = 20 V	f_T	min.	300 MHz
Noise figure at R_S = 1 kΩ			
I_C = 100 μA; V_{CE} = 5 V			
f = 10 Hz to 15.7 kHz	F	max.	5 dB
h-parameters (common emitter)			
I_C = 1 mA; V_{CE} = 10 V; f = 1 kHz			
Input impedance	h_{ie}		1 to 10 kΩ
Reverse voltage transfer ratio	h_{re}		0.5 to 8 10^{-4}
Small-signal current gain	h_{fe}		100 to 400
Output admittance	h_{oe}		1 to 40 μs

* Pulse test condition: t_p = 300 μs; duty factor ≤ 2%.