Document Title

256K x8 bit 3.3V Low Power CMOS slow SRAM

Revision History

Revision No	History	Draft Date	Remark
10	Initial Revision History Insert Revised - Improved operating current Icc1 : 60mA -> 35mA	Jul.29.2000	Final
11	Change the Notch Location of sTSOP - Left-Top => Left-Center	Sep.04.2000	Final
12	Revised - V_{IH} max : Vcc + 0.2V => Vcc + 0.3V - V_{IL} min : - 0.2V => - 0.3V	Dec.16.2000	Final
13	Changed Logo - HYUNDAI -> hynix	Apr.30.2001	Final

DESCRIPTION

The HY62V8200 is a high speed, low power and 2M bit CMOS SRAM organized as 262,144 words by 8bit. The HY62V8200 uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particularly well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

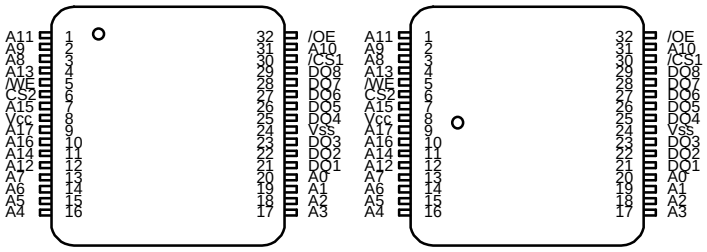
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL-part)
  -. 2.0V(min) data retention
- Standard pin configuration
  -. 32-sTSOPI-8X13.4, 32-TSOPI -8X20
  (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)	Temperature (°C)
HY62V8200	3.0~3.6	70*/85/100	5	25	0~70
HY62V8200-E	3.0~3.6	70*/85/100	5	25	-25~85(E)
HY62V8200-I	3.0~3.6	70*/85/100	5	25	-40~85(I)

Note 1. Blank : Commercial, E : Extended, I : Industrial
2. Current value is max.
* 70ns is available with 30pF test load

PIN CONNECTION



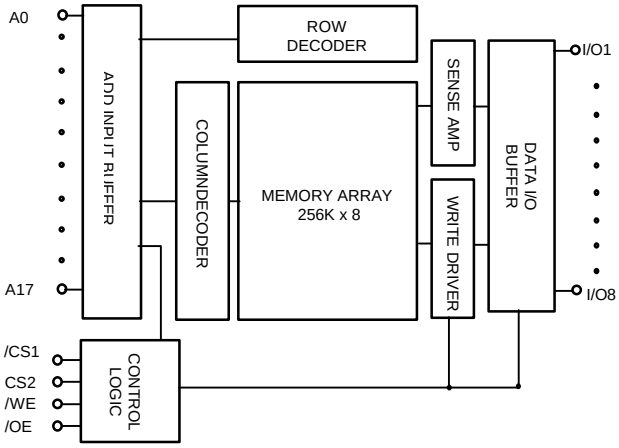
TSOP-I
(Standard)

sTSOP-I
(Standard)

PIN DESCRIPTION

Pin Name	Pin Function
/CS1	Chip Select 1
CS2	Chip Select 2
/WE	Write Enable
/OE	Output Enable
A0 ~ A17	Address Input
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(3.0V~3.6V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62V8200LLT1	70*/85/100	LL-part		TSOPI(Standard)
HY62V8200LLR1	70*/85/100	LL-part		TSOPI(Reversed)
HY62V8200LLST	70*/85/100	LL-part		Smaller TSOPI(Standard)
HY62V8200LLSR	70*/85/100	LL-part		Smaller TSOPI(Reversed)
HY62V8200LLT1-E	70*/85/100	LL-part	E	TSOPI(Standard)
HY62V8200LLR1-E	70*/85/100	LL-part	E	TSOPI(Reversed)
HY62V8200LLST-E	70*/85/100	LL-part	E	Smaller TSOPI(Standard)
HY62V8200LLSR-E	70*/85/100	LL-part	E	Smaller TSOPI(Reversed)
HY62V8200LLT1-I	70*/85/100	LL-part	I	TSOPI(Standard)
HY62V8200LLR1-I	70*/85/100	LL-part	I	TSOPI(Reversed)
HY62V8200LLST-I	70*/85/100	LL-part	I	Smaller TSOPI(Standard)
HY62V8200LLSR-I	70*/85/100	LL-part	I	Smaller TSOPI(Reversed)

Note 1. Blank : Commercial, E : Extended, I : Industrial
* 70ns is available with 30pF test load

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.2 to 3.9	V	
V_{CC}	Voltage on Vcc supply relative to Vss	-0.2 to 4.0	V	
T_A	Operating Temperature	0 to 70	°C	HY62V8200
		-25 to 85	°C	HY62V8200-E
		-40 to 85	°C	HY62V8200-I
T_{STG}	Storage Temperature	-55 to 150	°C	
P_D	Power Dissipation	1.0	W	
I_{OUT}	Data Output Current	50	mA	
T_{SOLDER}	Lead Soldering Temperature & Time	260 • 5	°C•sec	

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS1	CS2	/WE	/OE	Mode	I/O	Power
H	X	X	X	Deselected	High-Z	Standby
X	L	X	X	Deselected	High-Z	Standby
L	H	H	H	Output Disabled	High-Z	Active
L	H	H	L	Read	Dout	Active
L	H	L	X	Write	D_{IN}	Active

Note :
1. H=V_{IH}, L=V_{IL}, X=don't care(V_{IH} or V_{IL})

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.4	V

Note
1. V_{IL} = -1.5V for pulse width less than 30ns

DC ELCTRICAL CHARACTERISTICS

Vcc= 3.0~3.6V, T_A = 0°C to 70°C/ -25°C to 85°C (E)/ -40°C to 85°C (I), unless otherwise specified

Sym.	Parameter		Test Condition	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current		Vss ≤ V_{IN} ≤ Vcc	-1	-	1	uA
I_{LO}	Output Leakage Current		Vss ≤ V_{OUT} ≤ Vcc, /CS1 = V_{IH} or CS2 = V_{IL} or /OE = V_{IH} or /WE = V_{IL}	-1	-	1	uA
Icc	Operating Power Supply Current		/CS1 = V_{IL}, CS2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA	-	-	5	mA
I_{CC1}	Average Operating Current		Min Duty Cycle = 100%, /CS1 = V_{IL} CS2 = V_{IH} V_{IN} = V_{IH} or V_{IL}	-	-	35	mA
			Cycle time = 1us, $I_{I/O}$ = 0mA, /CS1 ≤ 0.2V, CS2 ≥ Vcc - 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ Vcc – 0.2V	-	-	6	mA
I_{SB}	TTL Standby Current (TTL Input)		/CS1 = V_{IH} or CS2 = V_{IL} -	-	-	0.5	mA
I_{SB1}	Standby Current (CMOS Input)	HY62V8200B	/CS1 ≥ Vcc - 0.2V, CS2 ≥ 0.2V or CS2 ≥ Vcc - 0.2V	-	-	25	uA
		HY62V8200B-E		-	-	25	uA
		HY62V8200B-I		-	-	25	uA
V_{OL}	Output Low Voltage		I_{OL} = 2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage		I_{OH} = -1mA	2.2	-	-	V

Note : Typical values are at Vcc = 3.3V, T_A = 25°C

CAPACITANCE

(Temp = 25°C, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	10	pF

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

Vcc= 3.0V~3.6V, T_A = 0°C to 70°C/ -25°C to 85°C(E)/ -40°C to 85°C(I), unless otherwise specified

#	Symbol	Parameter	-70*		-85		-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	70	-	85	-	100	-	ns
2	tAA	Address Access Time	-	70	-	85	-	100	ns
3	tACS	Chip Select Access Time	-	70	-	85	-	100	ns
4	tOE	Output Enable to Output Valid	-	40	-	45	-	50	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	20	0	25	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	25	0	30	ns
9	tOH	Output Hold from Address Change	15	-	15	-	15	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	70	-	85	-	100	-	ns
11	tCW	Chip Selection to End of Write	60	-	70	-	80	-	ns
12	tAW	Address Valid to End of Write	60	-	70	-	80	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	50	-	60	-	70	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	25	0	30	ns
17	tDW	Data to Write Time Overlap	30	-	35	-	40	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

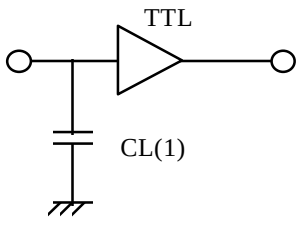
AC TEST CONDITIONS

T_A = 0°C to 70°C / -25°C to 85°C (E)/ -40°C to 85°C (I), unless otherwise specified

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	tCLZ,tOLZ,tCHZ,tOHZ,tWHZ,tOW	CL = 5pF + 1TTL Load
	Others	CL = 100pF + 1TTL Load
		CL = 30pF + 1TTL Load

Note
* : Test load is 30pF for 70ns device.

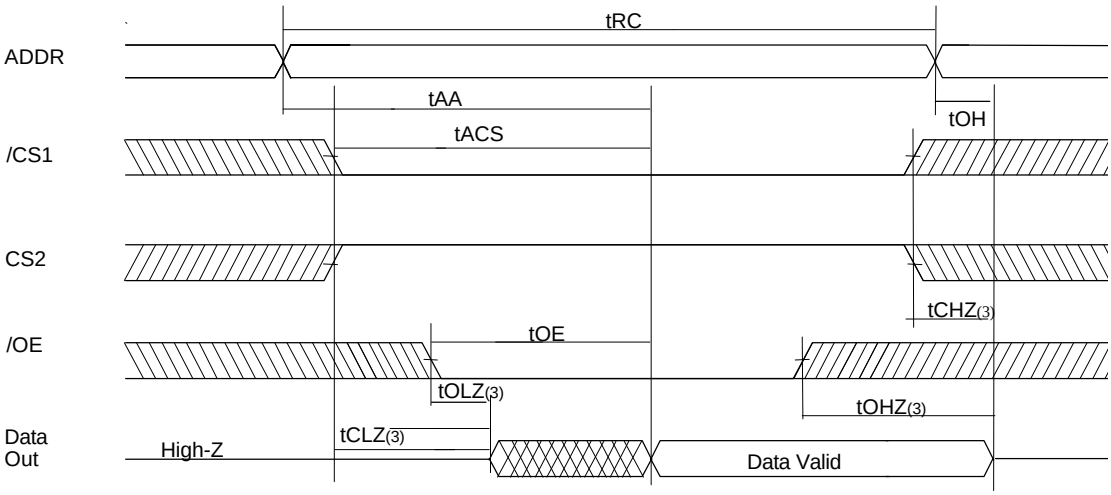
AC TEST LOADS



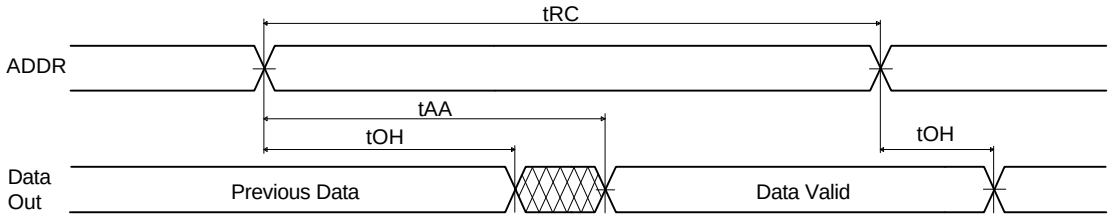
Note : 1 Including jig and scope capacitance

TIMING DIAGRAM

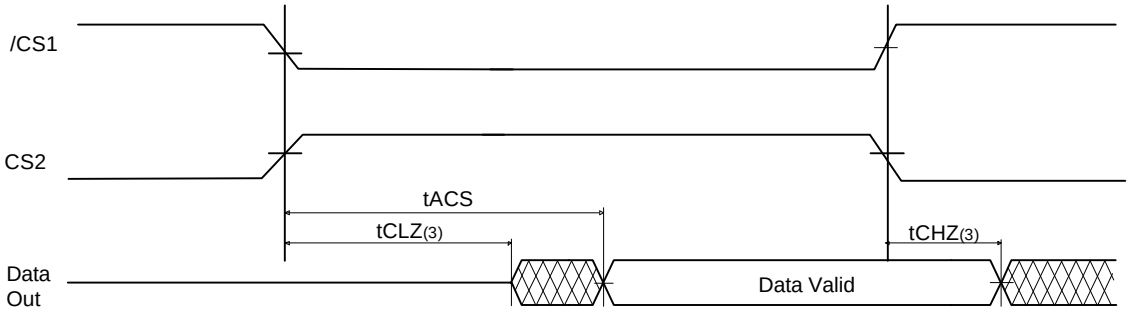
READ CYCLE 1(Note1,4)



READ CYCLE 2(Note 1,2,4)

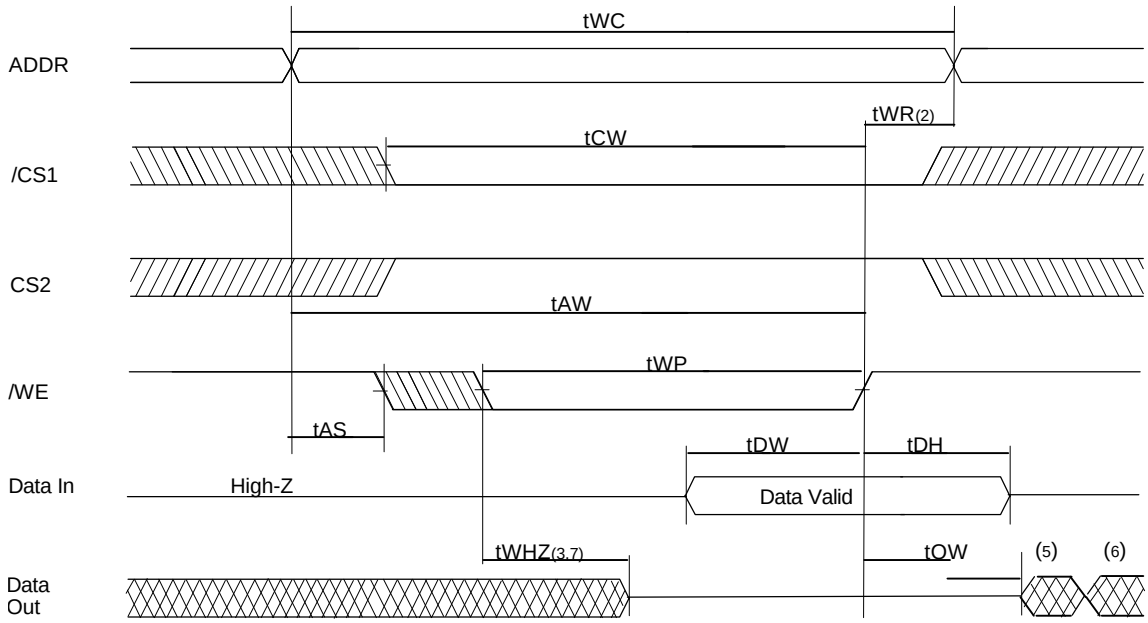


READ CYCLE 3(Note 1,2,4)

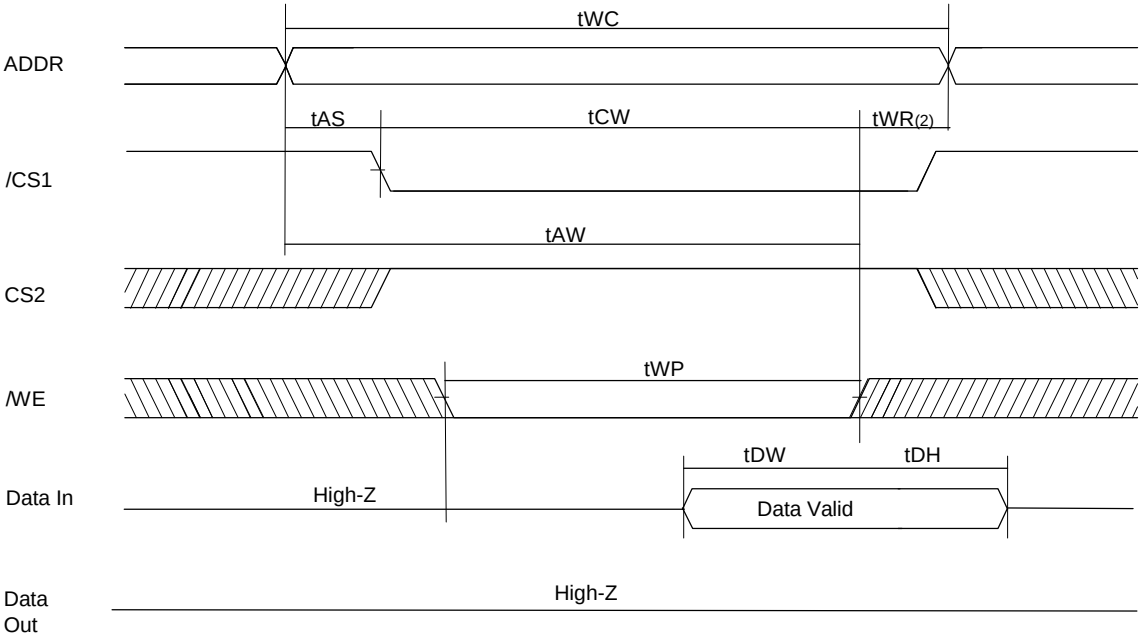


Notes:
1. A read occurs during the overlap of a low /OE, a high /WE, a low /CS1 and a high CS2.
2. /OE = V_{IL}
3. Transition is measured ± 200mV from steady state voltage.
   This parameter is sampled and not 100% tested.
4. /CS1 in high for the standby, low for active
   CS2 in low for the standby, high for active

WRITE CYCLE 1(1,4,5,8) (/WE Controlled)



WRITE CYCLE 1(1,4,5,8) (/CS1, CS2 Controlled)



Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /WE, a low /CS1 and a high CS2. A write begins at the latest transition among /CS1 going now, CS2 going high and /WE going low: A write ends at the earliest transition among /CS1 going high, CS2 low and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR1 is applied in case a write ends as /CS1, or /WE going high, and tWR2 is applied in case a write ends at CS2 going low.
5. If /OE, CS2 and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS1 goes low simultaneously with /WE going low, the outputs remain in high impedance state.
7. Dout is the read data of the new address.
8. When /CS1 is low and CS2 is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

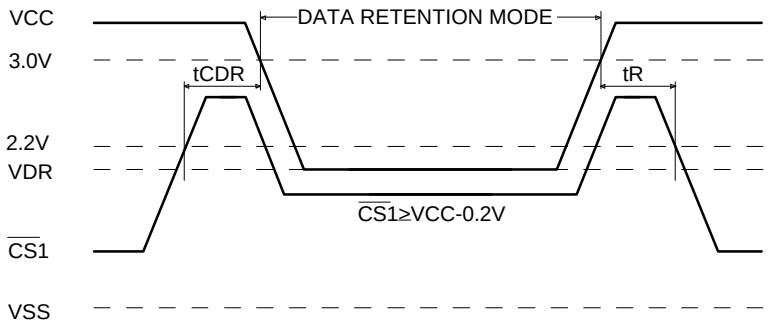
DATA RETENTION ELECTRIC CHARACTERISTIC

T_A = 0°C to 70°C / -25°C to 85°C (E)/ -40°C to 85°C (I)

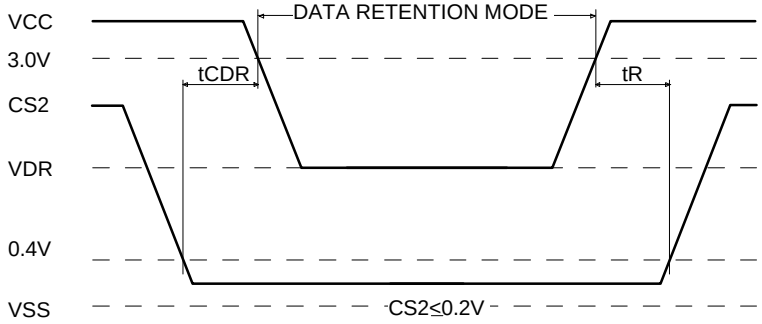
Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	Vcc for Data Retention		/CS1≥Vcc-0.2V, CS2≤0.2V or ≥Vcc – 0.2V, Vss≤V_{IN}≤Vcc	2.0	-	-	V
I_{CCDR}	Data Retention Current	HY62V8200	Vcc=3.0V, /CS1≥Vcc - 0.2V, CS2≤0.2V or ≥Vcc – 0.2V, Vss≤V_{IN}≤Vcc	-	-	25	uA
		HY62V8200-E		-	-	25	uA
		HY62V8200-I		-	-	25	uA
tCDR	Chip Deselect to Data Retention Time		See Data Retention Timing Diagram	0	-	-	ns
tR	Operating Recovery Time			5	-	-	ms

Notes:
1. Typical values are under the condition of T_A = 25°C.

DATA RETENTION TIMING DIAGRAM 1

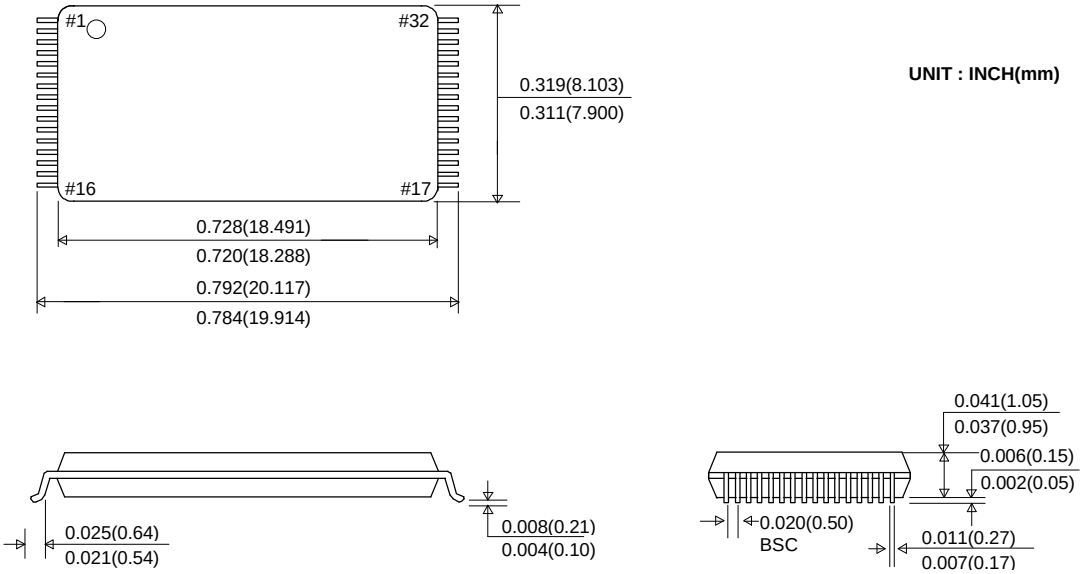


DATA RETENTION TIMING DIAGRAM 2



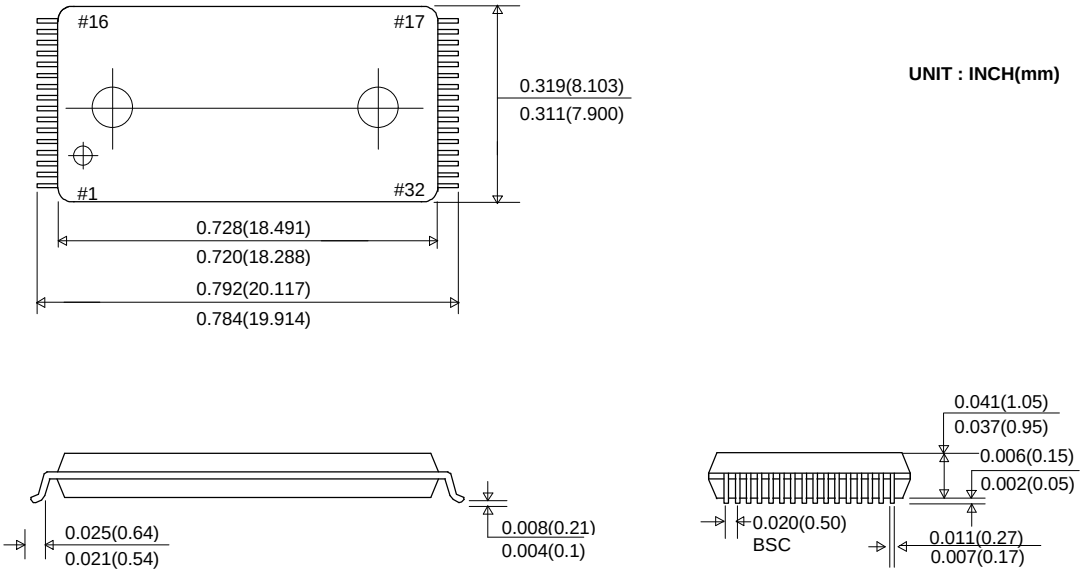
PACKAGE INFORMATION

32pin 8x20mm Thin Small Outline Package Standard(T1)



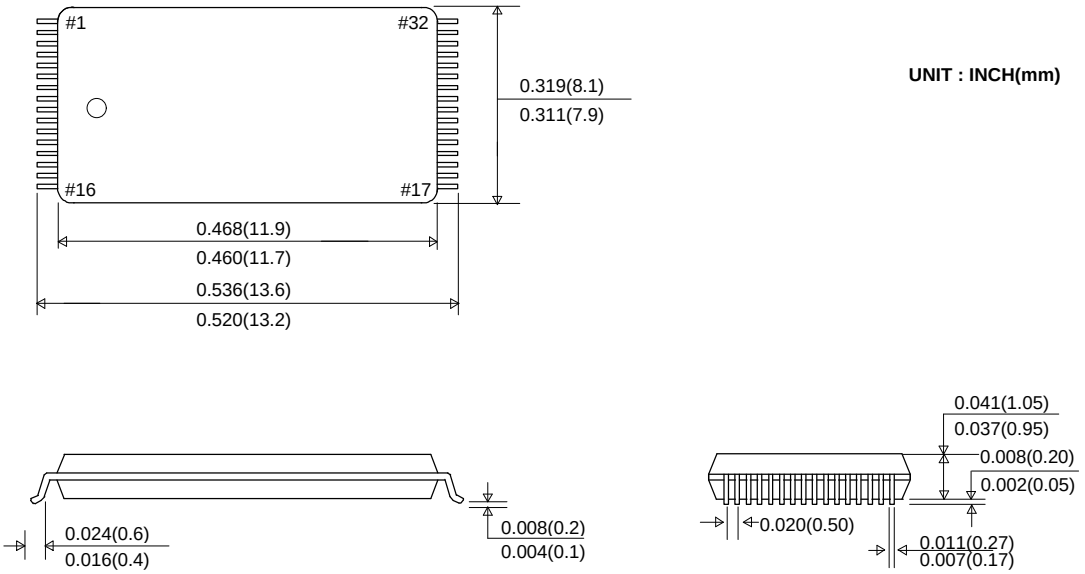
UNIT : INCH(mm)

32pin 8x20mm Thin Small Outline Package Reversed(R1)



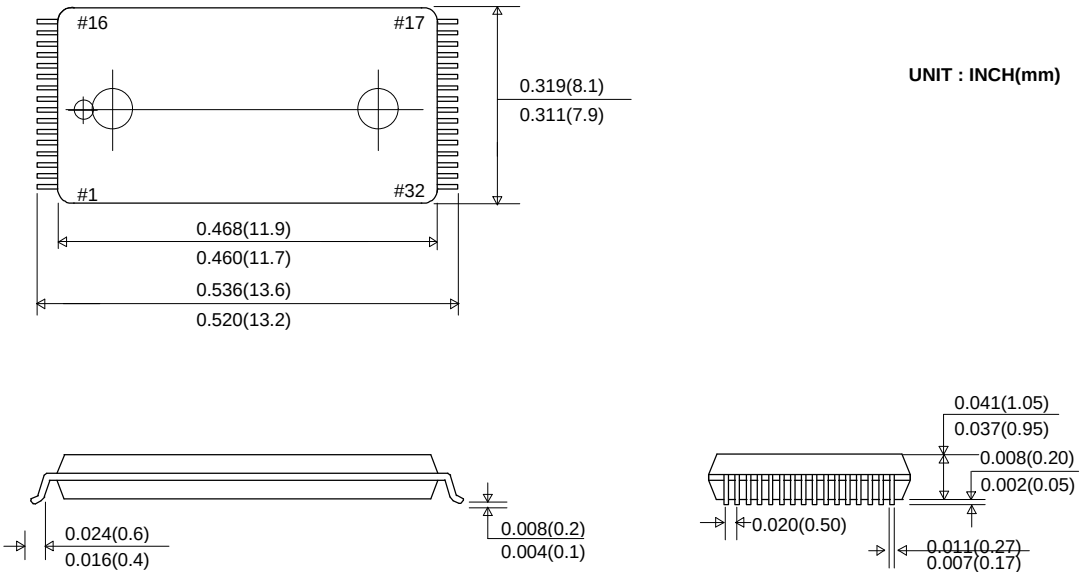
UNIT : INCH(mm)

32pin 8x13.4mm Smaller Thin Small Outline Package Standard(ST)



UNIT : INCH(mm)

32pin 8x13.4mm Smaller Thin Small Outline Package Reversed(SR)



UNIT : INCH(mm)