FEMTOCLOCKS™ DIFFERENTIAL CLOCK GENERATOR FOR PCI EXPRESS

ICS841604I

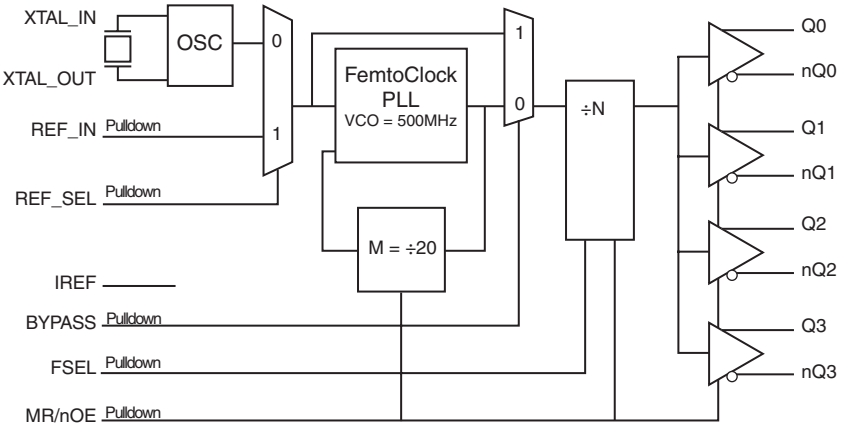
General Description

The ICS841604I is an optimized PCIe and sRIO clock generator and member of the HiPerClocks™ family of high-performance clock solutions from ICS. The device uses a 25MHz parallel crystal to generate 100MHz and 125MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solutions. The device has excellent phase jitter (< 1ps rms) suitable to clock components requiring precise and low-jitter PCIe or sRIO or both clock signals. Designed for telecom, networking and industrial applications, the ICS841604I can also drive the high-speed sRIO and PCIe SerDes clock inputs of communication processors, DSPs, switches and bridges.

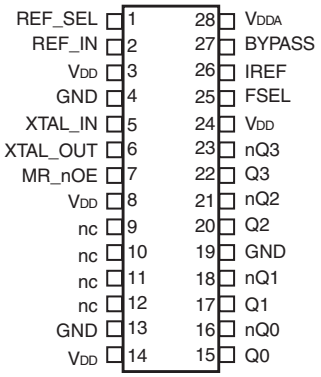
Features

- Four differential clock outputs: configurable for PCIe (100MHz) and sRIO (125MHz) clock signals
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference clock input
- Supports the following output frequencies: 100MHz or 125MHz
- VCO: 500MHz
- PLL bypass and output enable
- RMS phase jitter, 125MHz, using a 25MHz crystal: 0.38ps (typical)
- Full 3.3V power supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS841604I
28-Lead TSSOP
6.1mm x 9.7mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	REF_SEL	Input	Pulldown	Reference select. Selects the input reference source. LVCMOS/LVTTL interface levels.
2	REF_IN	Input	Pulldown	LVCMOS/LVTTL PLL reference clock input.
3, 8, 14, 24	V_{DD}	Power		Core supply pins.
4, 13, 19	GND	Power		Power supply ground.
5, 6	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. (PLL reference.)
7	MR/nOE	Input	Pulldown	Active HIGH master reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are in high impedance (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
9, 10, 11, 12	nc	Unused		No connect.
15, 16	Q0, nQ0	Output		Differential output pair. HCSL interface levels.
17, 18	Q1, nQ1	Output		Differential output pair. HCSL interface levels.
20, 21	Q2, nQ2	Output		Differential output pair. HCSL interface levels.
22, 23	Q3, nQ3	Output		Differential output pair. HCSL interface levels.
25	FSEL	Input	Pulldown	Output frequency select pin. LVCMOS/LVTTL interface levels.
26	IREF	Output		HCSL current reference resistor output. A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QX/nQX clock outputs.
27	BYPASS	Input	Pulldown	Selects PLL operation/PLL bypass operation. LVCMOS/LVTTL interface levels.
28	V_{DDA}	Power		Analog supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. FSEL FUNCTION TABLE (f_{ref} = 25MHz)

Input		Outputs
FSEL	N	Q0:1/nQ0:1
0	5	VCO/5 (100MHz) PCIe (default)
1	4	VCO/4 (125MHz) sRIO

TABLE 3B. BYPASS FUNCTION TABLE

Input	
BYPASS	PLL Configuration
0 (default)	PLL on
1	PLL bypassed (Q0:Q3/N)

NOTE 1: Asynchr. function (may cause output glitch).

TABLE 3C. MR/nOE FUNCTION TABLE

Input	
MR/nOE	Function[NOTE 1]
0 (default)	Outputs enabled
1	Device reset, outputs disabled (HI-Z)

NOTE 1: Asynchr. function (may cause output glitch).

TABLE 3D. REF_SEL FUNCTION TABLE

Input	
REF_SEL	Input Reference
0 (default)	XTAL
1	REF_IN

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	64.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.13	3.3	V_{DD}	V
I_{DD}	Power Supply Current			65		mA
I_{DDA}	Analog Supply Current			13		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_IN, REF_SEL, BYPASS, MR/nOE, FSEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	REF_IN, REF_SEL, BYPASS, MR/nOE, FSEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				TBD	Ω
Shunt Capacitance				7	pF
Drive Level				0.1	mW

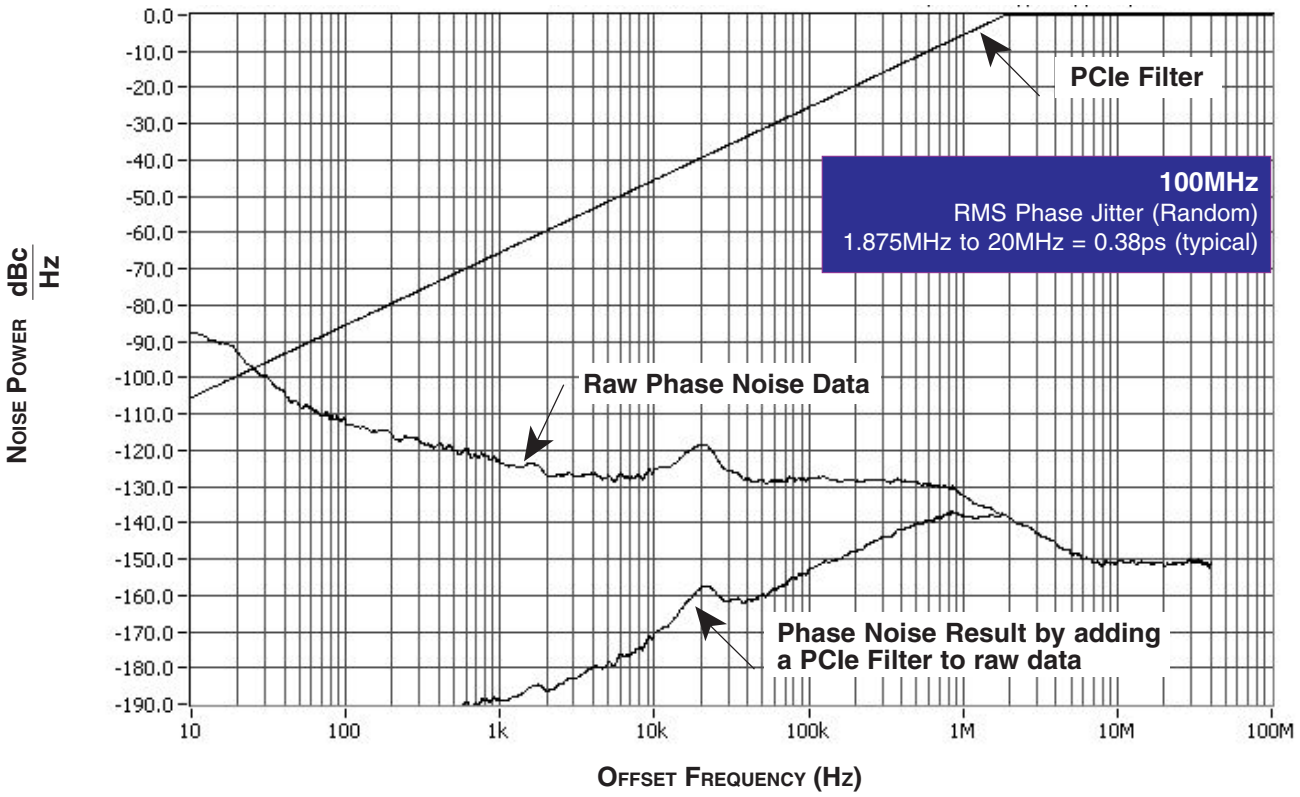
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = -40°C TO 85°C

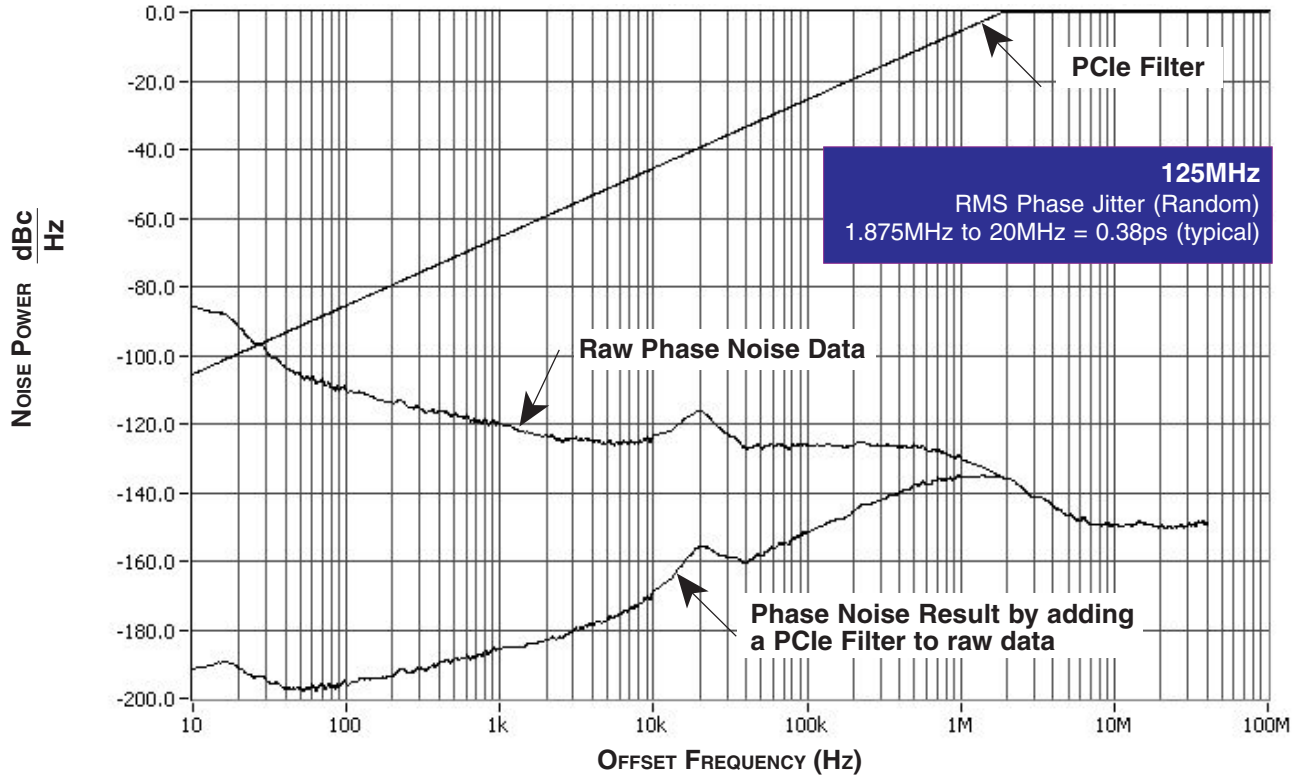
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	VCO/5		100		MHz
		VCO/4		125		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	100MHz, (1.875MHz - 20MHz)		0.38		ps
		125MHz, (1.875MHz - 20MHz)		0.38		ps
*t*sk(o)	Output Skew; NOTE 2, 3			50		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3			TBD		ps
t_L	PLL Lock Time				100	ms
V_{HIGH}	Voltage High		660		850	mV
V_{LOW}	Voltage Low		-150			mV
V_{OVS}	Max. Voltage, Overshoot				V_{HIGH} + 0.3	V
V_{UDS}	Min. Voltage, Undershoot		-0.3			V
V_{rb}	Ringback Voltage				0.2	V
V_{CROSS}	Absolute Crossing Voltage		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges				140	mV
t_R / t_F	Output Rise/Fall Time	measured between 0.175 to 0.525	175		700	ps
$\Delta t_R / \Delta t_F$	Rise/Fall Time Variation				125	ps
t_{RFM}	Rise/Fall Matching				125	ps
odc	Output Duty Cycle		45		55	%

NOTE: All specifications are taken at 100MHz and 125MHz.
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

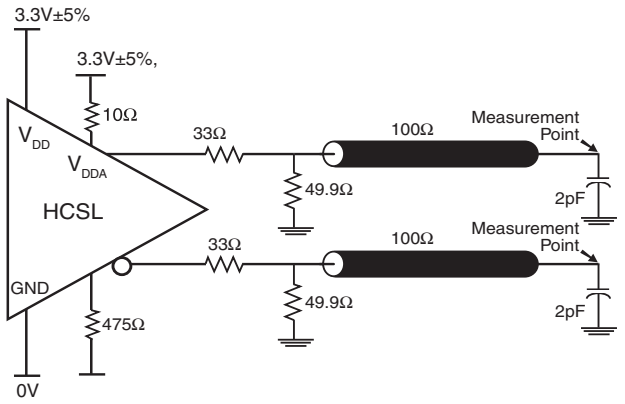
TYPICAL PHASE NOISE AT 100MHz



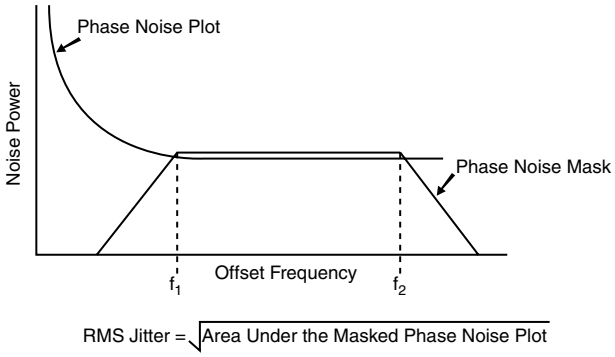
TYPICAL PHASE NOISE AT 125MHz



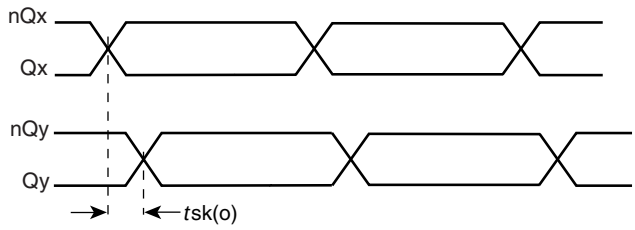
PARAMETER MEASUREMENT INFORMATION



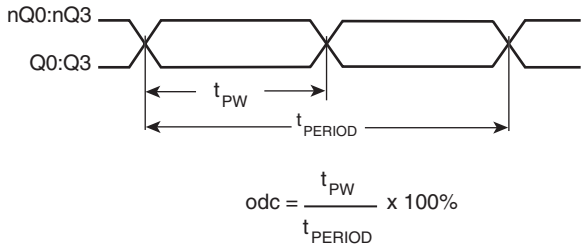
HCSL OUTPUT LOAD AC TEST CIRCUIT



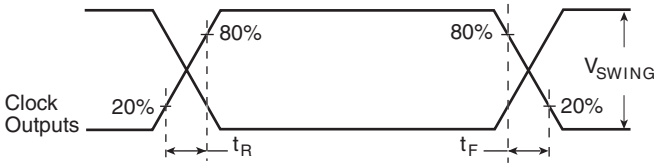
RMS PHASE JITTER



OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS841604I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a 0.01µF bypass capacitor should be connected to each V_{DDA}.

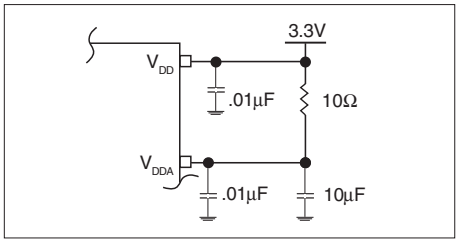


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS841604I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

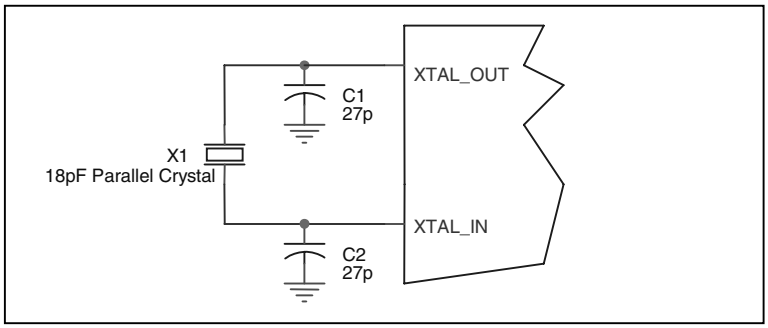


FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

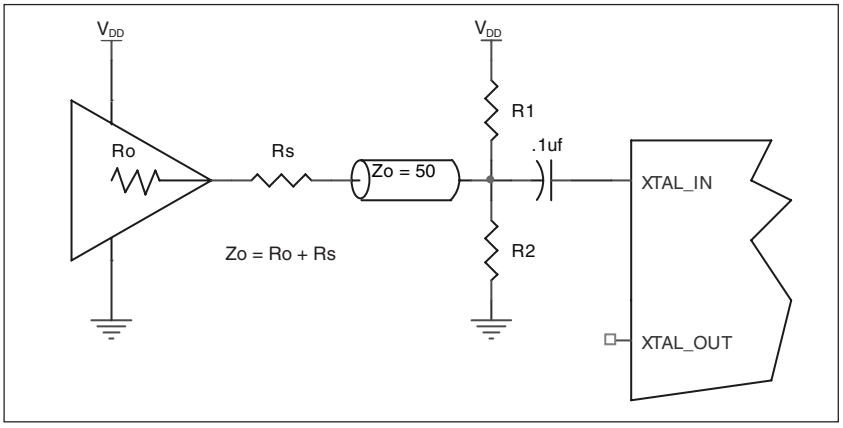


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_IN INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

DIFFERENTIAL OUTPUTS

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

SCHEMATIC EXAMPLE

Figure 4 shows an example of ICS841604I application schematic. In this example, the device is operated at V_{DD} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of HCSL terminations are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

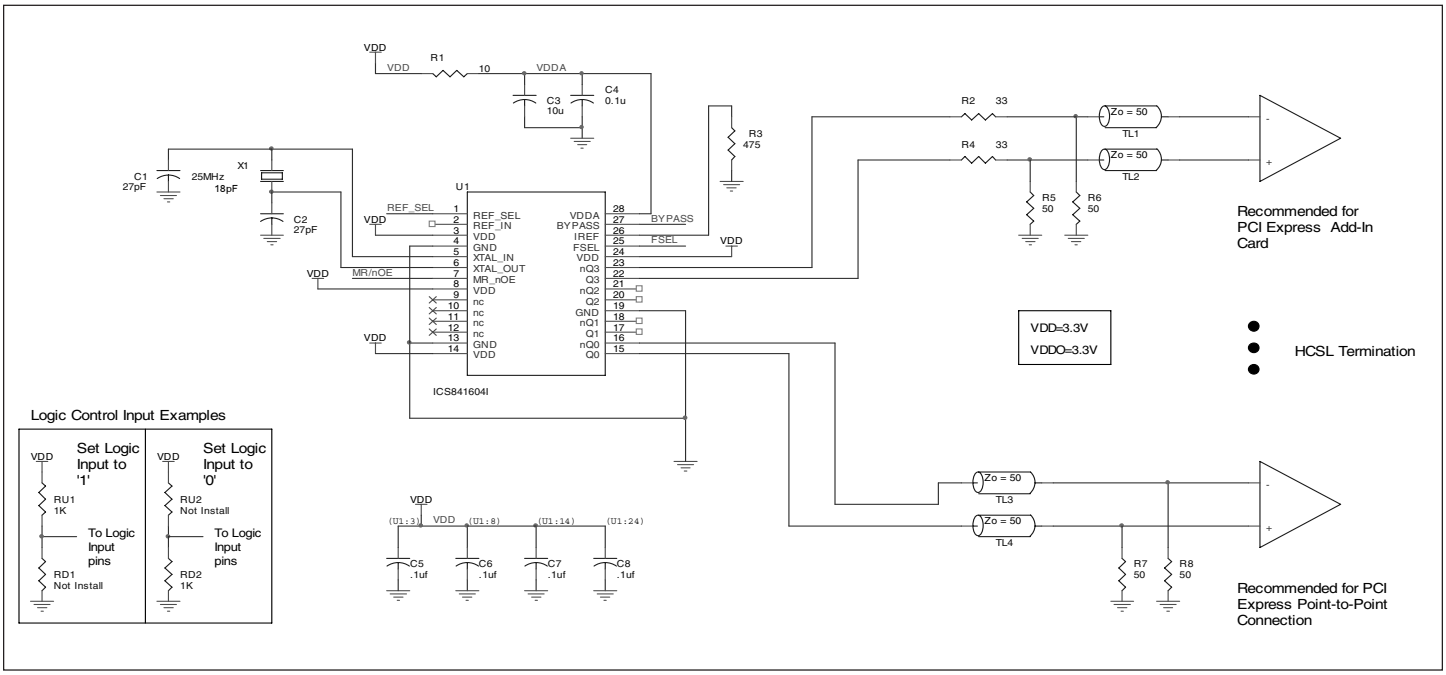


FIGURE 4. ICS841604I SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS841604I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS41604I is the sum of the core power plus the analog plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA})$ = 3.465V * (65mA + 13mA) = **270.27mW**
- Power $(outputs)_{MAX}$ = **45mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 45mW = **180mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 270.27mW + 180mW = **450.27mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in Section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 64.54°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.450W * 64.5°C/W = 114°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 28-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	64.5°C/W	60.4°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 5.*

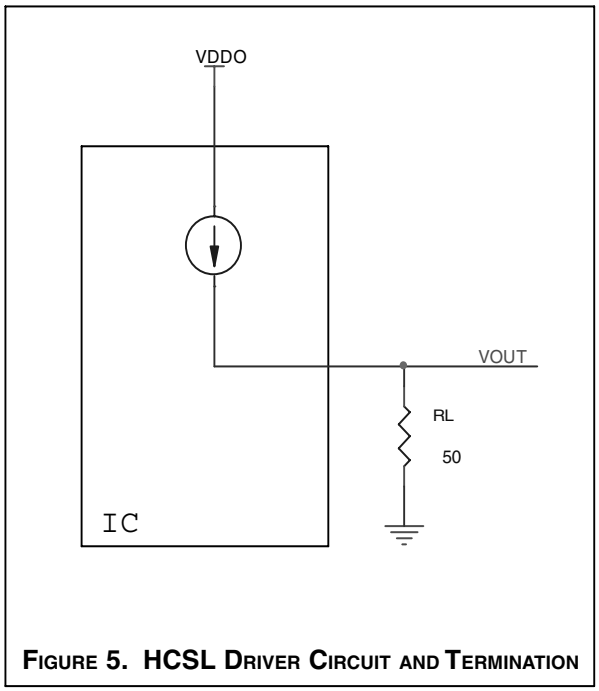


FIGURE 5. HCSL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{DD} – 2V.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$

$Pd\_L = (V_{OL\_MIN}/R_L) * V_{OL\_MIN}$

Pd_H = (0.85V/50Ω) * (3.465V – 0.85V) = **44.5mW**

Pd_L = (0.15V/50Ω) * 0.15V = **0.45mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **45mW**

RECOMMENDED TERMINATION

Figure 6A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

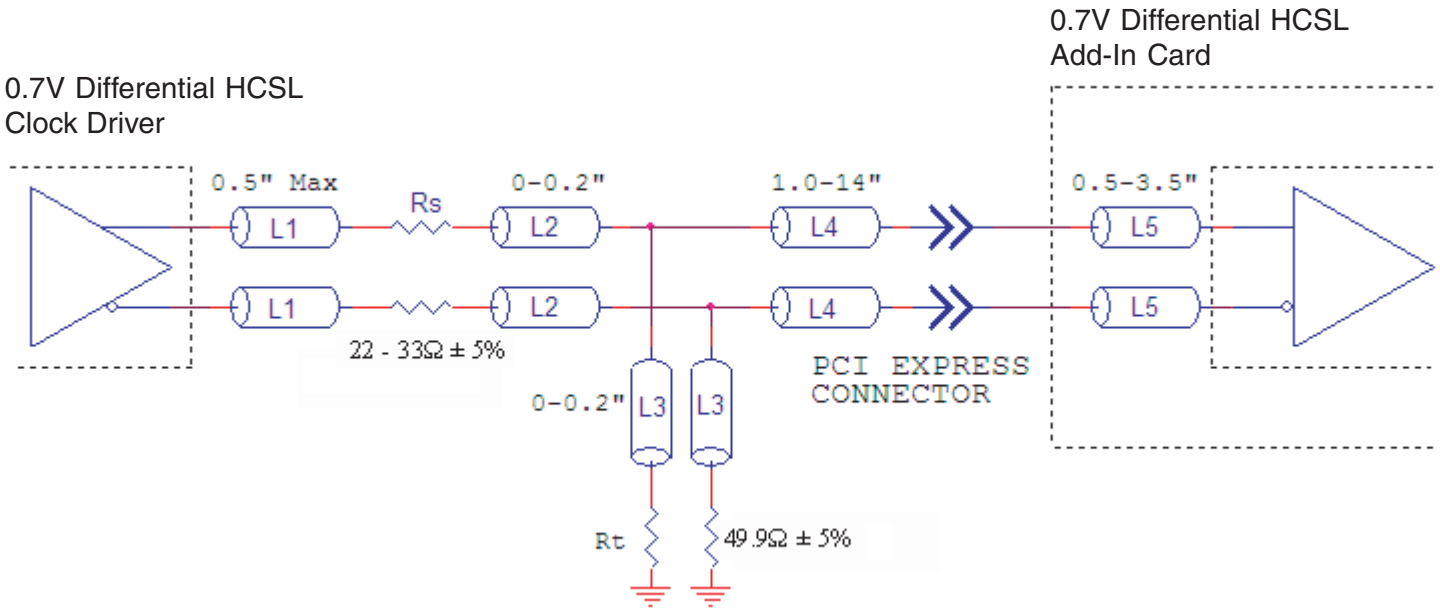


FIGURE 6A. RECOMMENDED TERMINATION

Figure 6B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

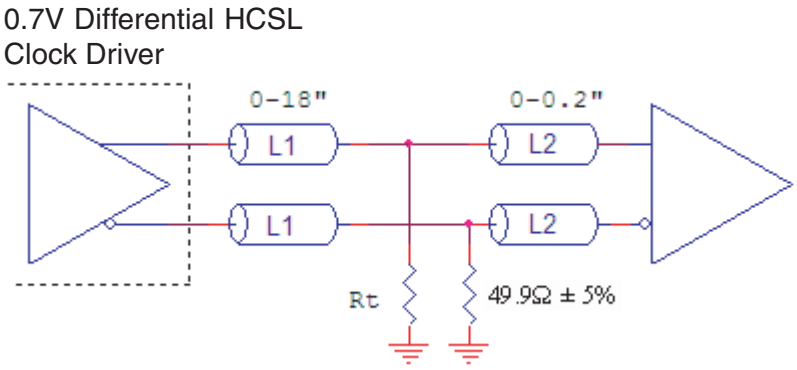


FIGURE 6B. RECOMMENDED TERMINATION

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 28 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	64.5°C/W	60.4°C/W	58.5°C/W

TRANSISTOR COUNT

The transistor count for ICS841604I is: 2785

PACKAGE OUTLINE - G SUFFIX FOR 28 LEAD TSSOP

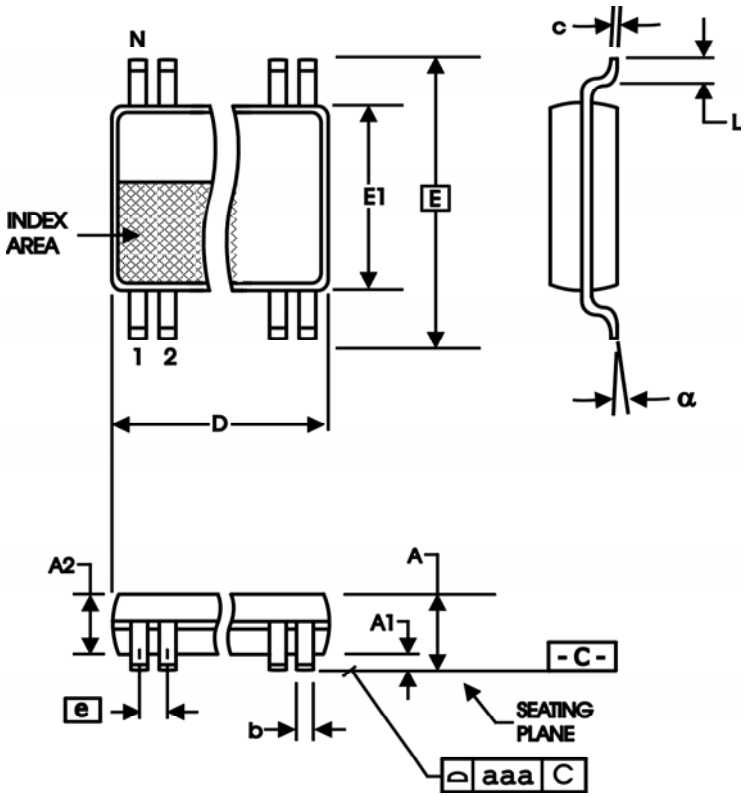


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	8.10 BASIC	
E1	6.00	6.20
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS841604AGI	ICS841604AGI	28 Lead TSSOP	tube	-40°C to 85°C
ICS841604AGIT	ICS841604AGI	28 Lead TSSOP	1000 tape & reel	-40°C to 85°C
ICS841604AGILF	TBD	28 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS841604AGILFT	TBD	28 Lead "Lead-Free" TSSOP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

www.IDT.com