HARRIS SEMICONDUCTOR

DG458, DG459

PRELIMINARY

November 1994

Single 8-Channel/Differential 4-Channel Fault Protected Analog Multiplexers

Features

- Fault and Overvoltage Protection
- ON-Resistance <1.5kΩ (+25°C)
- Low Power Consumption (P_D <3mW)
- Fast Switching Action
  - t_A <500ns
  - $t_{ON/OFF(EN)}$ <250ns
- Fail Safe with Power Loss (No Latch-Up)
- Upgrade from IH5108/IH5208
- TTL, CMOS Compatible Logic

Applications

- Data Acquisition Systems
- Audio Switching Systems
- Automatic Testers
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Analog Selector Switch

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG458DJ	-40°C to +85°C	16 Lead Plastic DIP
DG458DY	-40°C to +85°C	16 Lead SOIC (W)
DG458AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG459DJ	-40°C to +85°C	16 Lead Plastic DIP
DG459DY	-40°C to +85°C	16 Lead SOIC (W)
DG459AK/883	-55°C to +125°C	16 Lead Ceramic DIP

Description

The DG458 Single 8-Channel and DG459 Differential 4-Channel monolithic CMOS analog multiplexers are drop-in replacements for the popular IH5108 and IH5208 series devices. They each include an array of eight analog switches, a series N-channel/P-channel/N-channel fault protection circuit, a TTL/CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds and an ENABLE input for device selection when several multiplexers are present.

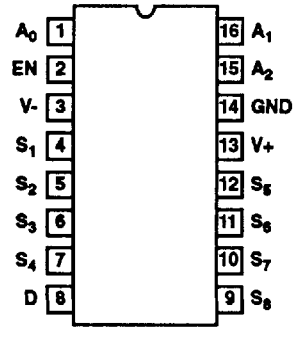
The DG458 and DG459 feature lower signal ON resistance (450Ω typical) and faster switch transition time (200ns typical) compared to the IH5108 or IH5208. The improvements in the DG458 series are made possible by using a high-voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies.

The 44V maximum voltage range permits controlling 20V peak-to-peak signals, while withstanding continuous overvoltages up to ±35V, providing an open fault circuit.

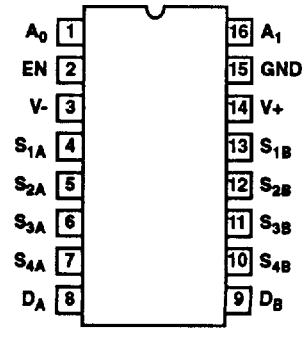
The analog switches are bilateral, break-before-make, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Pinouts

DG458 (CDIP, PDIP, SOIC)
TOP VIEW



DG459 (CDIP, PDIP, SOIC)
TOP VIEW

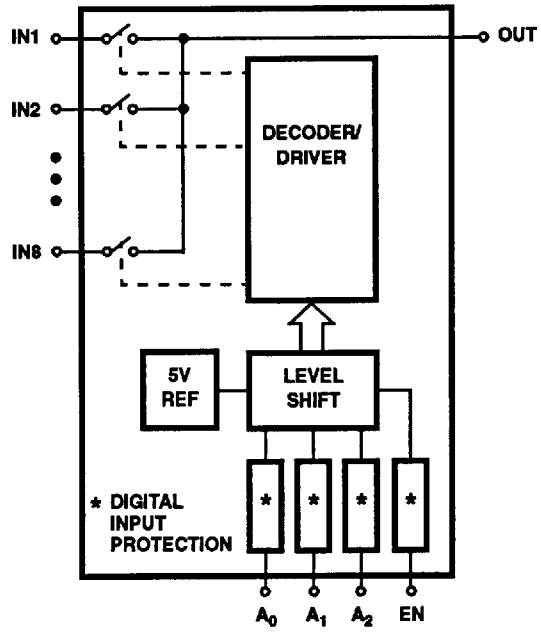


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

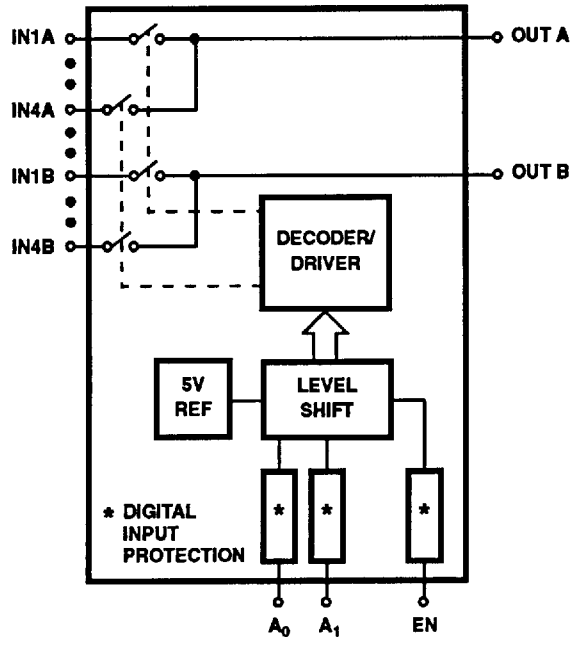
File Number 3280.2

Functional Block Diagrams

DG458



DG459



Absolute Maximum Ratings

V+ to V- ..... +44V
V+ to GND 22V
V- to GND ..... -25V
Digital Input, V_{EN}, V_A ..... (V-) -4V to (V+) +4V
Analog Input Overvoltage w/Power On, V_S .... (V-) -20V to (V+) +20V
Analog Input Overvoltage w/Power Off, V_S ..... -35V to +35V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed 1ms, 10% Duty Cycle Max)
Storage Temperature Range (D Suffix) ..... -65°C to +125°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance ..... θ_{JA}
Plastic DIP Package ..... 145°C/W
SOIC Package ..... 100°C/W
Operating Temperature (D Suffix) ..... -40°C to +85°C
Junction Temperature (D Suffix) ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... ±20V Max
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0.8V Max
Input High Voltage ..... 2.4V Min
Input Rise and Fall Time ..... ≤20ns

Electrical Specifications

V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 1) TEMP	D SUFFIX -40°C TO +85°C (NOTE 3) MIN	(NOTE 2) TYP	(NOTE 3) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_A	See Figure 15	+25°C	-	200	500	ns
Break-Before-Make Time, t_{BBM}	See Figure 16	+25°C	10	45	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	See Figure 17	+25°C	-	140	250	ns
		Full	-	-	500	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$		+25°C	-	50	250	ns
		Full	-	-	500	ns
Settling Time, t_S	To 0.1%	+25°C	-	0.5	-	µs
	To 0.01%	+25°C	-	1.5	-	µs
OFF Isolation	V_{EN} = 0V, R_L = 1kΩ C_L = 15pF V_S = $3V_{RMS}$, f = 100kHz (Note 7)	+25°C	-	90	-	dB
Logic Input Capacitance, C_{IN}	f = 1MHz	+25°C	-	5	-	pF
Source OFF Capacitance, $C_{S(OFF)}$		+25°C	-	5	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$						
DG458		+25°C	-	15	-	pF
DG459		+25°C	-	10	-	pF
Drain ON Capacitance, $C_{D(ON)}$						
DG458		+25°C	-	40	-	pF
DG459		+25°C	-	35	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}	Note 4	Full	-10	-	10	V
Drain-Source ON Resistance, $R_{DS(ON)}$	V_D = ±9.5V, I_S = -400µA (Note 5)	+25°C	-	0.45	1.5	kΩ
		Full	-	-	1.8	kΩ
	V_D = ±5V, I_S = -400µA (Note 5)	+25°C	-	180	400	Ω
$R_{DS(ON)}$ Matching Between Channels, $\Delta R_{DS(ON)}$	V_D = 0V, I_S = -400µA (Note 6)	+25°C	-	6	-	%

Electrical Specifications V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 1) TEMP	D SUFFIX -40°C TO +85°C (NOTE 3) MIN	(NOTE 2) TYP	(NOTE 3) MAX	UNITS
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ∓10V	+25°C	-1	0.03	1	nA
		Full	-20	-	20	nA
Drain Off Leakage Current, $I_{D(OFF)}$						
DG458	V_{EN} = 0V, V_S = ∓10V, V_D = ±10V	+25°C	-1	0.1	1	nA
		Full	-50	-	50	nA
DG459		+25°C	-2	0.1	2	nA
		Full	-25	-	25	nA
Differential Off Drain Leakage Current, I_{DIFF}	DG459 Only	Full	-20	-	20	nA
Drain On Leakage Current, $I_{D(ON)}$						
DG458	V_S = V_D = ±10V, V_{AL} = 0.8V, V_{AH} = 2.4V, Sequence Each Switch On	+25°C	-5	0.1	5	nA
		Full	-50	-	50	nA
DG459		+25°C	-5	0.05	5	nA
		Full	-25	-	25	nA
DIGITAL CONTROL						
Input Low Threshold, V_{AL}		Full	-	-	0.8	V
Input Low Threshold, V_{AL}		Full	2.4	-	-	V
Logic Input Control, I_A	V_A = 2.4V or 0.8V	Full	-	-1	1	µA
FAULT						
Output Leakage Current (With Overvoltage), $I_{D(OFF)}$	V_S = ±33V, V_D = 0V (See Figure 14)	+25°C	-	0.02	-	nA
Input Leakage Current (With Overvoltage), $I_{S(OFF)}$	V_S = ±25V, V_D = ±10V (See Figure 14)	+25°C	-10	0.005	10	µA
Input Leakage Current (With Power Supplies Off), $I_{S(OFF)}$	V_A = ±25V, V_{SUPS} = 0V, V_D = A_0 = A_1 = A_2 = EN = 0V	+25°C	-5	0.001	5	µA
POWER SUPPLIES						
Positive Supply Current, I+	V_{EN} = High or Low V_A = 0V	+25°C	-	0.05	0.1	mA
		Full	-	-	0.2	mA
Negative Supply Current, I-		+25°C	-0.1	-0.01	-	mA
		Full	-0.2	-	-	mA
Power Supply Range for Continuous Operation		+25°C	±4.5	-	±18	V

NOTES:

1. Full = as determined by the operating temperature suffix.
2. Typical values are for Design Aid Only, not guaranteed nor subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. When the analog signal exceeds the +13.5V or -12V $R_{DS(ON)}$ starts to rise until only leakage currents flow.
5. Electrical Characteristics such as $R_{DS(ON)}$ change when supplies other than ±15V are used.
6. $$\Delta R_{DS(ON)} = \frac{R_{DS(ON)}MAX - R_{DS(ON)}MIN}{\Delta R_{DS(ON)}AVE}$$
7. Worst case is channel 4 due to close proximity of input and output leads of package. This parameter varies with package style.

Typical Performance Curves +25°C, Unless Otherwise Specified

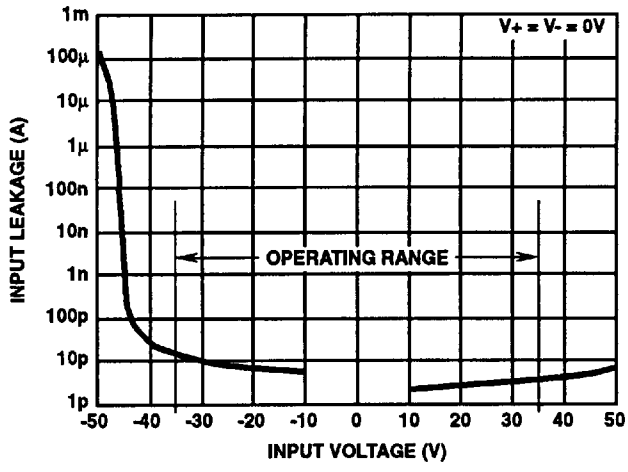


FIGURE 1. INPUT LEAKAGE vs INPUT VOLTAGE

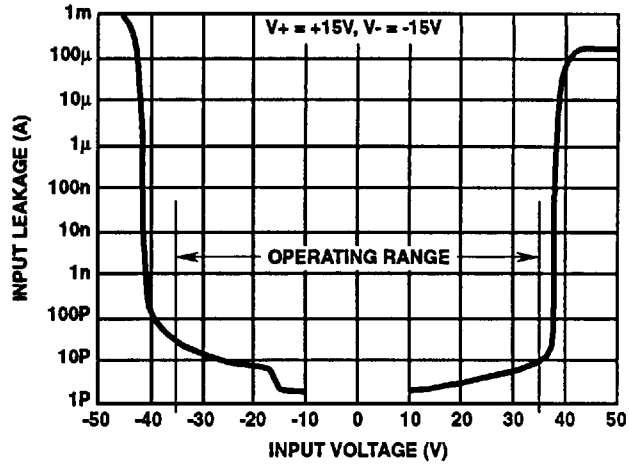


FIGURE 2. OFF CHANNEL LEAKAGE CURRENT vs INPUT VOLTAGE

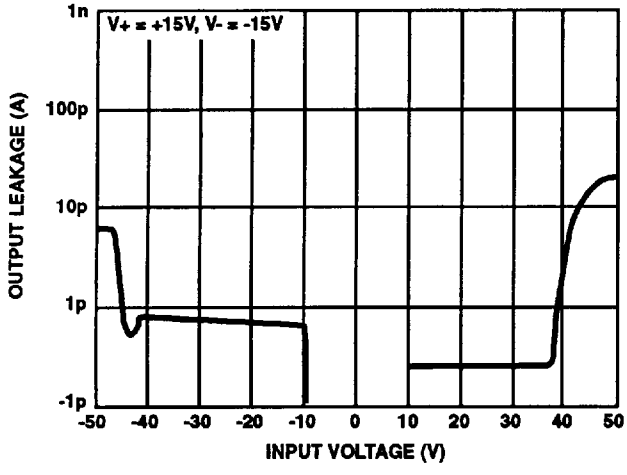


FIGURE 3. OUTPUT LEAKAGE vs OFF CHANNEL OVERVOLTAGE

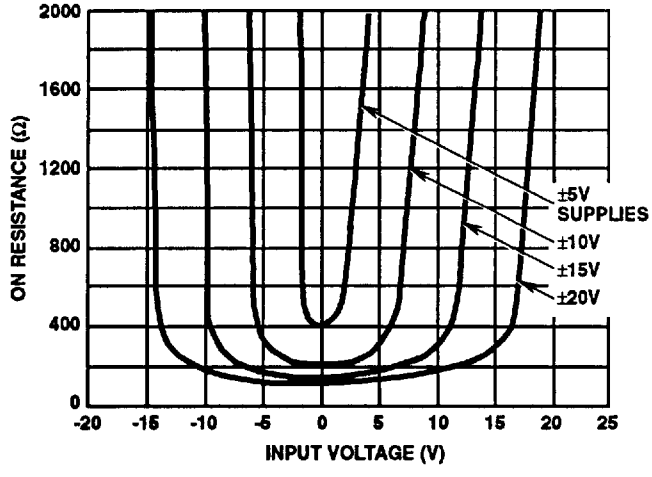


FIGURE 4. $R_{DS(ON)}$ vs INPUT VOLTAGE

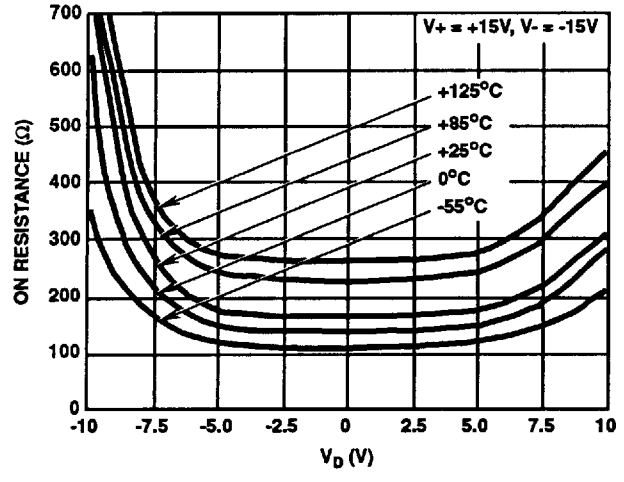


FIGURE 5. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

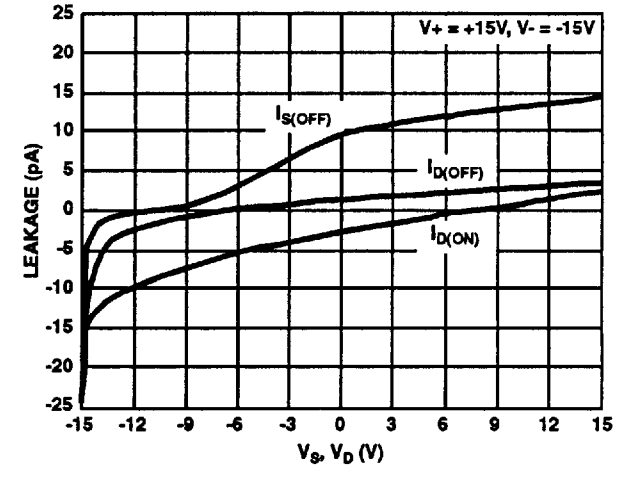


FIGURE 6. LEAKAGE CURRENT vs V_S, V_D

Typical Performance Curves +25°C, Unless Otherwise Specified (Continued)

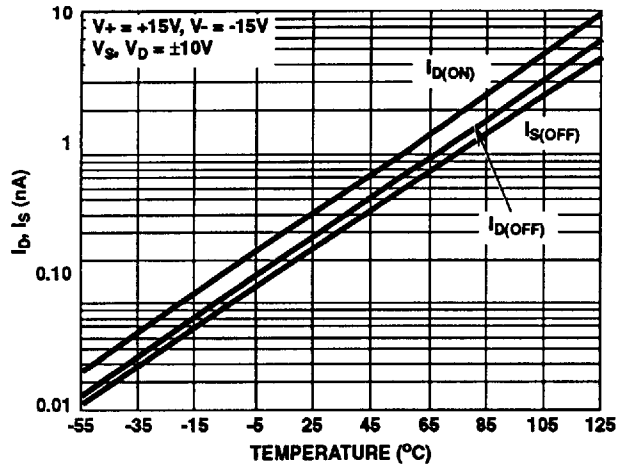


FIGURE 7. LEAKAGE CURRENT vs TEMPERATURE

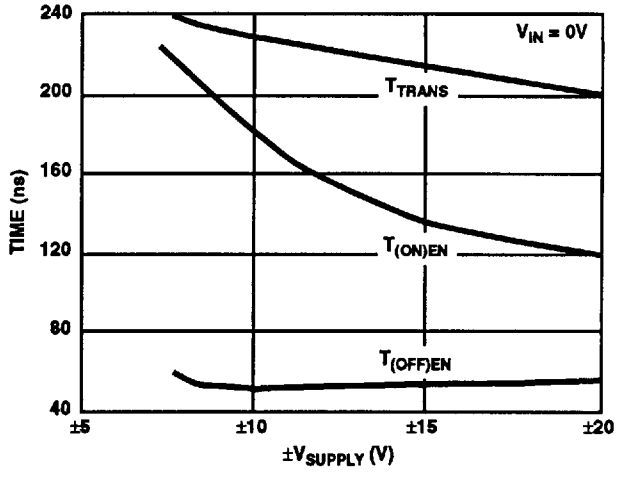


FIGURE 8. SWITCHING TIMES (t_{RANS}, t_{ON}, t_{OFF}) vs ±V SUPPLIES

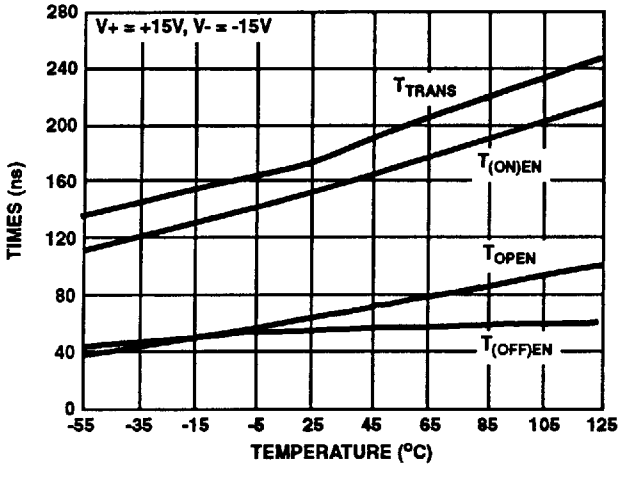


FIGURE 9. SWITCHING TIMES vs TEMPERATURE

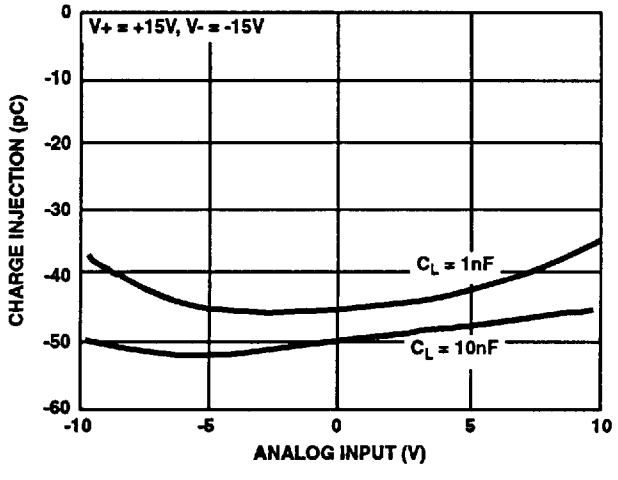


FIGURE 10. Q_{INJ} vs V_S

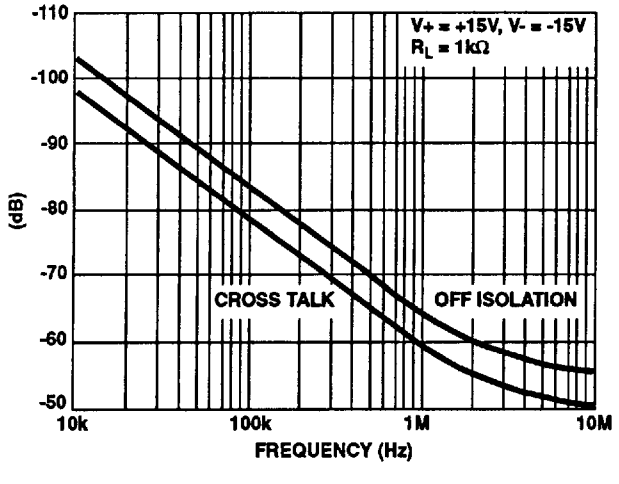


FIGURE 11. OFF ISOLATION AND $CROSS_{TALK}$ vs FREQUENCY3

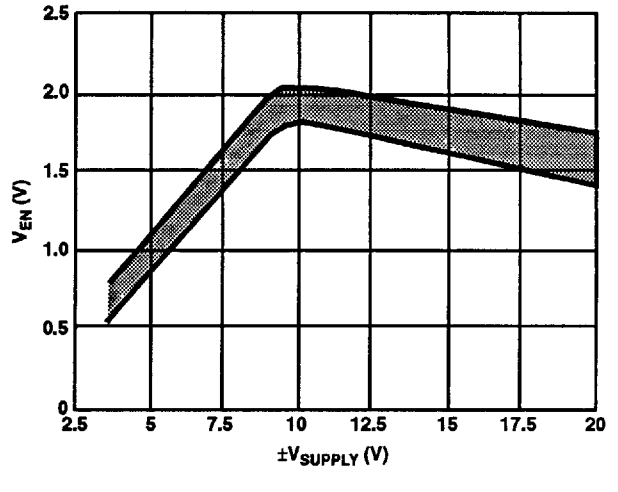


FIGURE 12. LOGIC INPUT SWITCHING THRESHOLD vs ±V SUPPLIES

Pin Description

PIN	SYMBOL	DESCRIPTION
DG458		
1	A_0	Logic decode input (bit 0, LSB)
2	EN	Enable input
3	V-	Negative power supply terminal
4	S_1	Source (input) for channel 1
5	S_2	Source (input) for channel 2
6	S_3	Source (input) for channel 3
7	S_4	Source (input) for channel 4
8	D	Drain (output)
9	S_8	Source (input) for channel 8
10	S_7	Source (input) for channel 7
11	S_6	Source (input) for channel 6
12	S_5	Source (input) for channel 5
13	V+	Positive power supply terminal (substrate)
14	GND	Ground terminal (Logic Common)
15	A_2	Logic decode input (bit 2, MSB)
16	A_1	Logic decode input (bit 1)
DG459		
1	A_0	Logic decode input (bit 0, LSB)
2	EN	Enable input
3	V-	Negative power supply terminal
4	S_{1A}	Source (input) for channel 1A
5	S_{2A}	Source (input) for channel 2A
6	S_{3A}	Source (input) for channel 3A
7	S_{4A}	Source (input) for channel 4A
8	D_A	Drain A (output a)
9	D_B	Drain B (output b)
10	S_{4B}	Source (input) for channel 4B
11	S_{3B}	Source (input) for channel 3B
12	S_{2B}	Source (input) for channel 2B
13	S_{1B}	Source (input) for channel 1B
14	V+	Positive power supply terminal
15	GND	Ground terminal (Logic Common)
16	A_1	Logic decode input (bit 1, MSB)

DG458 TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG459 TRUTH TABLE

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1A, 1B
0	1	1	2A, 2B
1	0	1	3A, 3B
1	1	1	4A, 4B

NOTES:

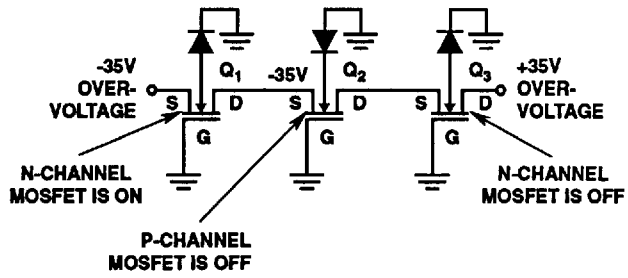
1. V_{AH} Logic "1" ≥ 2.4V
2. V_{AL} Logic "0" ≤0.8V

Detailed Description

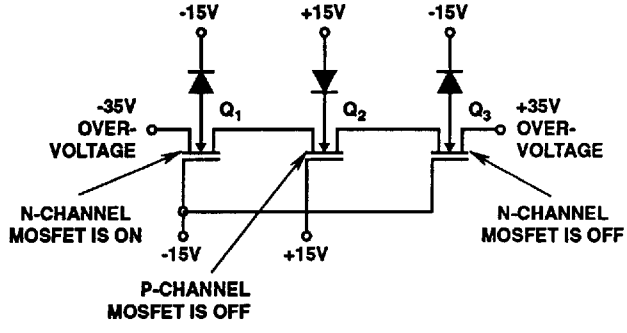
The DG458 and DG459 multiplexers are full fault and overvoltage protected for continuous input voltages up to ±35V whether or not voltage is applied to the power supply pins (V+, V-). These multiplexers are built on a high voltage junction-isolated silicon gate CMOS process. Two n-channel and one p-channel MOSFETs are connected in series to form each channel (Figure 13).

Within the normal analog signal range (±10V), the $R_{DS(ON)}$ variation as a function of analog signal voltage is comparable to that of the classic parallel n-MOS and p-MOS switches.

When the analog signal approaches or exceeds either supply rail, even for an on-channel, one of the three series MOSFETs gets cut off, providing inherent protection against overvoltages even if the multiplexer power supply voltages are lost. This protection is good up to the breakdown voltage of the respective series MOSFETs. Under fault conditions only sub microamp leakage currents can flow in or out of the multiplexer. This not only provides protection for the multiplexer and succeeding circuitry, but it allows normal, undisturbed operation of all other channels. Additionally, in case of power loss to the multiplexer, the loading caused on the transducers and signal sources is insignificant, therefore redundant multiplexers can be used on critical applications such as telemetry and avionics.



13A. OVERVOLTAGE WITH MUX POWER OFF



13B. OVERVOLTAGE WITH MUX POWER ON

FIGURE 13. OVERVOLTAGE PROTECTION

Test Circuits

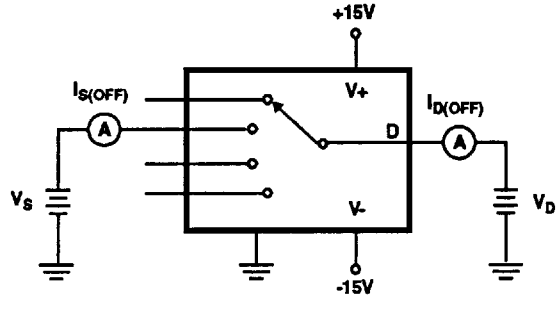


FIGURE 14. ANALOG INPUT OVERVOLTAGE

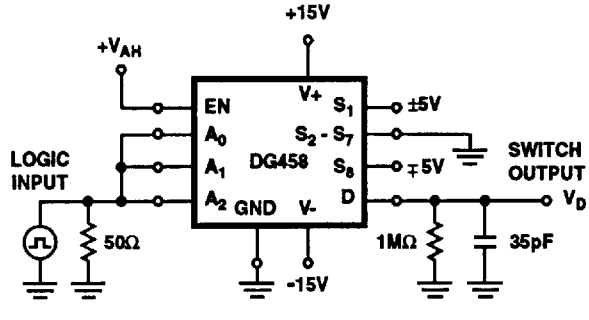


FIGURE 15A.

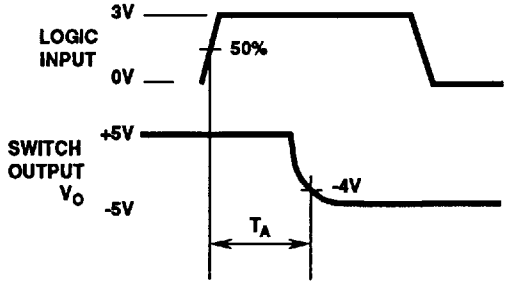


FIGURE 15B.

FIGURE 15. TRANSITION TIME

Test Circuits (Continued)

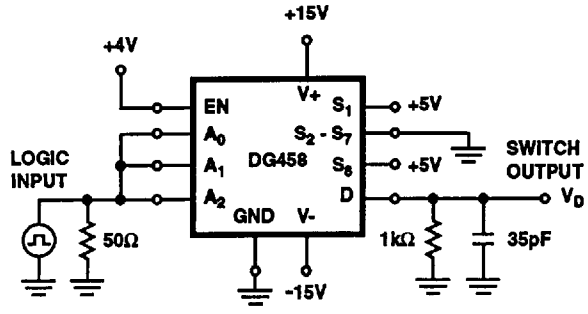


FIGURE 16A.

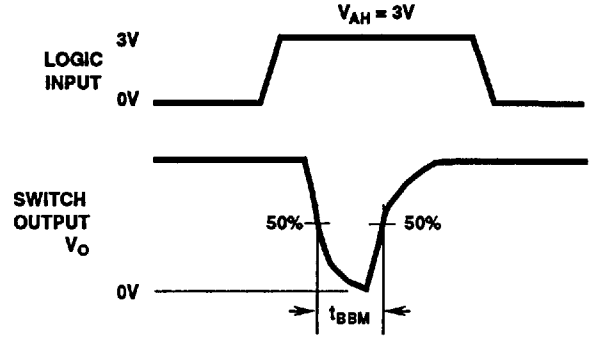


FIGURE 16B.

FIGURE 16. BREAK-BEFORE-MAKE TIME

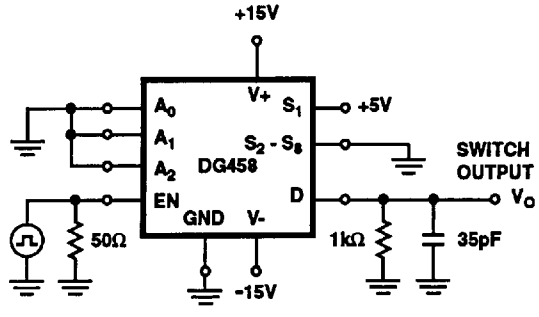


FIGURE 17A.

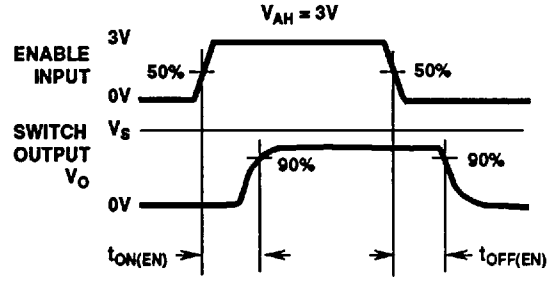


FIGURE 17B.

FIGURE 17. ENABLE DELAY

Die Characteristics

DIE DIMENSIONS:
2490µm x 4060µm x 485µm ±25µm

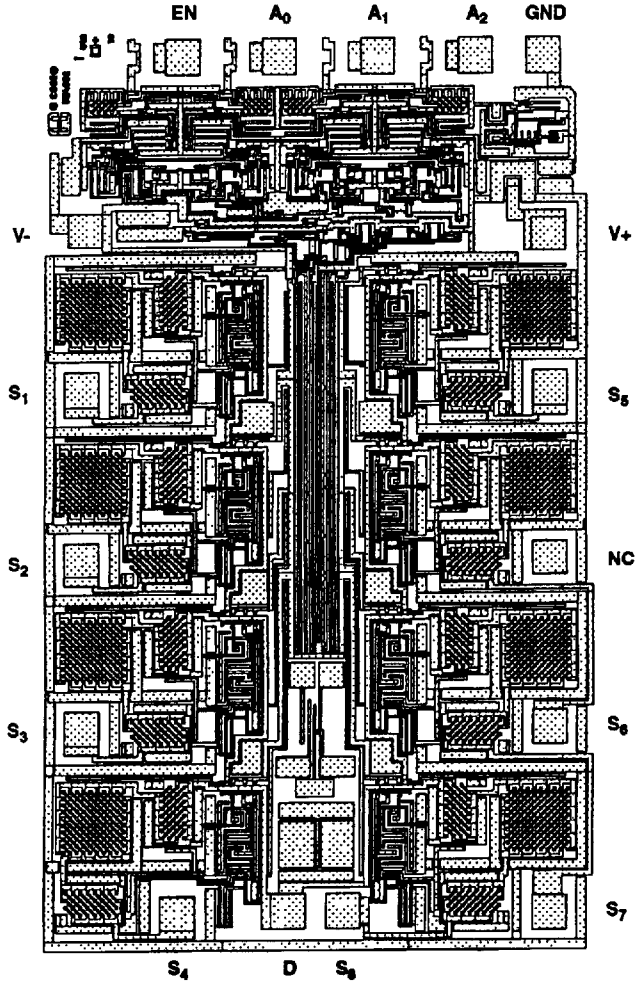
METALLIZATION:
Type: Si - Al
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

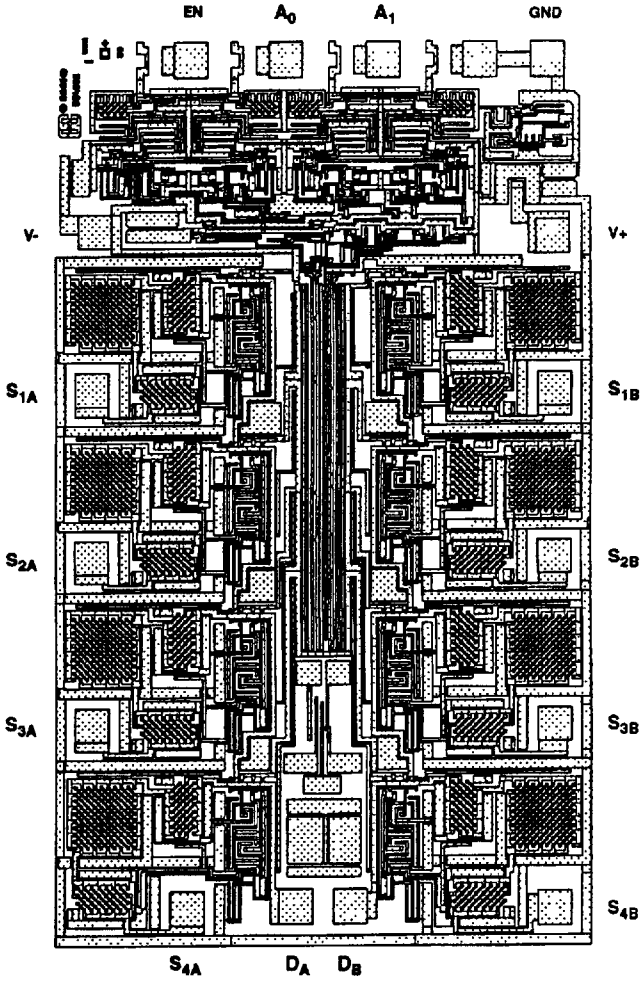
WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

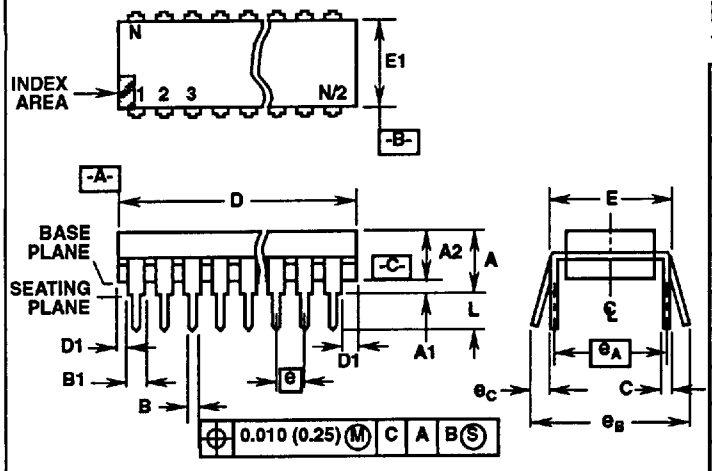
DG458



DG459



Dual-In-Line Plastic Packages (PDIP)



E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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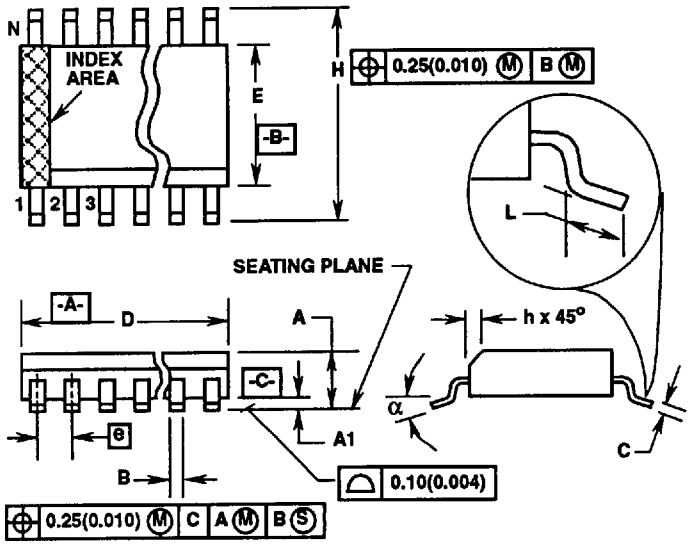
NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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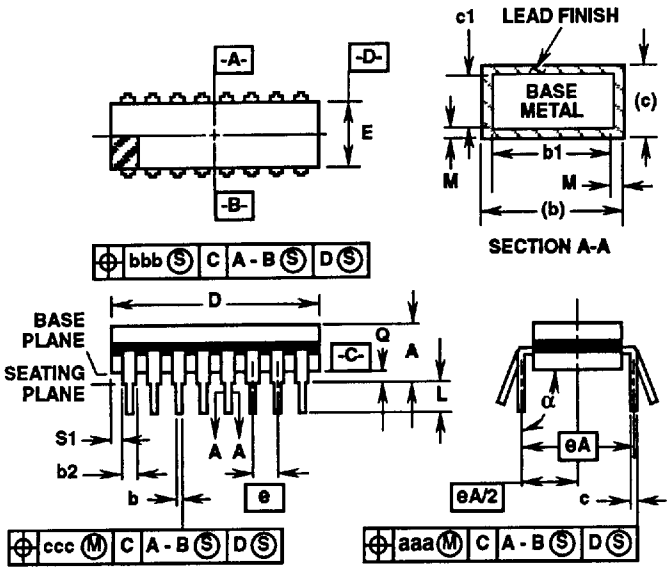
NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.